EMB1412 MOSFET Gate Driver

Check for Samples: EMB1412

FEATURES

- **Compound CMOS and Bipolar Outputs Reduce Output Current Variation**
- **7A sink/3A Source Current**
- **Fast Propagation Times (25 ns Typical)**
- **Fast Rise and Fall Times (14 ns/12 ns Rise/Fall with 2 nF Load)**
- **Inverting and Non-Inverting Inputs Provide Either Configuration with a Single Device**
- **Supply Rail Under-Voltage Lockout Protection**
- **Dedicated Input Ground (IN_REF) for Split Supply or Single Supply Operation**
- **Thermally Enhanced 8-Pin VSSOP Package**
- **Output Swings from V_{CC} to V_{EE} Which can be Negative Relative to Input Ground**

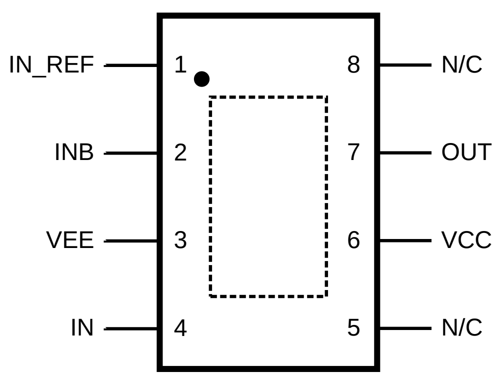
APPLICATIONS

- **Battery Management Systems**

DESCRIPTION

The EMB1412 MOSFET gate driver provides high peak gate drive current in 8-Lead exposed-pad VSSOP package, with improved power dissipation required for high frequency operation. The compound output driver stage includes MOS and bipolar transistors operating in parallel that together sink more than 7A peak from capacitive loads. Combining the unique characteristics of MOS and bipolar devices reduces drive current variation with voltage and temperature. Under-voltage lockout protection is provided to prevent damage to the MOSFET due to insufficient gate turn-on voltage. The EMB1412 provides both inverting and non-inverting inputs to satisfy requirements for inverting and non-inverting gate drive with a single device type.

PIN CONFIGURATIONS



8-Pin VSSOP
See DGN Package

ORDERING INFORMATION

Order Number	Package Type	TI Package Drawing	Supplied As
EMB1412MY	Exposed DAP VSSOP	DGN	1000 shipped on Tape & Reel
EMB1412MYX	Exposed DAP VSSOP	DGN	3500 shipped on Tape & Reel
EMB1412MYE	Exposed DAP VSSOP	DGN	250 shipped on Tape & Reel

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN DESCRIPTIONS

Pin	Name	Description	Application Information
4	IN	Non-inverting input pin	TTL compatible thresholds. Pull up to VCC when not used.
3	VEE	Power ground for driver outputs	Connect to either power ground or a negative gate drive supply for positive or negative voltage swing.
6	VCC	Positive Supply voltage input	Locally decouple to VEE. The decoupling capacitor should be located close to the chip.
7	OUT	Gate drive output	Capable of sourcing 3A and sinking 7A. Voltage swing of this output is from VEE to VCC.
1	IN_REF	Ground reference for control inputs	Connect to power ground (VEE) for standard positive only output voltage swing. Connect to system logic ground when VEE is connected to a negative gate drive supply.
2	INB	Inverting input pin	TTL compatible thresholds. Connect to IN_REF when not used.
5, 8	N/C	Not internally connected	
- - -	Exposed Pad	Exposed Pad, underside of package	Internally bonded to the die substrate. Connect to VEE ground pin for low thermal impedance.

ABSOLUTE MAXIMUM RATINGS(1)

V_{CC} to V_{EE}	−0.3V to 15V
V_{CC} to IN_REF	−0.3V to 15V
IN/INB to IN_REF	−0.3V to 15V
IN_REF to V_{EE}	−0.3V to 5V
Storage Temperature Range	−55°C to +150°C
Maximum Junction Temperature	+150°C
Operating Junction Temperature	−40°C+125°C
ESD Rating	2kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.

ELECTRICAL CHARACTERISTICS

T_J = −40°C to +125°C, V_{CC} = 12V, INB = IN_REF = V_{EE} = 0V, No Load on output, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
V_{CC}	V_{CC} Operating Range	V_{CC} – IN_REF and V_{CC} - V_{EE}	3.5		14	V
UVLO	V_{CC} Under-voltage Lockout (rising)	V_{CC} – IN_REF	2.4	3.0	3.5	V
V_{CCH}	V_{CC} Under-voltage Hysteresis			230		mV
I_{CC}	V_{CC} Supply Current			1.0	2.0	mA
CONTROL INPUTS						
V_{IH}	Logic High		2.3			V
V_{IL}	Logic Low				0.8	V
V_{thH}	High Threshold		1.3	1.75	2.3	V
V_{thL}	Low Threshold		0.8	1.35	2.0	V
HYS	Input Hysteresis			400		mV
I_{IL}	Input Current Low	IN = INB = 0V	-1	0.1	1	µA
I_{IH}	Input Current High	IN = INB = V_{CC}	-1	0.1	1	µA
OUTPUT DRIVER						
R_{OH}	Output Resistance High	I_{OUT} = -10mA (1)		30	50	Ω
R_{OL}	Output Resistance Low	I_{OUT} = 10mA (1)		1.4	2.5	Ω
I_{SOURCE}	Peak Source Current	OUT = V_{CC}/2, 200ns pulsed current		3		A
I_{SINK}	Peak Sink Current	OUT = V_{CC}/2, 200ns pulsed current		7		A
SWITCHING CHARACTERISTICS						
td1	Propagation Delay Time Low to High, IN/ INB rising (IN to OUT)	C_{LOAD} = 2 nF		25	40	ns
td2	Propagation Delay Time High to Low, IN / INB falling (IN to OUT)	C_{LOAD} = 2 nF		25	40	ns
tr	Rise time	C_{LOAD} = 2 nF		14		ns
tf	Fall time	C_{LOAD} = 2 nF		12		ns
LATCHUP PROTECTION						
	AEC –Q100, METHOD 004	T_J = 150°C		500		mA
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient, 0 LFPM Air Flow	VSSOP Package		60		°C/W
θ_{JC}	Junction to Case	VSSOP Package		4.7		°C/W

(1) The output resistance specification applies to the MOS device only. The total output current capability is the sum of the MOS and Bipolar devices.

TIMING WAVEFORMS

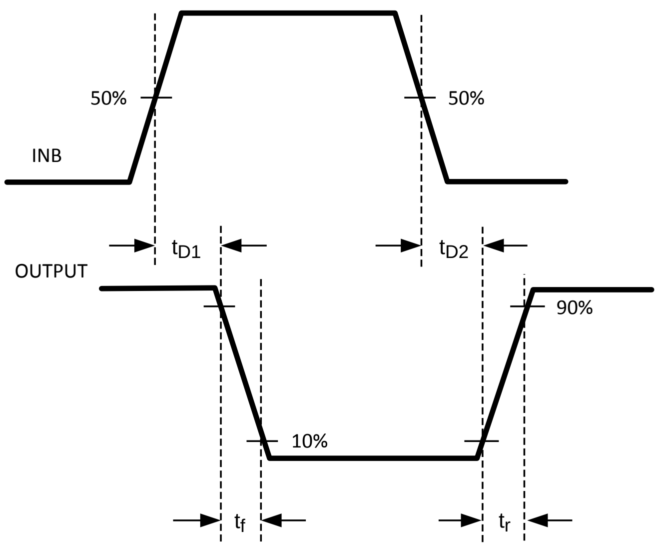


Figure 1. (a)

Figure 2. (b)

Figure 3. (a) Inverting, (b) Non-Inverting

DETAILED OPERATING DESCRIPTION

The EMB1412 is a high speed , high peak current (7A) single channel MOSFET driver. The high peak output current of the EMB1412 will switch power MOSFET's on and off with short rise and fall times, thereby reducing switching losses considerably. The EMB1412 includes both inverting and non-inverting inputs that give the user flexibility to drive the MOSFET with either active low or active high logic signals. The driver output stage consists of a compound structure with MOS and bipolar transistor operating in parallel to optimize current capability over a wide output voltage and operating temperature range. The bipolar device provides high peak current at the critical Miller plateau region of the MOSFET V_{GS} , while the MOS device provides rail-to-rail output swing. The totem pole output drives the MOSFET gate between the gate drive supply voltage V_{CC} and the power ground potential at the V_{EE} pin.

The control inputs of the driver are high impedance CMOS buffers with TTL compatible threshold voltages. The negative supply of the input buffer is connected to the input ground pin IN_REF. An internal level shifting circuit connects the logic input buffers to the totem pole output drivers. The level shift circuit and separate input/output ground pins provide the option of single supply or split supply configurations. When driving the MOSFET gates from a single positive supply, the IN_REF and V_{EE} pins are both connected to the power ground.

The isolated input and output stage grounds provide the capability to drive the MOSFET to a negative V_{GS} voltage for a more robust and reliable off state. In split supply configuration, the IN_REF pin is connected to the ground of the controller which drives the EMB1412 inputs. The V_{EE} pin is connected to a negative bias supply that can range from the IN_REF potential to as low as 14 V below the Vcc gate drive supply. For reliable operation, the maximum voltage difference between V_{CC} and IN_REF or between V_{CC} and V_{EE} is 14V.

The minimum recommended operating voltage between Vcc and IN_REF is 3.5V. An Under Voltage Lock Out (UVLO) circuit is included in the EMB1412 which senses the voltage difference between V_{CC} and the input ground pin, IN_REF. When the V_{CC} to IN_REF voltage difference falls below 2.8V the driver is disabled and the output pin is held in the low state. The driver will resume normal operation when the V_{CC} to IN_REF differential voltage exceeds 3.0V.

LAYOUT CONSIDERATIONS

Attention must be given to board layout when using EMB1412. Some important considerations include:

1. A Low ESR/ESL capacitor must be connected close to the IC and between the V_{CC} and V_{EE} pins to support high peak currents being drawn from V_{CC} during turn-on of the MOSFET.
2. Proper grounding is crucial. The driver needs a very low impedance path for current return to ground avoiding inductive loops. Two paths for returning current to ground are a) between EMB1412 IN_REF pin and the ground of the circuit that controls the driver inputs and b) between EMB1412 V_{EE} pin and the source of the power MOSFET being driven. Both paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance. These ground paths should be distinctly separate to avoid coupling between the high current output paths and the logic signals that drive the EMB1412. With rise and fall times in the range of 10 to 30nsec, care is required to minimize the lengths of current carrying conductors to reduce their inductance and EMI from the high di/dt transients generated when driving large capacitive loads.
3. If either channel is not being used, the respective input pin (IN or INB) should be connected to either V_{EE} or V_{CC} to avoid spurious output signals.

THERMAL PERFORMANCE

The primary goal of the thermal management is to maintain the integrated circuit (IC) junction temperature (Tj) below a specified limit to ensure reliable long term operation. The maximum T_J of IC components should be estimated in worst case operating conditions. The junction temperature can be calculated based on the power dissipated on the IC and the junction to ambient thermal resistance θ_{JA} for the IC package in the application board and environment. The θ_{JA} is not a given constant for the package and depends on the PCB design and the operating environment.

REVISION HISTORY

Changes from Original (May 2013) to Revision A **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
EMB1412MY/NOPB	PREVIEW	MSOP-PowerPAD	DGN	8		Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SA3B	
EMB1412MYE/NOPB	PREVIEW	MSOP-PowerPAD	DGN	8		Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SA3B	
EMB1412MYX/NOPB	PREVIEW	MSOP-PowerPAD	DGN	8		Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SA3B	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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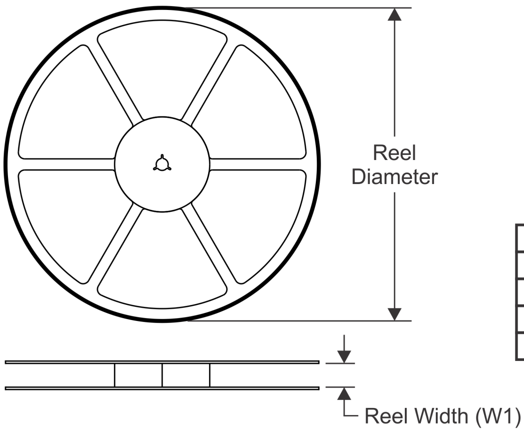
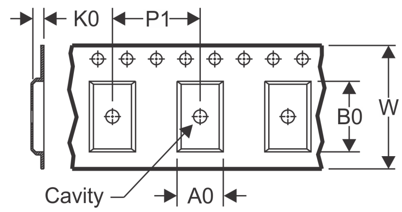
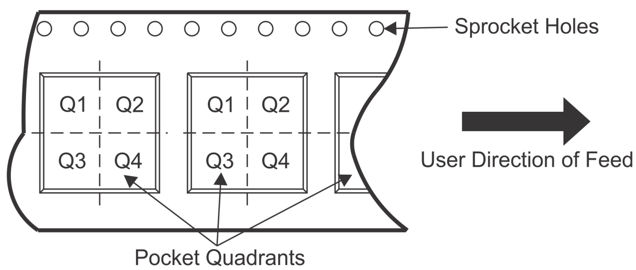
TAPE AND REEL INFORMATION





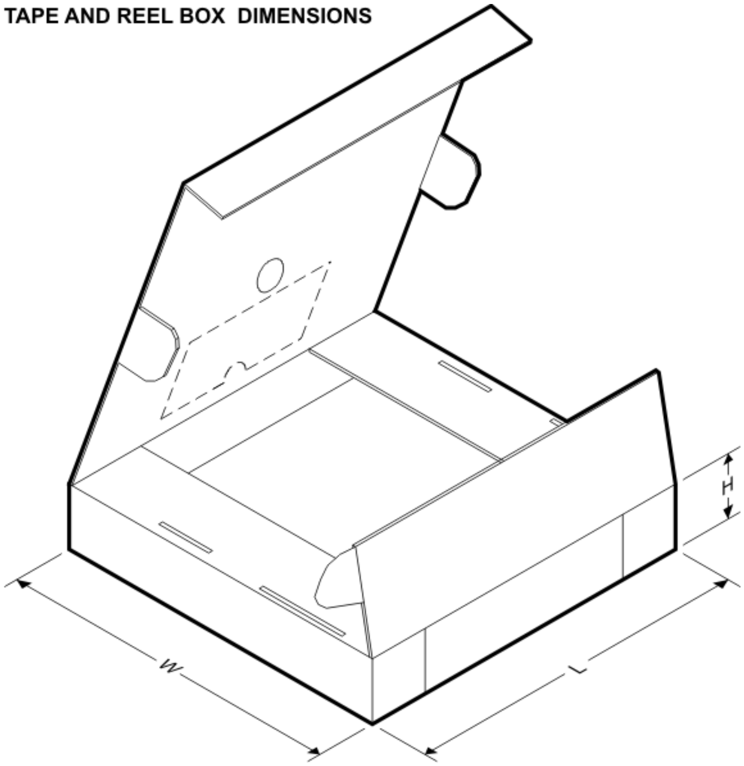
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
EMB1412MY/NOPB	MSOP-PowerPAD	DGN	8	0	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
EMB1412MYE/NOPB	MSOP-PowerPAD	DGN	8	0	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
EMB1412MYX/NOPB	MSOP-PowerPAD	DGN	8	0	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

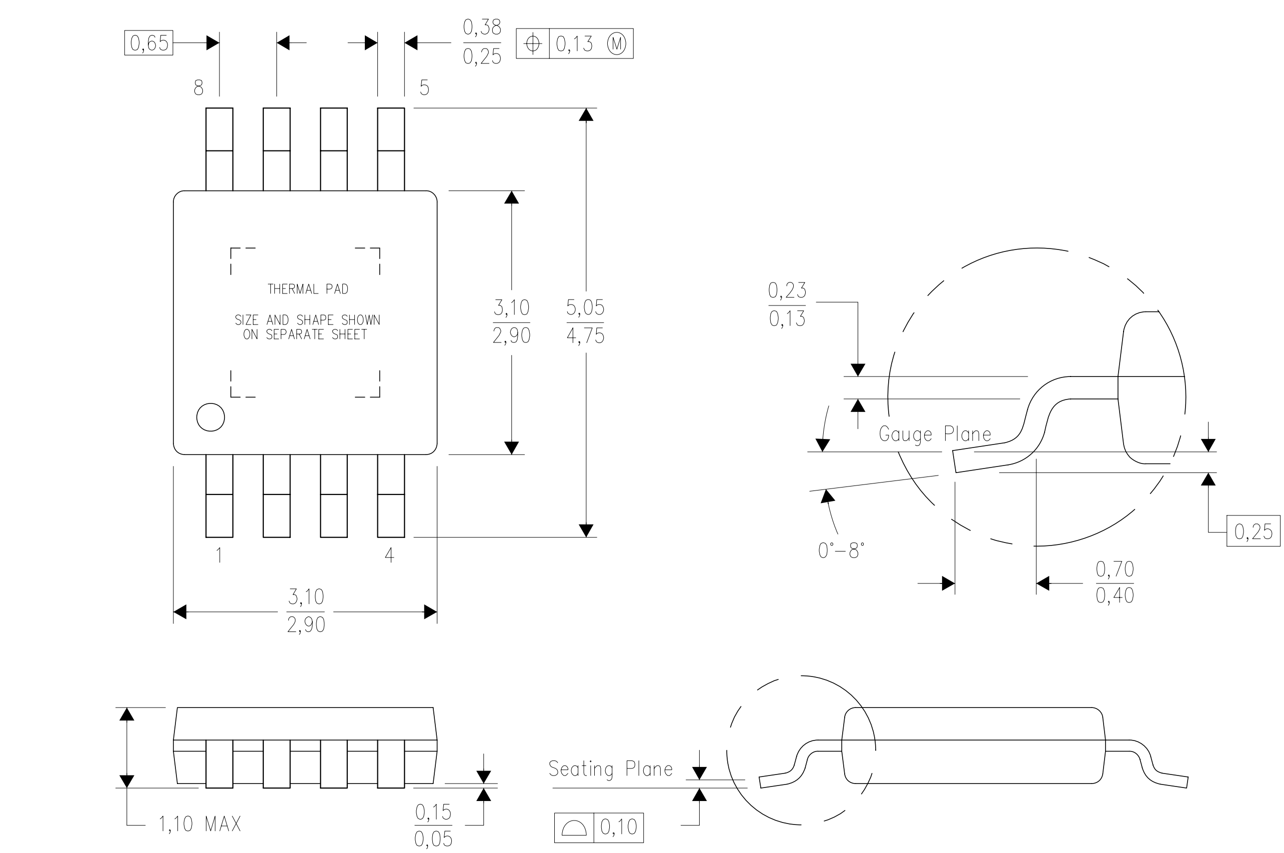
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
EMB1412MY/NOPB	MSOP-PowerPAD	DGN	8	0	210.0	185.0	35.0
EMB1412MYE/NOPB	MSOP-PowerPAD	DGN	8	0	210.0	185.0	35.0
EMB1412MYX/NOPB	MSOP-PowerPAD	DGN	8	0	367.0	367.0	35.0

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.