HB56D436 Series

4,194,304-word × 36-bit High Density Dynamic RAM Module

The HB56D436 is a 4 M × 36 dynamic RAM module, mounted 8 pieces of 16-Mbit DRAM (HM5117400AS) sealed in SOJ package and 4 pieces of 4-Mbit DRAM (HM514100BS/CS) sealed in SOJ package. An outline of the HB56D436 is 72-pin single in-line package. Therefore, the HB56D436 makes high density mounting possible without surface mount technology. The HB56D436 provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ on the its module board.

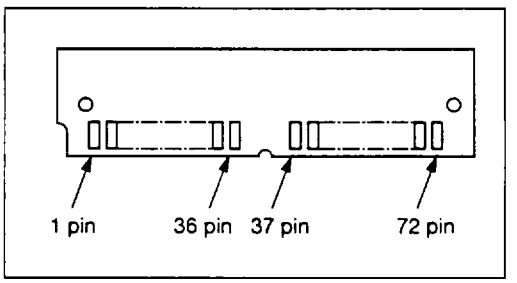
Feature

- 72-pin single in-line package
  - Lead pitch: 1.27 mm
- Single 5 V (± 5%) supply
- High speed
  - Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
  - Active mode: 6.93 W/6.30 W/5.67 W (max)
  - Standby mode: 126 mW (max)
- Fast page mode capability
- 2,048 refresh cycle/32 ms
- 2 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- TTL compatible.

Ordering Information

Type No.	Access time	Package	Contact pad
HB56D436BR-6A	60 ns	72-pin SIP socket type	Gold
HB56D436BR-7A	70 ns		
HB56D436BR-8A	80 ns		
HB56D436SBR-6A	60 ns	72-pin SIP socket type	Solder
HB56D436SBR-7A	70 ns		
HB56D436SBR-8A	80 ns		
HB56D436BR-6AC	60 ns	72-pin SIP socket type	Gold
HB56D436BR-7AC	70 ns		
HB56D436BR-8AC	80 ns		
HB56D436SBR-6AC	60 ns	72-pin SIP socket type	Solder
HB56D436SBR-7AC	70 ns		
HB56D436SBR-8AC	80 ns		

Pin Arrangement



Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	19	A10	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V_{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	V_{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V_{SS}

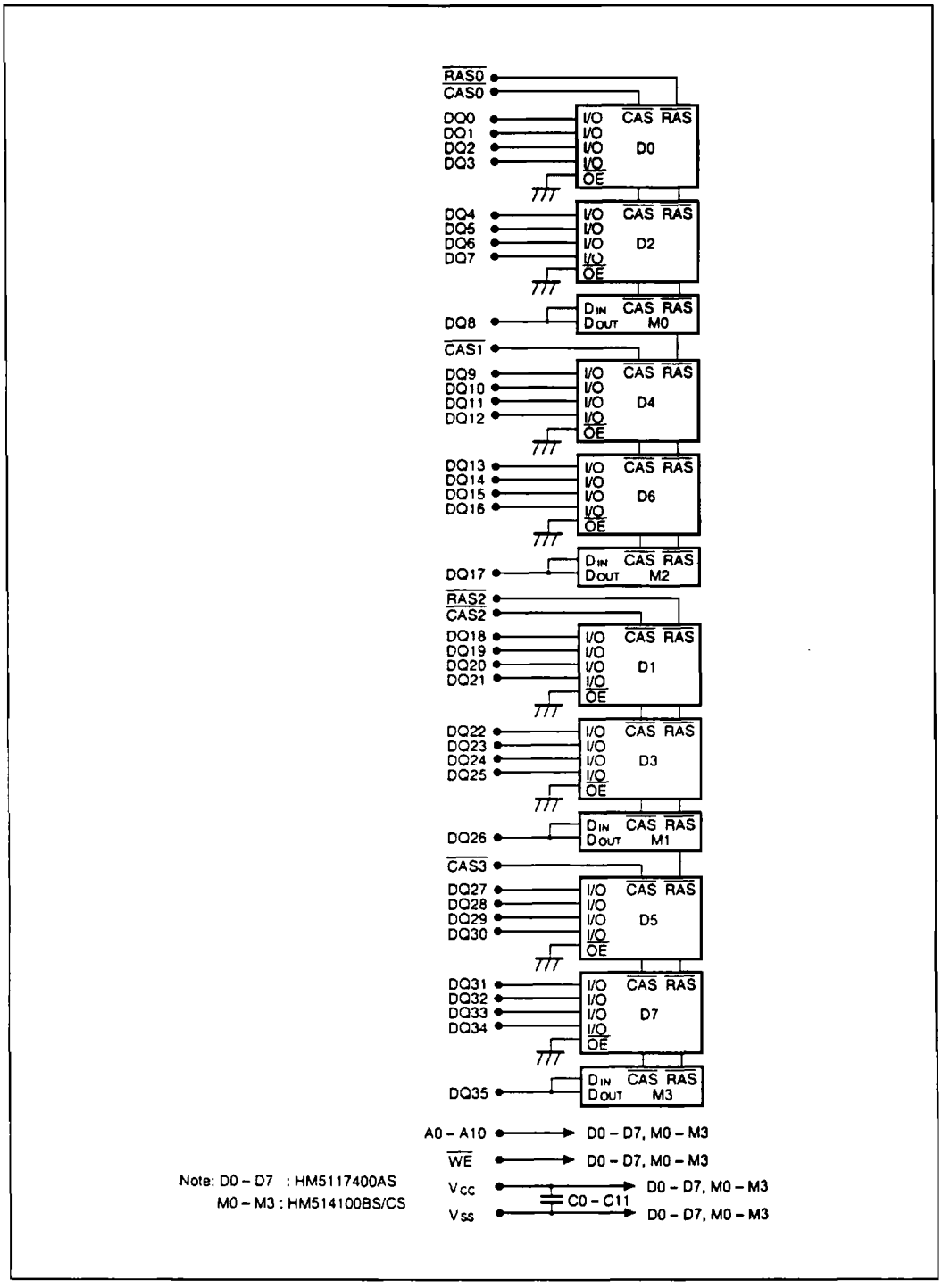
Pin Description

Pin name	Function
A0 – A10	Address input: A0 – A10 Row address: A0 – A10 Column address: A0 – A10 Refresh address: A0 – A10
DQ0 – DQ35	Data-in/data-out
$\overline{CAS0}$ – $\overline{CAS3}$	Column address strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row address strobe
$\overline{WE}$	Read/write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
PD1 – PD4	Presence detect pin
NC	No connection

Presence Detect Pin Arrangement

		HB56D436		
Pin No.	Pin name	60 ns	70 ns	80 ns
67	PD1	V_{SS}	V_{SS}	V_{SS}
68	PD2	NC	NC	NC
69	PD3	NC	V_{SS}	NC
70	PD4	NC	NC	V_{SS}

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	12	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5 %, V_{SS} = 0 V)

		HB56D436BR/SBR								
		60 ns		70 ns		80 ns				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test condition	Note
Operating current	I_{CC1}	—	1320	—	1200	—	1080	mA	t_{RC} = min	1, 2
Stanby current	I_{CC2}	—	24	—	24	—	24	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	12	—	12	—	12	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} –0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	1320	—	1200	—	1080	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	60	—	60	—	60	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	1320	—	1200	—	1080	mA	t_{RC} = min	
Page mode current	I_{CC7}	—	1080	—	960	—	880	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current Dout = disable	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (Address)	C_{I1}	—	88	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	104	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	57	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	36	pF	1
Output capacitance (DQ0 – 7, 9 – 16, 18 – 25, 27 – 34)	$C_{I/O1}$	—	17	pF	1, 2
Output capacitance (DQ8, 17, 26, 35)	$C_{I/O2}$	—	22	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) *1, *2

Read, Write and Refresh Cycle (Common parameters)

		HB56D436BR/SBR							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Note
Random read or write cycle time	t_{RC}	110	—	130	—	150	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	20	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	4
$\overline{RAS}$ hold time	t_{RSH}	15	—	20	—	20	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	5
Refresh period	t_{REF}	—	32	—	32	—	32	ms	17

Read Cycle

		HB56D436BR/SBR							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Note
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	ns	6, 7, 16
Access time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	ns	7, 8, 15, 16
Access time from address	t_{AA}	—	30	—	35	—	40	ns	7, 9, 15, 16
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	10
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	10
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Output buffer turn-off time	t_{OFF}	0	15	0	20	0	20	ns	11

Write Cycle

		HB56D436BR/SBR							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Note
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	12
Write command hold time	t_{WCH}	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	13
Data-in hold time	t_{DH}	15	—	15	—	15	—	ns	13

Refresh Cycle

		HB56D436BR/SBR							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Note
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	20	—	20	—	20	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	10	—	10	—	10	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

		HB56D436BR/SBR							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Note
Fast page mode cycle time	t_{PC}	40	—	45	—	50	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	14
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	35	—	40	—	45	ns	7, 15, 16
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	—	40	—	45	—	ns	

Test Mode Cycle

		HB56D436BR/SBR							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Note
Test mode $\overline{WE}$ setup time	t_{WTS}	0	—	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	t_{WTH}	10	—	10	—	10	—	ns	

Counter Test Cycle

		HB56D436BR/SBR							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Note
$\overline{CAS}$ precharge time in counter test cycle	t_{CPT}	40	—	40	—	40	—	ns	

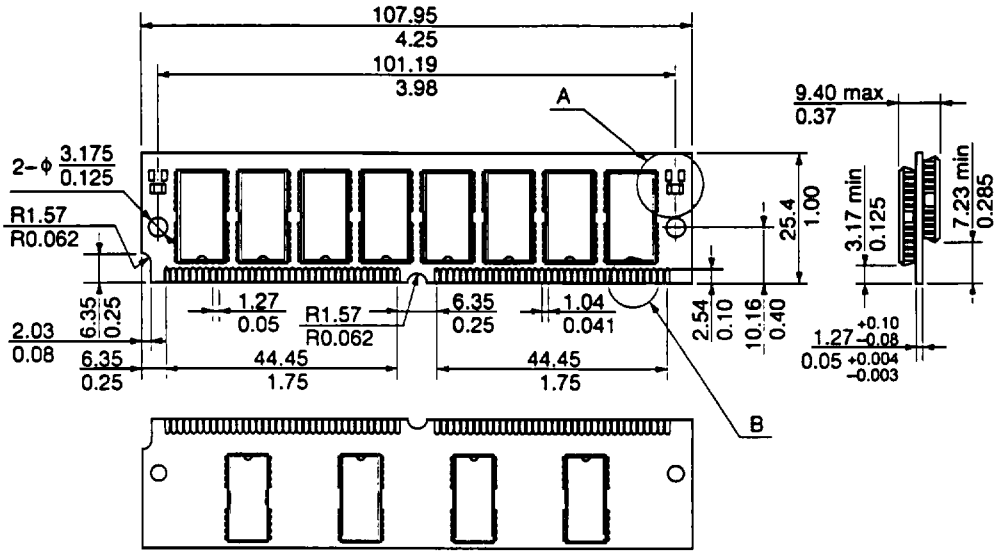
Notes: 1. AC measurements assume t_T = 5 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
11. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
12. Early write cycle only. ($t_{WCS} \geq t_{WCS}$ (min.))
13. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles.
14. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
15. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
16. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{CPA} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
17. t_{REF} is determined by 2,048 refresh cycles.

Timing Waveform

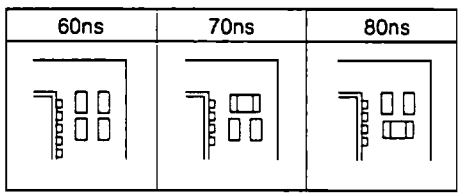
- Refer to the HM5117400A data sheet.
- The HB56D436 writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)).
- Delayed write cycle is not available.

Physical Outline

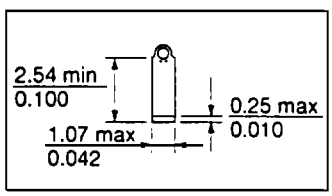
Unit: mm/inch



Detail A



Detail B



Note: The plating of the contact finger is gold.