# NFC ISO15693 SENSOR TRANSPONDER

## FEATURES

- ISO/IEC 15693, ISO/IEC 18000-3 (Mode 1) Compliant RF Interface
- Power Supply System With Either Battery or 13.56-MHz H-Field Supply
- Full-Differential First-Order Sigma-Delta (ΣΔ) Modulator
- Internal Temperature Sensor
- Resistive Sensor Bias Interface
- CRC16-Bit Generator
- MSP430 Mixed Signal Microcontroller
  - 2-kB FRAM
  - 4-kB SRAM
  - 8-kB ROM
  - Low Supply Voltage Range: 1.45 V to 1.65 V
  - Low Power Consumption
    - Active Mode (AM): 260 µA/MHz (1.5 V)
    - Standby Mode (LPM3, WDT_A Mode): 15 µA
    - Off Mode (LPM4): 9 µA
  - Wake-Up From LPM3 in Less Than TBD µs
  - 16-Bit RISC Architecture
  - Up to 4-MHz System Clock
  - Compact Clock System
    - 4-MHz High-Frequency Clock
    - 256-kHz Internal Low-Frequency Clock Source (Adjustable)
    - External Clock Input
  - 16-Bit Timer_A With Three Capture/Compare Registers
  - LV Port Logic
    - $V_{OL}$ Lower Than 0.15 V at 400 µA
    - $V_{OH}$ Higher Than $V_{DDB}$ – 0.15 at 400 µA
    - Timer0 PWM Signal Available on All Ports
  - eUSCI_B Module Supports 4-Wire SPI and $I^2C$
  - 32-Bit Watchdog Timer (WDT_A)
  - ROM Development Mode (Map ROM Addresses to SRAM to Enable Firmware Development)
  - Full Four-Wire JTAG Debug Interface
- For Complete Module Descriptions, See the *RF430xxx15xH Family User's Guide* (SLAU419)

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## DESCRIPTION

The Texas Instruments RF430FRL15xH is a 13.56-MHz transponder chip with a programmable 16-bit MSP430 low-power microcontroller. It features embedded universal FRAM nonvolatile memory for storage of program code or user data suc as calibration and measurement data. The RF430FRL15xH supports communication, parameter setting, and configuration via the ISO/IEC 15693, ISO18000-3 compliant RFID interface and the SPI or $I^2C$ Interface. Sensor measurements are supported by the internal temperature sensor and the on-board slow-acquisition 14-bit sigma-delta analog-to-digital converter. Two configurable operational amplifiers allow for connection of external analog sensors.

Optimized for operation in fully passive (battery-less) or single-cell battery-powered (semi-active) mode to achieve extended battery life in portable and wireless sensing applications. FRAM is a new nonvolatile memory that combines the speed, flexibility, and endurance of SRAM with the stability and reliability of flash, all at lower total power consumption.

**Table 1. Family Members**

| Device | FRAM (kB) | SRAM (kB) | Timer | 13.56 MHz ISO15693 Front End | eUSCI_B | SD14 |
|---|---|---|---|---|---|---|
| RF430FRL151H | 2 | 1 | Yes | Yes | Yes | Yes |
| RF430FRL152H | 2 | 4 | Yes | Yes | Yes | Yes |
| RF430FRL153H | 2 | 4 | Yes | Yes | No | Yes |
| RF430FRL154H | 2 | 4 | Yes | Yes | Yes | No |

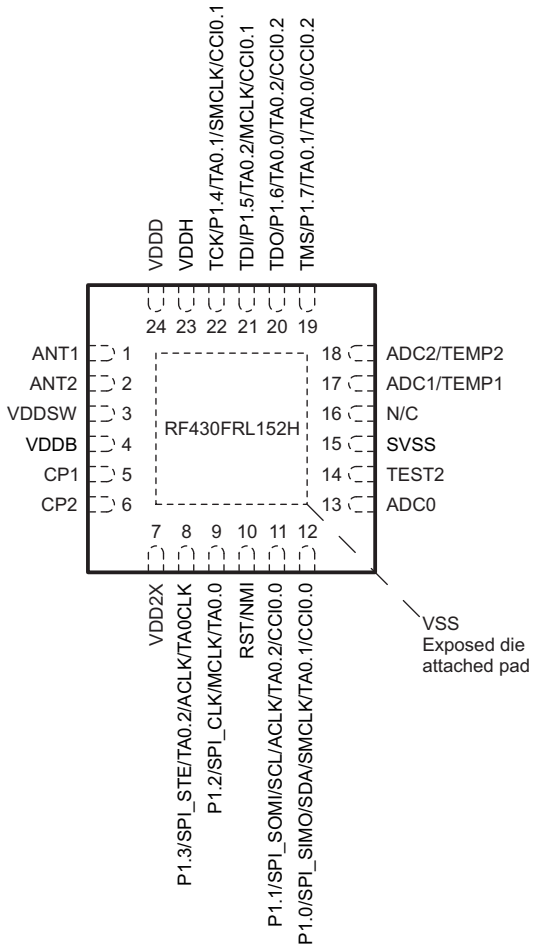
**Table 2. Ordering Information(1)**

| $T_A$ | PACKAGED DEVICES(2) PLASTIC 24-PIN QFN (RGE) |
|---|---|
| 0°C to 70°C | RF430FRL151HCRGER<br>RF430FRL152HCRGER<br>RF430FRL153HCRGER<br>RF430FRL154HCRGER |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.

## TERMINAL ASSIGNMENTS

**RGE PACKAGE**
**(TOP VIEW)**

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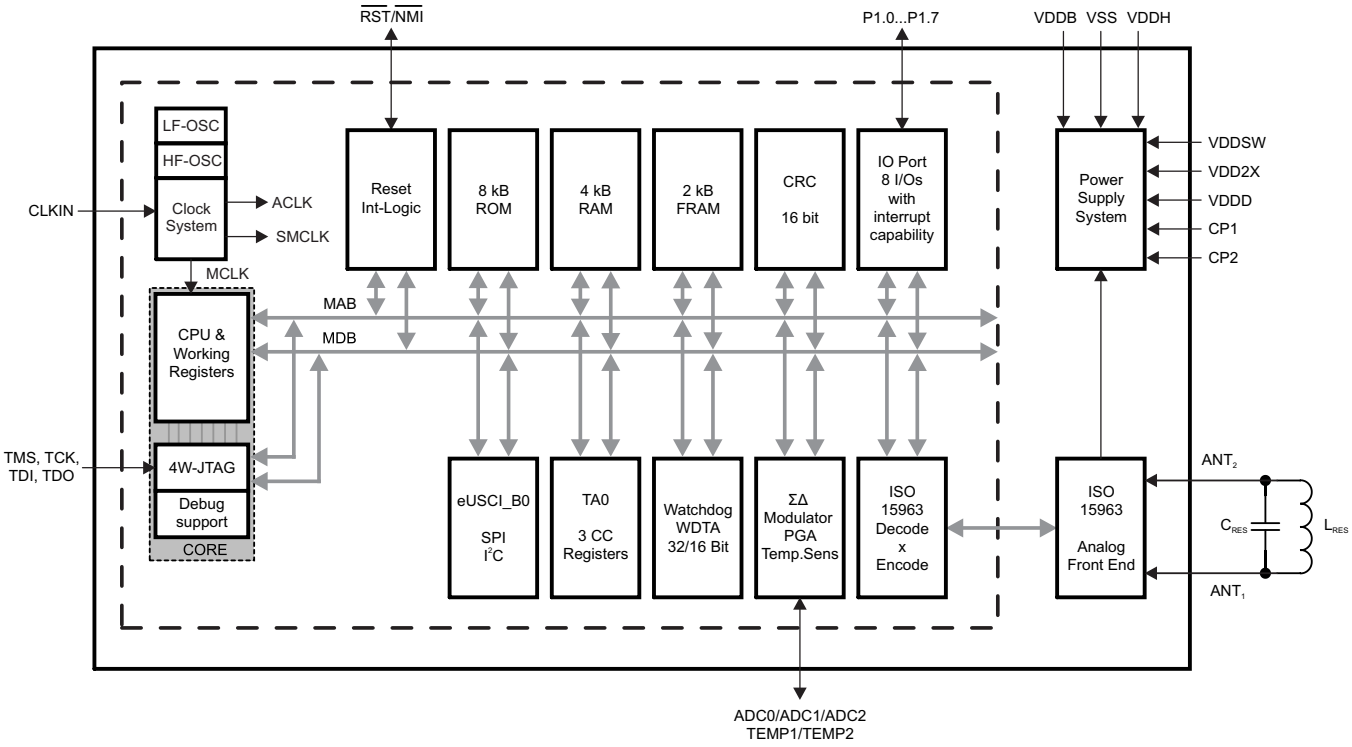
## Functional Block Diagram




## Table 3. Terminal Functions

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| ANT1 | 1 | I | Antenna input 1 |
| ANT2 | 2 | I | Antenna input 2 |
| $V_{DDSW}$ | 3 | | Selected supply voltage |
| $V_{DDB}$ | 4 | | Battery supply voltage |
| CP1 | 5 | | Charge pump flying cap terminal 1 |
| CP2 | 6 | | Charge pump flying cap terminal 2 |
| $V_{DD2X}$ | 7 | | Voltage doubler output |
| P1.3<br>SPI_STE<br>TA0.2<br>ACLK<br>TA0CLK | 8 | I/O | General-purpose digital I/O<br>SPI slave transmit enable<br>Timer_A TA0 OUT2 output<br>ACLK output (divided by 1, 2, 4, 8, 16, or 32)<br>Timer_A TA0 clock signal TA0CLK input |
| P1.2<br>SPI_CLK<br>MCLK<br>TA0.0 | 9 | I/O | General-purpose digital I/O<br>SPI clock<br>MCLK output<br>Timer_A TA0 OUT0 output |
| RST/NMI | 10 | I | Reset input active low<br>Non-maskable interrupt input |

(1) I = input, O = output

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**Table 3. Terminal Functions (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| P1.1<br>SPI_SOMI<br>SCL<br>ACLK<br>TA0.2<br>CCI0.0 | 11 | I/O | General-purpose digital I/O<br>SPI slave out master in<br>I2C clock<br>ACLK output (divided by 1, 2, 4, or 8 )<br>Timer_A TA0 OUT2 output<br>Timer_A TA0 CCR0 capture: CCI0B input, compare |
| P1.0<br>SPI_SIMO<br>SDA<br>SMCLK<br>TA0.1<br>CCI0.0 | 12 | I/O | General-purpose digital I/O<br>SPI slave in master out<br>I2C data<br>SMCLK output<br>Timer0_A3 OUT1 output<br>Timer_A TA0 CCR0 capture: CCI0A input, compare |
| ADC0 | 13 | I | ADC input pin 0 |
| TEST | 14 | | Test Pin |
| SVSS | 15 | | Sensor reference potential |
| NC | 16 | | N/C |
| ADC1 / TEMP1 | 17 | | ADC input pin 1 / Resistive bias pin 1 |
| ADC2 / TEMP2 | 18 | | ADC input pin 2 / Resistive bias pin 2 |
| TMS<br>P1.7<br>TA0.1<br>TA0.0<br>CCI0.2 | 19 | I/O | JTAG test mode select<br>General-purpose digital I/O<br>Timer_A TA0 OUT1 output<br>Timer_A TA0 OUT0 output<br>Timer_A TA0 CCR2 capture: CCI2B input, compare |
| TDO<br>P1.6<br>TA0.0<br>TA0.2<br>CCI0.2 | 20 | I/O | JTAG test data output<br>General-purpose digital I/O<br>Timer_A TA0 OUT0 output<br>Timer_A TA0 OUT2 output<br>Timer_A TA0 CCR2 capture: CCI2A input, compare |
| TDI<br>P1.5<br>TA0.2<br>MCLK<br>CCI0.1 | 21 | I/O | JTAG test data input<br>General-purpose digital I/O<br>Timer_A TA0 OUT2 output<br>MCLK output<br>Timer_A TA0 CCR1 capture: CCI1B input, compare |
| TCK<br>P1.4<br>TA0.1<br>SMCLK<br>CCI0.1<br>CLKIN | 22 | I/O | JTAG test clock<br>General-purpose digital I/O<br>Timer_A TA0 OUT1 output<br>SMCLK output<br>Timer_A TA0 CCR1 capture: CCI1A input, compare<br>External clock input pin |
| $V_{DDH}$ | 23 | | Rectified voltage from RF-AFE |
| $V_{DDD}$ | 24 | | Digital supply voltage |
| $V_{SS}$ | | | Ground reference, bonded to exposed pad(2) |

(2) VSS combines both digital ground ($DV_{SS}$) and analog ground ($AV_{SS}$)

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