FEATURES

- 168-pin industry standard 8-byte dual-in-line memory module
- JEDEC compliant: Preliminary Ballot 744.1
  : No. 95 MO-161
- High performance, CMOS
- Single 5.0V ± 10% power supply
- TTL-compatible inputs and outputs
- Fast Page Mode access cycle
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$, HIDDEN
- Refresh: 2048 refresh cycles every 32 ms
- Dimensions: 5.25" (length) x 1.00" (height) x 0.354" (max thickness)

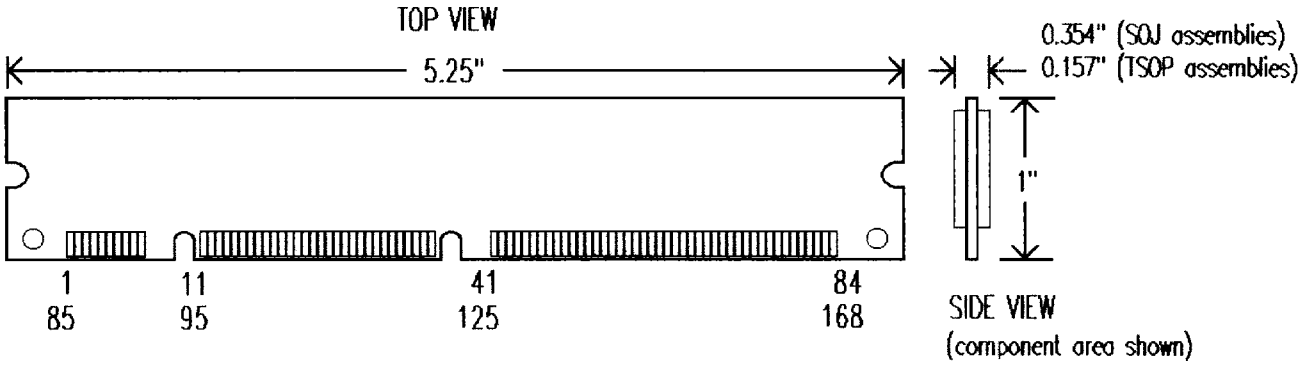
PERFORMANCE RANGE

SYMBOL	PARAMETER	Rating	
		60 ns	70 ns
t_{RAC}	$\overline{\text{RAS}}$ Access Time	60 ns (max)	70 ns (max)
t_{CAC}	$\overline{\text{CAS}}$ Access Time	15 ns (max)	20 ns (max)
t_{AA}	Access Time from Column Address	30 ns (max)	35 ns (max)
t_{RC}	Random Read or Write Cycle Time	110 ns (min)	130 ns (min)
t_{PC}	Fast Page Mode Cycle Time	40 ns (min)	45 ns (min)

ORDERING INFORMATION

DESCRIPTION	PART NUMBER	ENGINEERING DESCRIPTOR
4M x 64, 60 ns, Gold Tabs, SOJ	20455C	CL001N04640B0BJ-60
4M x 64, 70 ns, Gold Tabs, SOJ	20456C	CL001N04640B0BJ-70
4M x 64, 60 ns, Gold Tabs, TSOP	20457C	CL001N04640B0BT-60
4M x 64, 70 ns, Gold Tabs, TSOP	20458C	CL001N04640B0BT-70

CARD OUTLINE



GENERAL DESCRIPTION

The 4M x 64 DIMM uses dynamic RAM devices and is designed for use as a general-purpose 8-byte wide memory assembly with 8 data bits per byte. The DIMM is populated with sixteen 4M x 4 DRAMs.

The DIMMs have a two wire serial port (I^2C interface) via a 256 byte serial EEPROM. It is used to read DIMM attributes, such as DIMM density, addressing, performance, and other features.

During Read or Write Cycles, each byte may be uniquely addressed via 22 address bits, with the first 11 bits (A0~A10) latched on $\overline{RAS}$ and the latter 11 bits (A0~A10) latched on $\overline{CAS}$. READ or WRITE cycles are selected with the $\overline{WE}$ input, with a logic low indicating a WRITE cycle and a logic HIGH indicating a READ cycle. During a WRITE cycle, data-in is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last.

FAST PAGE MODE operation allows for faster READs or WRITEs within a row-address-defined page boundary. A FAST PAGE MODE cycle is initiated with $\overline{RAS}$ followed by $\overline{CAS}$, then strobing $\overline{CAS}$ to latch different column addresses while holding $\overline{RAS}$ LOW.

Returning $\overline{RAS}$ and $\overline{CAS}$ high terminates a memory cycle and returns the DRAMs to a reduced-current STANDBY state.

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$-ONLY,CBR, or HIDDEN) so that all 2048 combinations of $\overline{RAS}$ addresses (A0~A10) are executed at least every 32 ms. The CBR refresh and HIDDEN refresh cycles will invoke the on-chip refresh address counters for automatic $\overline{RAS}$ addressing.

PIN DESCRIPTION

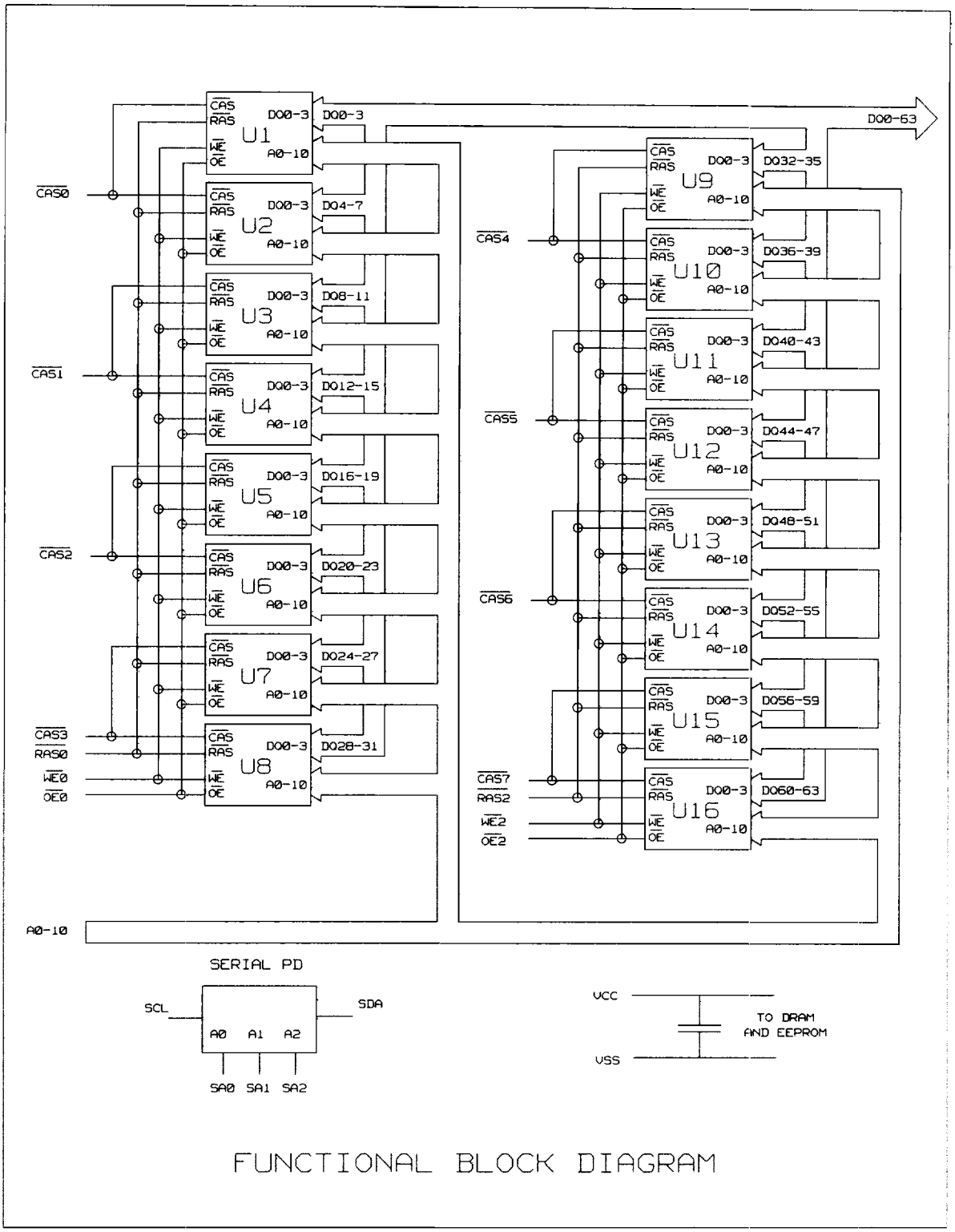
$\overline{RAS0}$,$\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$~$\overline{CAS7}$	Column Address Strobe
$\overline{WE0}$,$\overline{WE2}$	Write Enable
$\overline{OE0}$,$\overline{OE2}$	Output Enable
A0~A10	Address Input
DQ0~DQ63	Data Input/Output
VCC	Power (+5.0V)
VSS	Ground
SDA	Serial Data
SCL	Serial Clock
SA0~SA2	Serial Address
NC	No Connect
DU	Don't Use

SERIAL PD ASSIGNMENTS

Byte #	Description	Serial EEPROM Entry Value	Serial EEPROM Data								
			Binary Bit								Hex
			7	6	5	4	3	2	1	0	
0	Number of Serial EEPROM Bytes	128	1	0	0	0	0	0	0	0	80
1	Total # Bytes in Serial EEPROM	256	0	0	0	0	1	0	0	0	08
2	Memory Type	FPM	0	0	0	0	0	0	0	1	01
3	# of Row Addresse Lines	11	0	0	0	0	1	0	1	1	0B
4	# of Column Address Lines	11	0	0	0	0	1	0	1	1	0B
5	# of DIMM Banks	1	0	0	0	0	0	0	0	1	01
6	Module Data Width (Low Byte)	64	0	1	0	0	0	0	0	0	40
7	Module Data Width (High Byte)	0	0	0	0	0	0	0	0	0	00
8	Module Interface Levels	TTL/5V	0	0	0	0	0	0	0	0	00
9	RAS Access	60ns	0	0	1	1	1	1	0	0	3C
		70ns	0	1	0	0	0	1	1	0	46
10	CAS Access	15ns	0	0	0	0	1	1	1	1	0F
		20ns	0	0	0	1	0	1	0	0	14
11	DIMM Configuration Type	None	0	0	0	0	0	0	0	0	00
12	Refresh Rate/Type	15.625us	0	0	0	0	0	0	0	0	00
13	DRAM Data Width	4	0	0	0	0	0	1	0	0	04
14	Error Checking Data Width	0	0	0	0	0	0	0	0	0	00

PIN CONFIGURATION

Pin #	Front Side	Pin #	Front Side	Pin #	Back Side	Pin #	Back Side
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	$\overline{OE2}$	86	DQ32	128	DU
3	DQ1	45	$\overline{RAS2}$	87	DQ33	129	NC
4	DQ2	46	$\overline{CAS2}$	88	DQ34	130	$\overline{CAS6}$
5	DQ3	47	$\overline{CAS3}$	89	DQ35	131	$\overline{CAS7}$
6	VCC	48	$\overline{WE2}$	90	VCC	132	DU
7	DQ4	49	VCC	91	DQ36	133	VCC
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VCC	101	DQ45	143	VCC
18	VCC	60	DQ20	102	VCC	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	DU	104	DQ47	146	DU
21	NC	63	NC	105	NC	147	NC
22	NC	64	VSS	106	NC	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VCC	68	VSS	110	VCC	152	VSS
27	$\overline{WE0}$	69	DQ24	111	DU	153	DQ56
28	$\overline{CAS0}$	70	DQ25	112	$\overline{CAS4}$	154	DQ57
29	$\overline{CAS1}$	71	DQ26	113	$\overline{CAS5}$	155	DQ58
30	$\overline{RAS0}$	72	DQ27	114	NC	156	DQ59
31	$\overline{OE0}$	73	VCC	115	DU	157	VCC
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	NC	164	NC
39	NC	81	NC	123	NC	165	SA0
40	VCC	82	SDA	124	VCC	166	SA1
41	VCC	83	SCL	125	DU	167	SA2
42	DU	84	VCC	126	DU	168	VCC



FUNCTIONAL BLOCK DIAGRAM

TRUTH TABLE

FUNCTION	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ROW ADDR	COL ADDR	DQx
Standby	H	X	X	X	X	X	Hi-Z
Read	L	L	H	L	ROW	COL	Valid D_{OUT}
Early-Write	L	L	L	X	ROW	COL	Valid D_{IN}
RMW	L	L	H→L	L→H	ROW	COL	Valid D_{OUT}
Fast Page Mode-Read 1st Cycle	L	H→L	H	L	ROW	COL	Valid D_{OUT}
Subsequent Cycles	L	H→L	H	L	N/A	COL	Valid D_{OUT}
Fast Page Mode-Write 1st Cycle	L	H→L	L	X	ROW	COL	Valid D_{IN}
Subsequent Cycles	L	H→L	L	X	N/A	COL	Valid D_{OUT}
Fast Page Mode-RMW 1st Cycle	L	H→L	H→L	H→L	ROW	COL	Valid D_{OUT}
Subsequent Cycles	L	H→L	H→L	H→L	N/A	COL	Valid D_{OUT}
$\overline{RAS}$-Only Refresh	L	H	X	X	ROW	N/A	Hi-Z
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	Hi-Z

X:"H" or "L" DIN:Data In DOUT:Data Out Hi-Z:High Impedance N/A:Not Applicable

ABSOLUTE MAXIMUM RATINGS (Note 1,22)

SYMBOL	PARAMETER	RATING	UNITS	NOTES
V_{CC}	Power Supply Voltage	-1.0 to 7.0	V	2
V_{IN}	Voltage on any Pin Relative to V_{SS}	-1.0 to 7.0	V	2
V_{OUT}		-1.0 to 7.0	V	2
T_{opr}	Operating Temperature	0 to 70	°C	
T_{stg}	Storage Temperature	-55 to 125	°C	
P_D	Power Dissipation	16	W	17,31
I_{OS}	Short Circuit Output Current	50	mA	17

RECOMMENDED OPERATING CONDITIONS (T_A= 0 to 70 °C) (Note 2)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Ground	0	0	0	V	
V_{IH}	Input High Voltage	2.4		min (6.5 , Vcc + 1.0)	V	22
V_{IL}	Input Low Voltage	-1		0.8	V	22

T_A: Ambient temperature

CAPACITANCE (f = 1 MHz; T_A = 25 °C) (Note 22)

SYMBOL	PARAMETER	MAX.	UNITS	NOTES
C_{I1}	Input Capacitance (A0-A10)	96	pF	
C_{I2}	Input Capacitance ($\overline{RAS0}$,$\overline{RAS2}$)	56	pF	
C_{I3}	Input Capacitance ($\overline{CAS0}$~$\overline{CAS7}$)	14	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	56	pF	
C_{I5}	Input Capacitance ($\overline{OE}$)	56	pF	
C_{O1}	Output Capacitance (Data In/Out)	7	pF	

T_A: Ambient temperature

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) (Note 18,22)

SYMBOL	PARAMETER		SPEED	MIN	MAX	NOTES
I_{CC1}	OPERATING CURRENT: Average Power Supply Operating Current ($\overline{RAS}$,$\overline{CAS}$, Address Cycling@t_{RC} = $t_{RC(min)}$, V_{CC} = $V_{CC\ (max)}$)(mA)		60 ns	-	1923	3,4,5,6, 16
			70 ns	-	1683	
I_{CC2}	STANDBY CURRENT (TTL): Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=Vcc, Data out is disabled (Hi-Z), all other inputs =Vcc, V_{CC} =$V_{CC\ (max)}$) (mA)		Don't Care	-	32	
I_{CC3}	$\overline{RAS}$-ONLY REFRESH CURRENT: Average Power Supply Current, $\overline{RAS}$-Only Mode ($\overline{RAS}$, Address Cycling, $\overline{CAS}$=V_{IH}@t_{RC}=$t_{RC(min)}$,V_{CC}=$V_{CC(max)}$) (mA)		60 ns	-	1923	3,4,5,6,16, 31
			70 ns	-	1683	
I_{CC4}	FAST PAGE MODE CURRENT: Average Power Supply Current, FPM ($\overline{RAS}$=V_{IL},$\overline{CAS}$, Address Cycling@ t_{PC}=$t_{PC(min)}$,V_{CC}=$V_{CC(max)}$) (mA)		60 ns	-	1283	3,4,5,7,16
			70 ns	-	1123	
I_{CC5}	STANDBY CURRENT (CMOS): Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V, Data Out is disabled (Hi-Z),V_{CC} = $V_{CC(max)}$) (mA)		Don't Care	-	16	
I_{CC6}	$\overline{CAS}$-BEFORE-$\overline{RAS}$, REFRESH CURRENT: Average Power Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Mode ($\overline{RAS}$,$\overline{CAS}$ Cycling@t_{RC}=$t_{RC(min)}$, V_{CC} = $V_{CC(max)}$)(mA)		60 ns	-	1763	3,4,5,6,16, 31
			70 ns	-	1603	
I_{LI}	INPUT LEAKAGE CURRENT: Input Leakage Current, any input (0≤V_{IN}≤V_{cc}, all other pins not under test=0V, $V_{CC=}$ $V_{CC(max)}$) (µA)	**A0~A10**		-160	160	
		$\overline{RAS0}$,$\overline{RAS2}$		-80	80	
		$\overline{CAS0}$~$\overline{CAS7}$		-20	20	
		$\overline{WE}$		-80	80	
		$\overline{OE}$		-80	80	
I_{LO}	OUTPUT LEAKAGE CURRENT: (Data Out is disabled (Hi-Z), 0≤V_{OUT}≤V_{CC})(µA)			-10	10	
V_{OH}	OUTPUT HIGH LEVEL: Output "H" Level Voltage (I_{OUT}=-5mA) (V)			2.4	-	2
V_{OL}	OUTPUT LOW LEVEL: Output "L" Level Voltage (I_{OUT}=+4.2mA) (V)			-	0.4	2

AC CHARACTERISTICS

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES (COMMON PARAMETERS)

(Recommended operating conditions unless otherwise noted.) (Note 8, 18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Random READ or WRITE Cycle Time (ns)	110	-	130	-	
t_{RP}	$\overline{RAS}$ Precharge Time (ns)	40	-	50	-	
t_{CP}	$\overline{CAS}$ Precharge Time (ns)	10	-	10	-	
t_{RAS}	$\overline{RAS}$ Pulse Width (ns)	60	10000	70	10000	23
t_{CAS}	$\overline{CAS}$ Pulse Width (ns)	15	10000	20	10000	23
t_{ASR}	Row Address Setup Time (ns)	0	-	0	-	22
t_{RAH}	Row Address Hold Time (ns)	10	-	10	-	
t_{ASC}	Column Address Setup Time (ns)	0	-	0	-	22
t_{CAH}	Column Address Hold Time (ns)	12	-	15	-	22
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time (ns)	20	45	20	50	10
t_{RAD}	$\overline{RAS}$ to Col. Address Delay Time (ns)	15	30	15	35	15
t_{RSH}	$\overline{RAS}$ Hold Time (ns)	15	-	20	-	22
t_{CSH}	$\overline{CAS}$ Hold Time (ns)	60	-	70	-	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time (ns)	5	-	5	-	22
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time (ns)	15	-	20	-	22,27
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN} (ns)	0	-	0	-	22,28
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ hold Time (ns)	5	-	5	-	22
t_T	Transition Time (Rise and Fall) (ns)	3	30	3	30	22
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$ (ns)	-	-	-	-	

READ CYCLES (Note 8, 18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{RAC}	Access Time from $\overline{RAS}$ (ns)	-	60	-	70	9,10,15,30
t_{CAC}	Access Time from $\overline{CAS}$ (ns)	-	15	-	20	9,10,30
t_{AA}	Access Time from Address (ns)	-	30	-	35	9,15,30
t_{OEA}	Access Time from $\overline{OE}$ (ns)	-	15	-	20	9
t_{RCS}	Read Command Setup Time (ns)	0	-	0	-	22
t_{RCH}	Read Command Hold Time to $\overline{CAS}$ (ns)	0	-	0	-	14,22
t_{RRH}	Read Command Hold Time to $\overline{RAS}$ (ns)	5	-	5	-	14,22
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time(ns)	30	-	35	-	22
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z (ns)	0	-	0	-	9,22
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$ (ns)	0	15	0	20	12,24
t_{DZC}	Data to $\overline{CAS}$ Low Delay Time (ns)	0	-	0	-	28
t_{CDD}	$\overline{CAS}$ High to Data Delay Time (ns)	15	-	18	-	27
t_{OFF}	Output Buffer Turn-Off Delay (ns)	0	15	0	20	12,24

WRITE CYCLES (Note 8, 18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{WCS}	Write Command Set Up Time (ns)	0	-	0	-	13
t_{WCH}	Write Command Hold Time (ns)	10	-	15	-	
t_{WP}	Write Command Pulse Width (ns)	10	-	15	-	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time (ns)	15	-	20	-	22
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time (ns)	15	-	20	-	
t_{DS}	D_{IN} Setup Time (ns)	0	-	0	-	25
t_{DH}	D_{IN} Hold Time (ns)	10	-	15	-	22,25
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$ (ns)	-	-	-	-	
t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$ (ns)	-	-	-	-	

SERIAL READ AND WRITE CYCLES (Note 8, 19, 22)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES
f_{SCL}	SCL Clock Frequency		100	kHz	
T_I	Noise Suppression Time Constant at SCL, SDA inputs		100	ns	
t_{AAE}	SCL Low to SDA Data Out Valid	0.3	3.5	µs	
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		µs	
$t_{HD:STA}$	Start Condition Hold Time	4		µs	
t_{LOW}	Clock Low Period	4.7		µs	
t_{HIGH}	Clock High Period	4		µs	
$t_{SU:STA}$	Start Condition Setup Time	4.7		µs	
$t_{HD:DAT}$	Data in Hold Time	0		µs	
$t_{SU:DAT}$	Data in Setup Time	250		ns	
t_R	SDA and SCL Rise Time		1	µs	
t_F	SDA and SCL Fall Time		300	ns	
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs	
t_{DHE}	Data Out Hold Time	300		µs	
t_{WR}	Write Cycle Time		10	ms	

FAST PAGE MODE CYCLES (Note 8, 18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{PC}	Fast Page Mode Cycle Time (ns)	40	-	45	-	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width (ns)	60	100000	70	100000	22
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (ns)	35	-	40	-	22
t_{CPA}	Access Time from $\overline{CAS}$ Precharge (ns)	-	35	-	40	9,21,22,30
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time (ns)	85	-	100	-	
t_{CPW}	$\overline{WE}$ Delay Time From $\overline{CAS}$ Precharge (ns)	60	-	70	-	13

REFRESH CYCLE (Note 8, 18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle) (ns)	10	-	15	-	22
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle) (ns)	5	-	5	-	22
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle) (ns)	10	-	10	-	22
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle) (ns)	10	-	10	-	22
t_{REF}	Refresh Period (2048 cycles) (ms)	-	32	-	32	

READ-MODIFY-WRITE CYCLE (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{RWC}	Read-Modify-Write Cycle Time (ns)	160	-	185	-	22
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time (ns)	85	-	100	-	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time (ns)	40	-	50	-	13,22
t_{AWD}	Column Address to $\overline{WE}$ Delay Time (ns)	55	-	65	-	13,22
t_{OEH}	$\overline{OE}$ Hold Time After $\overline{WE}$ Low (ns)	15	-	20	-	

NOTES

1. Permanent damage to the device may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. All voltages referenced to V_{SS}.

3. I_{CC} is specified as an average current.

4. This parameter depends on output loading and/or cycle rates.

5. Specified values are obtained with the output open.

6. Address can be changed a maximum of once while $\overline{RAS}=V_{IL}$.

7. Address can be changed a maximum of once while $\overline{CAS}=V_{IH}$.

8. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition time (t_T) is measured between $V_{IH(min)}$ and $V_{IL(max)}$, and is assumed to be 5ns for all inputs. All input signals must transit between V_{IH} and V_{IL} (or V_{IL} and V_{IH}) without slope reversal.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. Operation within the $t_{RCD(max)}$ limit ensures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.

11. Assumes that $t_{RAD} \leq t_{RAD(max)}$.

12. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

13. This is a non-restrictive operating parameter. It is included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pins will remain high impedance (open circuit) for the duration of the cycle. If $t_{CWD(min)} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$, and $t_{CPW} \geq t_{CPW(min)}$ (for Fast Page Mode cycle only), then the cycle is a Read-Modify-Write cycle and the data output pins will hold the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out (at access time) is indeterminate.

14. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

15. Operation within the $t_{RAD(max)}$ limit ensures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled exclusively by t_{AA}.

16. Specified values are obtained with minimum cycle time.

17. Specified values are obtained with T_A=25°C.

18. An initial pause of 200µs is required after power-up followed by a minimum of eight initialization cycles (any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles with $\overline{WE}$ high) before proper device operation is assured. Also, any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles with $\overline{WE}$ high are required after prolonged periods (greater than t_{REF}) of $\overline{RAS}$ inactivity before proper device operation is assured.

19. Measured with a load equivalent to 50pF and 500 ohms.

20. Write cycle is applicable instead of read cycle. Timing requirements for $\overline{RAS}$,$\overline{CAS}$ and Address are the same for Hidden Refresh Write Cycle as that shown for Hidden Refresh Read Cycle. $\overline{WE}$, D_{IN} and D_{OUT} for Hidden Refresh Write Cycle are the same as for Write Cycle.

21. t_{CPA} is access time from $\overline{CAS}$ precharge (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, then t_{CPA} is longer than $t_{CPA(max)}$.

22. Calculated based on data supplied by the DRAM manufacturer(s).

23. Maximum value is calculated based on data supplied by the DRAM manufacturer(s).

24. Minimum value is calculated based on data supplied by the DRAM manufacturer(s).

25. This parameter is referenced to the $\overline{CAS}$ leading edge in Early Write cycles and to the $\overline{WE}$ leading edge in Read-Modify-Write cycles.

26. V_{IN} = 0 Volt.

27. Either t_{CDD} or t_{ODD} must be satisfied.

28. Either t_{DZC} or t_{DZO} must be satisfied.

29. $t_{RASP(MIN)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

30. The access time is limited by all four parameters t_{RAC}, t_{CAC}, t_{AA}, t_{CPA}.

31. This assumes all $\overline{RAS}$ (and all $\overline{CAS}$ for CBR refresh) are active.

For Timing Diagrams see **"FPM Timing Diagrams"** (Document No. **20432C**).

Available from fax-on-demand and Website: **http://www.celestica.com/memory/**

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