



# CML Semiconductor Products

PRODUCT INFORMATION

## FX013 HSC Tone Decoder for 'Pagers

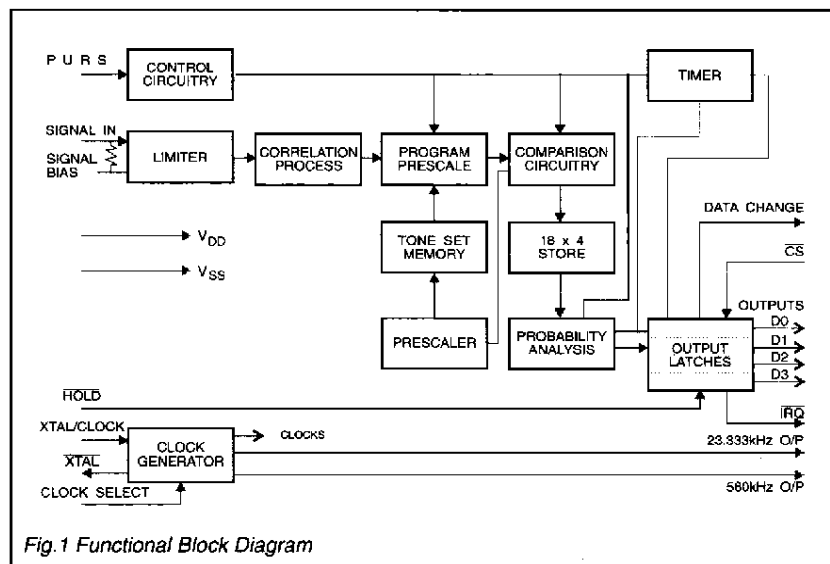
### Obsolete Product

### - For Information Only -

#### Features

- 'N'-Tone HSC Decoding
- EIA and CCIR Tonesets
- 4-Bit Parallel (HEX) Data Output
- $\mu$ Processor Interface
- Auxiliary 23.33kHz Clock Output
- Low-Power (2.5V @ 500 $\mu$ A<sub>MIN</sub>) Requirement

- Radiopaging, PMR Selcall and Remote Signalling Applications
- Selectable 560kHz or 4.48MHz Xtal/Clock Operation
- Automatic Power-Up Reset Facility
- 24-Pin/Lead Package Versions



# FX013

#### Brief Description

The FX013 is a very low-voltage continuous "N"-Tone EIA and CCIR HSC tone decoder which is ideal for tone-paging applications.

From an analogue signal input the FX013 will produce a representative 4-bit (HEX) parallel output word for either toneset. Hold, Data Change and Interrupt features combined with the 4-bit data output enable  $\mu$ Processor interface and control. Alternatively, the FX013 may be used in a simple passive system using the Data Change and Data Outputs

This device can be used with a customer specified  $\mu$ Processor or with a pre-programmed address decoder/display driver.

The FX013 has on-chip automatic Power-Up Reset circuitry, which with selected time-constant components ensures the correct start-up settings for most supply conditions, making this device ideal for installation within radiopaging units.

Operating at 2.5 volts with a minimum current requirement of 500 $\mu$ A, the FX013 is available in two toneset versions to decode either EIA (A) or CCIR (C) tones.

To cater for variations in design requirements the FX013 is produced in both 24-pin cerdip DIL and plastic quad packages.

## Pin Number

## Function

FX013J/LG	
3	<b>Signal In:</b> HSC input tones are a.c. coupled to this pin; dc bias of the internal high gain limiter is set up by an internal 3M $\Omega$ bias resistor connected between this pin and the Signal Bias pin. Neither pin should be loaded with any other circuitry.
5	<b>Signal Bias:</b> See Signal In.
7	<b>23.33kHz Clock Out:</b> A 23.333kHz buffered squarewave logic output directly derived from the oscillator frequency (nominally 560.0kHz). This pin may be used for auxiliary functions, e.g. external timing of received tone periods and for other '03 series devices.
8	<b>Xtal:</b> Output from on-chip Inverter.
9	<b>Xtal/Clock:</b> Input to on-chip inverter. May be used in conjunction with the Xtal O/P and a 560kHz ceramic resonator/trimming capacitor, or a 4.48MHz Xtal Circuit. May also be used with a buffered input from an externally derived 560kHz or 4.48MHz clock.
10	<b>560kHz Buffered O/P:</b> A buffered 560kHz signal is output from this pin.
11	<b>Clock Frequency Select:</b> Normally at logic "1" if a 560kHz resonator is being used. If held at logic "0," a divide by 8 function is switched in after the oscillator circuit to divide down the 4.48MHz frequency to 560kHz. This pin has an internal 1M $\Omega$ pullup resistor.
12	<b>V<sub>ss</sub>:</b> Negative Supply (GND).
13	<b>Hold I/P:</b> If taken to V <sub>ss</sub> and a tone is input, the resulting Data Change output latches to logic "1" and the Data lines output the code for the detected tone regardless of subsequent changes to the input tone, until Hold is returned to V <sub>DD</sub> . This facilitates interrupt/handshake routines for $\mu$ Processors when used in conjunction with the Data Change O/P. This pin has an internal 1M $\Omega$ pullup resistor.
14	<b>Power-Up Reset (P U R S):</b> To reset internal circuitry on power-up, a logic "1" is required at this pin for a duration of at least 1.0ms after clock is applied. For slow-rising supplies the time constant recommended by the components in Figure 2 should be increased accordingly.
15	<b>IRQ:</b> Interrupt Request. This output, is latched to logic "0" when a tone is detected and the CS pin is at V <sub>DD</sub> , i.e. chip disabled. This pin is reset to logic "1," enabling its for use in wire-ORing with similar outputs from other peripherals. This pin has internal 1k $\Omega$ pulldown and 100k $\Omega$ pullup resistors on-chip.
16	<b>CS:</b> Chip Select. When this pin is at V <sub>DD</sub> , the chip is disabled and the data outputs D0 - D3 and Data Change output go open circuit. When at V <sub>ss</sub> the chip is enabled and the IRQ output is reset to logic "1."
17	<b>Data Change:</b> A 1.0 ms pulse is generated at this pin upon detection of a valid tone and new data is presented to the D0 - D3 outputs. The signal from this pin can be latched at a logic "1" after detection of a tone (see Hold input). This output is tri-state.
19	<b>D3 Data Outputs:</b> A 4-bit word, that represents the HEX value of the decoded tone frequency, is output from these pins after a successful decode. These outputs are tri-state. See Table 1.
20	
22	
23	
24	<b>V<sub>DD</sub>:</b> Positive Supply
1, 2, 4, 6, 18, 21	Not connected. Leave open-circuit.

## Application Information

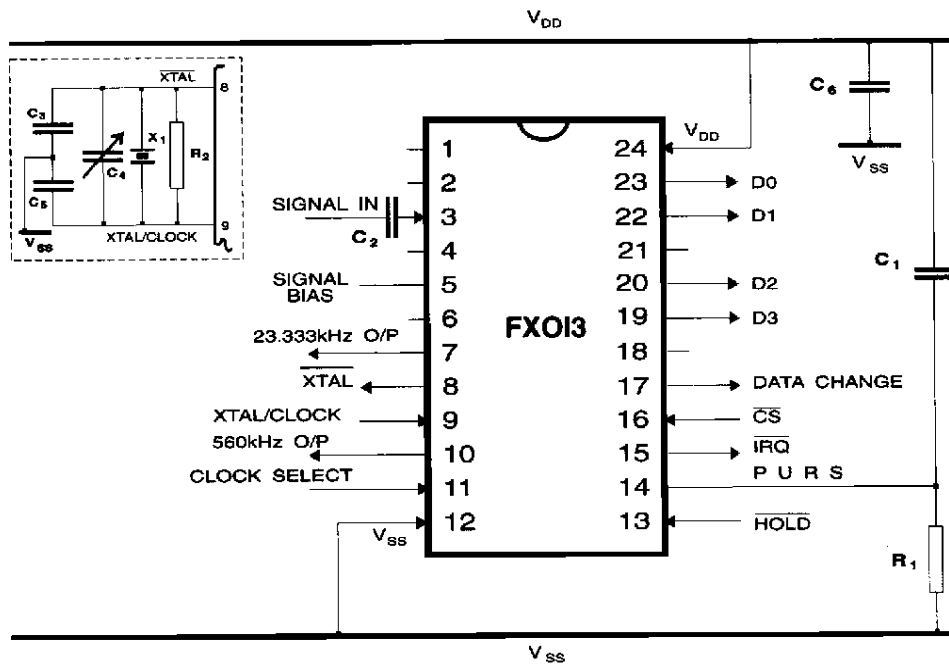


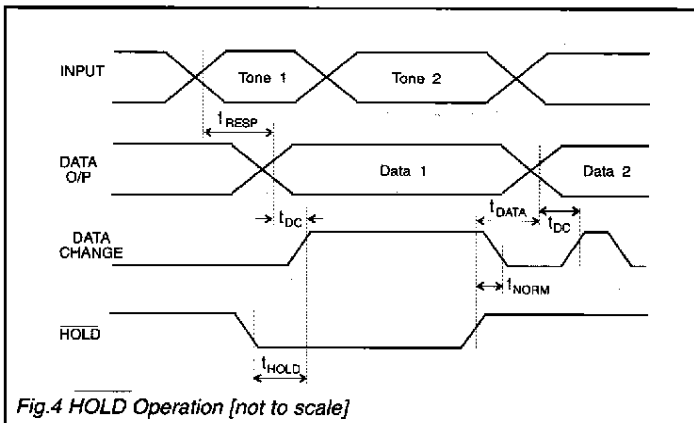
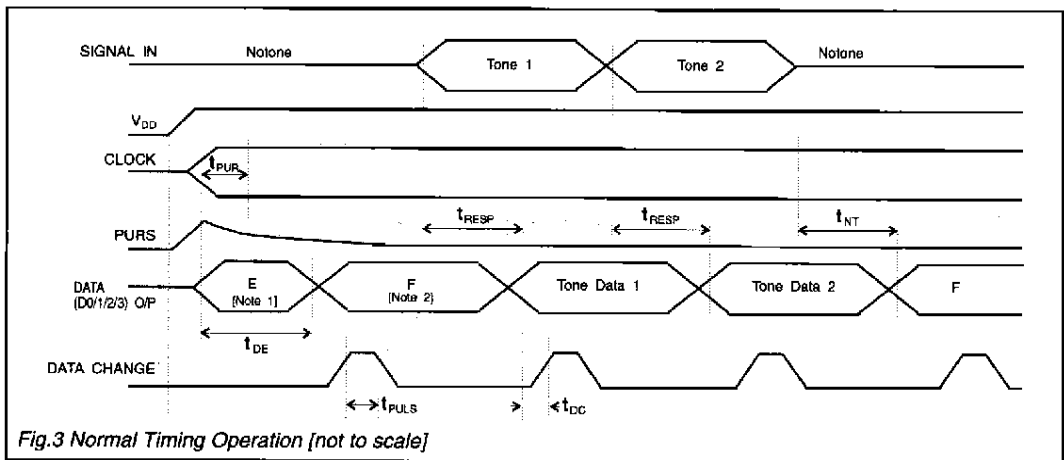
Fig. 2 Recommended External Components

Component	Value
$R_1$	1M $\Omega$
$R_2$	1M $\Omega$
$C_1$	0.01 $\mu$ F
$C_2$	0.001 $\mu$ F
$C_3$	47.0pF
$C_4$	5 - 65pF
$C_5$	47.0pF
$C_6$	1.0 $\mu$ F
$X_1$	560kHz

Tolerance:  $R = \pm 10\%$   $C = \pm 20\%$

Input Tone Frequencies (Hz)		Binary Coded Output				Quadradecimal Data Character
FX013 A (EIA)	FX013 C (CCIR)	D3	D2	D1	D0	
600	1981	0	0	0	0	0
741	1124	0	0	0	1	1
882	1197	0	0	1	0	2
1023	1275	0	0	1	1	3
1164	1358	0	1	0	0	4
1305	1446	0	1	0	1	5
1446	1540	0	1	1	0	6
1587	1640	0	1	1	1	7
1728	1747	1	0	0	0	8
1869	1860	1	0	0	1	9
2151	2400	1	0	1	0	A
2433	930	1	0	1	1	B
2010	2247	1	1	0	0	C
2292	991	1	1	0	1	D
459	2110	1	1	1	0	E
NOTONE	NOTONE	1	1	1	1	F

Table 1 Decode Frequency Tonesets

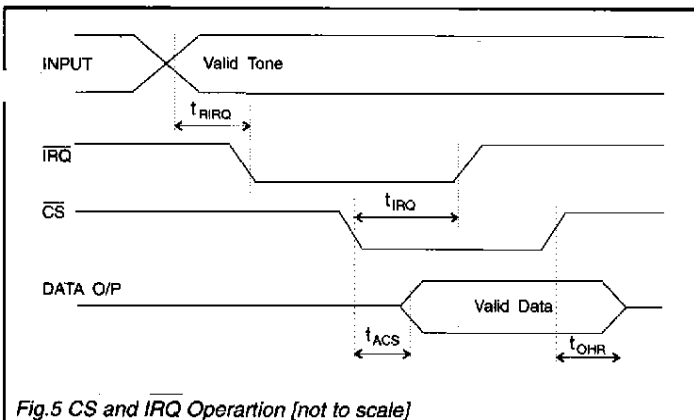


### Timing Specification

	Min.	Typ.	Max.	Unit
$t_{PUR}$	2.0	-	-	ms
$t_{DE}$	-	33.0	-	ms
$t_{PULS}$	-	1.0	-	ms
$t_{DC}$	0.5	-	1.0	ms
$t_{RESP}$	20.0	-	33.0	ms
$t_{NT}$	33.0	-	53.0	ms
$t_{DATA}$	-	-	2.0	ms
$t_{NORM}$	-	-	120	$\mu$ s
$t_{HOLD}$	50.0	-	-	$\mu$ s
$t_{IRQ}$	-	-	250	ns
$t_{RIRO}$	20.5	-	34.0	ms
$t_{ACS}$	-	-	250	ns
$t_{OHR}$	-	-	100	ns

### Notes:

1. 'E' is the start-up (power-up reset) condition.
2. The state of D0/1/2/3 will represent the input frequency present during and after Power-Up Reset (F [Notone] in the Figure 3 example).



## Specification

### Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref $V_{SS} = 0V$ )	-0.3 to ( $V_{DD} + 0.3V$ )
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ $T_{AMB} = 25^{\circ}C$	800mW Max.
Derating	10mW/ $^{\circ}C$
Operating Temperature ( $T_{OP}$ ): <b>FX013J/LG</b>	-40 $^{\circ}C$ to +85 $^{\circ}C$
Storage temperature range ( $T_{ST}$ ): <b>FX013J/LG</b>	-55 $^{\circ}C$ to +125 $^{\circ}C$

### Functional Limits .....

Supply Voltage ( $V_{DD}$ )

Min.	Max.	Unit
2.5	5.5	V at 25 $^{\circ}C$

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD} = 5.0V$   $T_{OP} = -40$  to +85  $^{\circ}C$ . Xtal/Clock or 'Clock In' Frequency = 560kHz.

Characteristics	See Note	Min.	Typ.	Max.	Unit
<b>Static Values</b>					
Supply Voltage ( $V_{SS}=0V$ )		2.5	-	5.5	V
Supply Current		-	500	-	$\mu A$
Logic "1" Output (Source = 1 mA)	1	4.5	-	-	V
Logic "0" Output (Sink = 1 mA)	1	-	-	0.5	V
Logic "1" Input Level	2	3.5	-	-	V
Logic "0" Input Level	2	-	-	1.5	V
Oscillator Output Level					
<b>Input Impedances</b>					
Signal In		-	1.0	-	M $\Omega$
Clock Select		-	1.0	-	M $\Omega$
Hold I/P		-	1.0	-	M $\Omega$
Chip Select		-	10.0	-	M $\Omega$
<b>Output Impedances</b>					
D0 - D3		-	1.0	-	k $\Omega$
Data Change		-	1.0	-	k $\Omega$
Oscillator Outputs		-	10.0	-	k $\Omega$
<b>Dynamic Values</b>					
Signal Input Range	3	35.0	-	$V_{DD}/2$	mVrms
Decode Bandwidth when $P > 0.995$					
QA	4	$\pm 20.0$	-	-	Hz
QC	4	$\pm 1.0$	-	-	%
Not-Decode Bandwidth when $P < 0.03$					
QA	5	-	-	$\pm 60.0$	Hz
QC	5	-	-	$\pm 3.0$	%
Noise Response Rate (hours per F - F : F single character response with no input tone).					
QA	6	-	0.15	-	/hour
QC	6	-	40.0	-	/hour
Decode Response Time:					
NOTONE to Tone (F - F)	7	20.0	25.0	33.0	ms
Tone to NOTONE, Tf (F - F)	7	33.0	-	53.0	ms
Minimum inter-tone gap for "F"	8	15.0	-	28.0	ms

### Notes:

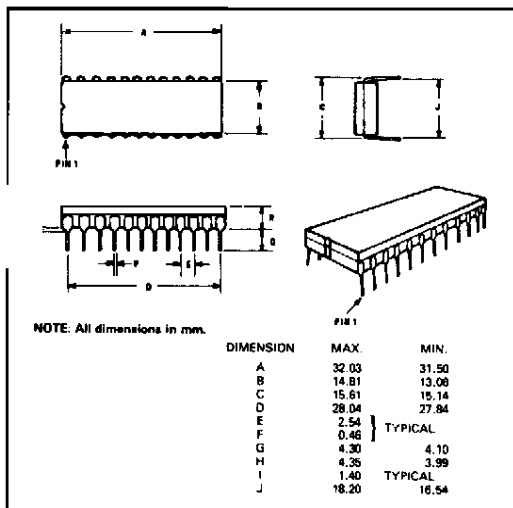
- Pins 7, 8, 17 and 19, 20, 22 and 23.
- Pins 13,14 and 16.
- An ac coupled sine/squarewave.
- With minimum tone period ( $T_p$ ) specified for toneset. P = Decode Probability. (QA) SNR = 3dB. (QC) SNR = 0dB.
- All conditions of input SNR and amplitude with maximum  $T_p$  specified for the toneset.
- Gaussian input noise, bandwidth 6.0kHz, maximum input level corresponds to 1-digit code falsing rate. F = random single character.
- Delay from change of input (tone applied/removed) to change at Q0-Q3 outputs.
- Included in  $t_{NR}$ . Minimum tone gap requirement for "Notone" recognition. Outputs = F after delay.

## Package Outlines

The FX013J, the cerdip package is shown in Figure 6 and the 'LG' quad plastic version in Figure 7.

Pin 1 identification marking is shown on the relevant diagram and pins on both package styles number anti-clockwise when viewed from the top (marked side).

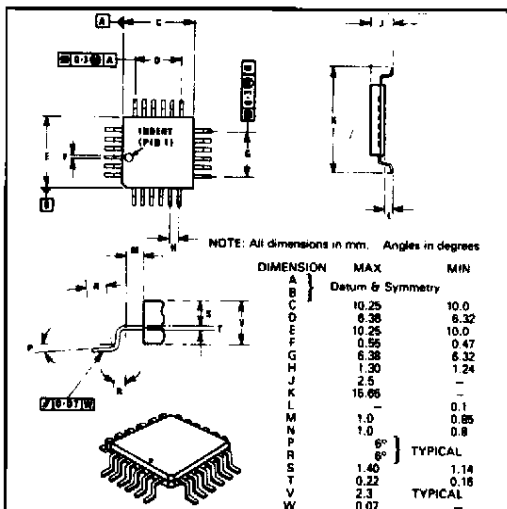
Fig.6 FX013J 24-pin cerdip Package



## Handling Precautions

The FX013 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

Fig.7 FX013LG quad plastic Package



## Ordering Information

The FX013 is available in two tonesets and two package styles: 'A' = EIA Tones

'C' = CCIR Tones

Please order the correct toneset in the correct package.

### FX013J 'A' / 'C'

24-pin cerdip DIL

### FX013LG 'A' / 'C'

24-pin plastic encapsulated  
bent and cropped