November 1989
Edition 1.1

FUJITSU

DATA SHEET

MB81C1002-70/-80/-10/-12

CMOS 1,048,576 BIT STATIC COLUMN MODE DYNAMIC RAM

CMOS 1,048,576 X 1 BIT Static Column Mode Dynamic RAM

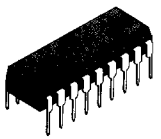
PRELIMINARY

The Fujitsu MB81C1002 is CMOS fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1002 has been designed for mainframe memories, buffer memories, and video image memories requiring high speed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB81C1002 High α-ray soft error immunity and long refresh time.

The CMOS circuits can be used as peripheral circuits. In addition, low power dissipation and high speed operation are realized.

The specification is applied to "BC" version revised with intent to realized faster access time. So faster speed version (70ns and 80ns) are available on this chip.



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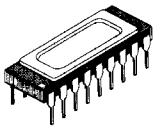

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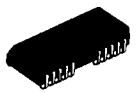

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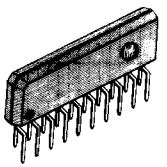

ZIP-20P-M02

PRODUCT LINE & FEATURES

Parameter	MB81C1002 -70	MB81C1002 -80	MB81C1002 -10	MB81C1002 -12
$\overline{RAS}$ Access Time	70ns max.	80ns max.	100ns max.	120ns max.
Random Cycle Time	140ns min.	155ns min.	180ns min.	210ns min.
Address Access Time	43ns max.	45ns max.	50ns max.	60ns max.
$\overline{CAS}$ Access Time	25ns max.	25ns max.	25ns max.	35ns max.
Static Column Mode Cycle Time	48ns min.	50ns min.	55ns min.	65ns min.
Low Power Dissipation • Operating current	413mW max.	385mW max.	330mW max.	275mW max.
• Standby current	11mW max. (TTL level) / 5.5mW max. (CMOS level)			

- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Static column Mode, Read-Modify-Write capacity
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to VSS		V_{IN}, V_{OUT}	−1 to +7	V
Voltage of V_{CC} supply relative to VSS		V_{CC}	−1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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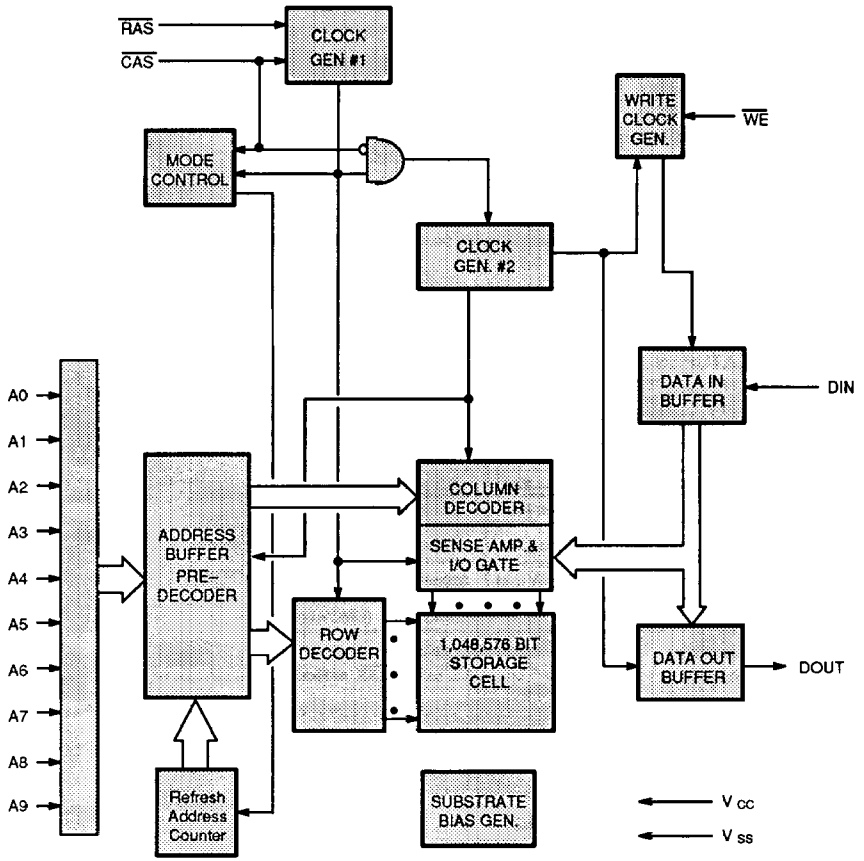
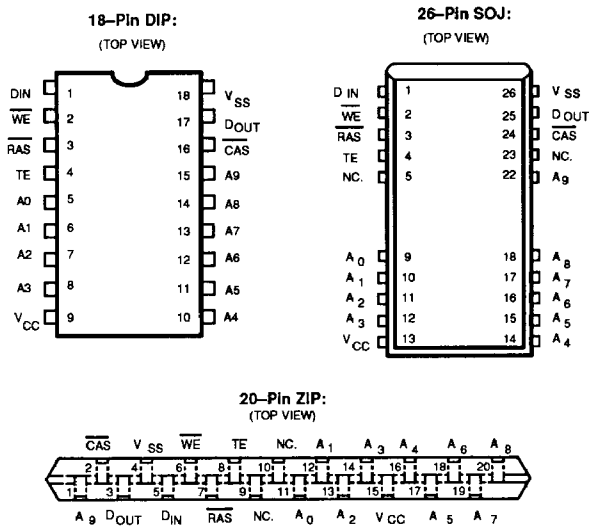
Fig. 1 — MB81C1002 DYNAMIC RAM—BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, D_{OUT}	C_{OUT}	—	5	pF

PIN ASSIGNMENTS AND DESCRIPTIONS



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A9	Address inputs.
VCC	+5 volt power supply.
TE	Test Enable (will be available).
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	-2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any one of 1,048,576 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A9 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

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WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Data is written into the MB81C1002 during write or read–modify–write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read–modify–write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater then t_{RAD} (max).

STATIC COLUMN MODE OF OPERATION

The static column mode operation allows continuous read, write, or read–modify–write cycle within a rowby applying new column address. In the static column mode, $\overline{RAS}$ can be kept low throughout static column mode operation.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) Notes 3

Parameter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	IOH = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	IOL = 4.2 mA	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	0V ≤ VIN ≤ 5.5V; 4.5V ≤ VCC ≤ 5.5V; VSS=0V; All other pins not under test =0V	–10	—	10	μA
Output leakage current		$I_{O(L)}$	0V ≤ VOUT ≤ 5.5V; Data out disabled	–10	—	10	
Operating current (Average power supply current) [2]	MB81C1002–70	ICC_1	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB81C1002–80					70	
	MB81C1002–10					60	
	MB81C1002–12					50	
Standby current (Power supply current)	TTL level	ICC_2	$\overline{RAS}$=$\overline{CAS}$=VIH	—	—	2.0	mA
	CMOS level		$\overline{RAS}$=$\overline{CAS}$ ≥ VCC–0.2V			1.0	
Refresh current #1 (Average power supply current) [2]	MB81C1002–70	ICC_3	$\overline{CAS}$=VIH, $\overline{RAS}$ cycling; t_{RC}= min	—	—	70	mA
	MB81C1002–80					65	
	MB81C1002–10					55	
	MB81C1002–12					45	
Static column mode current [2]	MB81C1002–70	ICC_4	$\overline{RAS}$ = $\overline{CAS}$ =VIL cycling; t_{SC} = min	—	—	37	mA
	MB81C1002–80					35	
	MB81C1002–10					30	
	MB81C1002–12					23	
Refresh current #2 (Average power supply current) [2]	MB81C1002–70	ICC_5	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} = min	—	—	70	mA
	MB81C1002–80					65	
	MB81C1002–10					55	
	MB81C1002–12					45	

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1002-70		MB81C1002-80		MB81C1002-10		MB81C1002-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	140	—	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	167	—	182	—	210	—	245	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	9	t_{CAC}	—	25	—	25	—	25	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	43	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	7	—	7	—	7	—	7	—	ns
8	Output Buffer Turn on Delay Time		t_{ON}	5	—	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	25	—	30	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	22	55	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	25	—	30	—	35	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	70	—	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	21	t_{CPN}	15	—	15	—	15	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	12	—	15	—	15	—	ns
21	Column Address Set Up Time	7	t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	20	—	20	—	20	—	25	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	43	—	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Hold Time		t_{WCH}	20	—	20	—	20	—	25	—	ns
29	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	15	—	20	—	ns
30	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	22	—	22	—	25	—	30	—	ns
31	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	17	—	17	—	20	—	25	—	ns
32	DIN Set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
33	DIN Hold Time		t_{DH}	20	—	20	—	20	—	25	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1002-70		MB81C1002-80		MB81C1002-10		MB81C1002-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
34	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15,20	t_{RWD}	70	—	80	—	100	—	120	—	ns
35	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	25	—	25	—	30	—	35	—	ns
36	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	43	—	45	—	50	—	60	—	ns
37	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
38	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
39	$\overline{CAS}$ Hold Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	15	—	20	—	ns
40	Access Time from $\overline{CAS}$ (Counter Test Cycle)		t_{CAT}	—	43	—	45	—	50	—	60	ns
50	Static Column Mode Read/Write Cycle Time		t_{SC}	48	—	50	—	55	—	65	—	ns
51	Static Column Mode Read–Modify–Write Cycle Time		t_{SRWC}	96	—	100	—	110	—	130	—	ns
52	Access Time Relative to Last Write	16	t_{ALW}	—	91	—	95	—	105	—	125	ns
53	Access Time from $\overline{WE}$ Precharge		t_{WPA}	—	25	—	25	—	30	—	35	ns
54	Output Hold Time for Column Address Change		t_{AOH}	10	—	10	—	10	—	10	—	ns
55	Write Latched Data Hold Time		t_{WOH}	0	—	0	—	0	—	0	—	ns
56	Column Address Hold Time Referenced to $\overline{RAS}$ Rising Time	17	t_{AHR}	15	—	15	—	15	—	15	—	ns
57	Last Write to Column Address Delay Time	18,19	t_{LWAD}	25	48	25	50	25	55	30	65	ns
58	Column Address Hold Time Referenced to Last Write		t_{AHLW}	91	—	95	—	105	—	125	—	ns
59	$\overline{RAS}$ to Second Write Delay Time		t_{RSWD}	70	—	80	—	100	—	120	—	ns
60	$\overline{WE}$ Inactive Time		t_{WI}	13	—	15	—	15	—	20	—	ns
61	Write Set Up Time for Output Disable	20	t_{WS}	0	—	0	—	0	—	0	—	ns
62	Write Hold Time for Output Disable	20	t_{WH}	0	—	0	—	0	—	0	—	ns
63	Static Column Mode $\overline{CAS}$ Precharge Time		t_{CP}	15	—	15	—	15	—	15	—	ns
64	Write Command Hold Time Referenced to $\overline{RAS}$		t_{WHR}	5	—	5	—	5	—	5	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ = VIH) of 200µs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leqq t_{RCD}$ (max), and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown. Refer to Fig. 2 and 3.
7. Assumes that write cycle only.
8. If $t_{RAD} \geqq t_{RAD}$ (max), access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min) + 2t_T + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
16. Assumes that $t_{LWAD} \leqq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{AWL} will be increased by the amount that t_{LWAD} exceeds the value shown.
17. t_{AHR} is specified to latch column address by the rising edge of $\overline{RAS}$.
18. Operation within the t_{LWAD} (max) limit insures that t_{AWL} (max) can be met. t_{LWAD}(max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled by t_{AA}.
19. t_{LWAD} (min) = t_{CAH} (min) + t_T (t_T=5ns).
20. t_{WS}, t_{WH} and t_{RWD} are specified as a reference point only. If $t_{WS} \geqq t_{WS}$(min) and $t_{WH} \geqq t_{WH}$(min), the data output pin will remain High-Z state through entire cycle. If It $t_{RWD} \geqq t_{RWD}$(min), the data output will contain data read from the selected cell.
21. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only

Fig. 2 – t_{RAC} vs. t_{RCD}

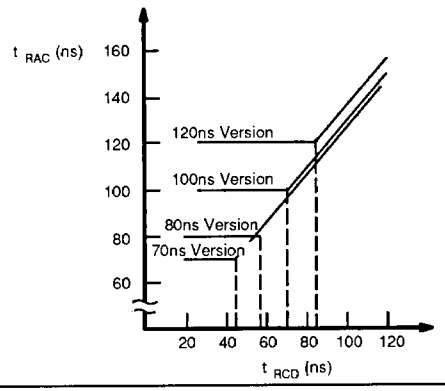
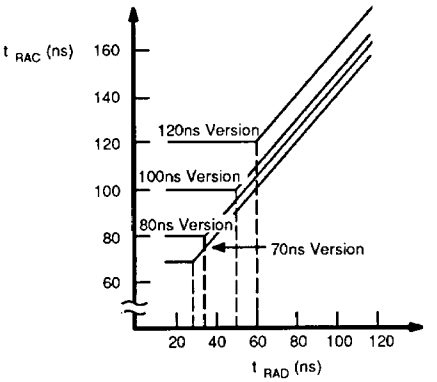


Fig. 3 – t_{RAC} vs. t_{RAD}



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FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	O	$t_{RCS} \geq t_{RCS}$ (min) $t_{RCH} \geq t_{RCH}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	*1 High-Z	O	$t_{WS} \geq t_{WS}$ (min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	O	$t_{CWD} \geq t_{CWD}$ (min)
Static Column Mode Read Cycle	L	L	H	*2 Valid	Valid	—	Valid	X	$t_{RCS} \geq t_{RCS}$ (min) $t_{RCH} \geq t_{RCH}$ (min)
Static Column Mode Write Cycle	L	L	L	*2 Valid	Valid	Valid	*1 High-Z	X	
Static Column Mode Read–Modify–Write Cycle	L	L	H → L	*2 Valid	Valid	X → Valid	Valid	X	$t_{CWD} \geq t_{CWD}$ (min)
Static Column Mode Mixed Cycle	L	L	L/H	*2 Valid	Valid	Valid	High-Z or Valid	X	
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	O	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	—	—	—	High-Z	O	
Hidden Refresh Cycle	H → L	L	X	—	—	—	Valid	O	Previous data is kept

Notes:

X : "H" or "L"

*1: If $t_{WS} < t_{WS}$ (min) and $t_{WH} < t_{WH}$ (min), the data output become invalid.

*2: After first cycle, row address is not necessary.

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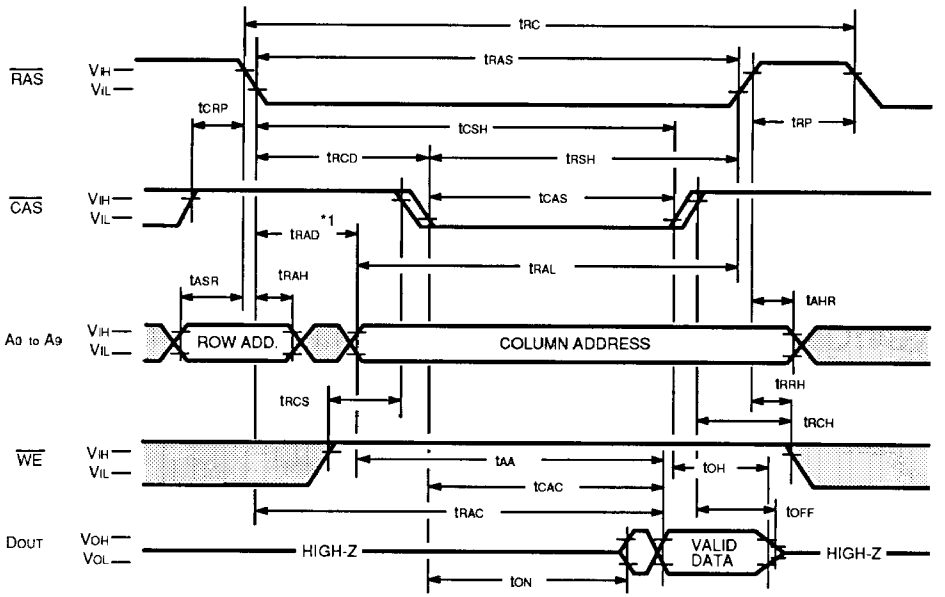
TIMING DIAGRAMS

Fig. 4 – READ CYCLE



*1; If tRAD ≥ tRAD (max), access time is tCAC or tAA whichever occur later.

"H" or "L"

DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" through out the cycle. Therow and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remain valid with $\overline{CAS}$ "L", i.e., if $\overline{CAS}$ goes "H", the data becomes invalid with tDH. During read cycle, the DIN pin is "H" or "L". The acces time is determined by $\overline{RAS}$(tRAC), $\overline{CAS}$(tCAC), or Column address input(tAA). If tRCD ($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is tCAC or tAA whichever occur later.

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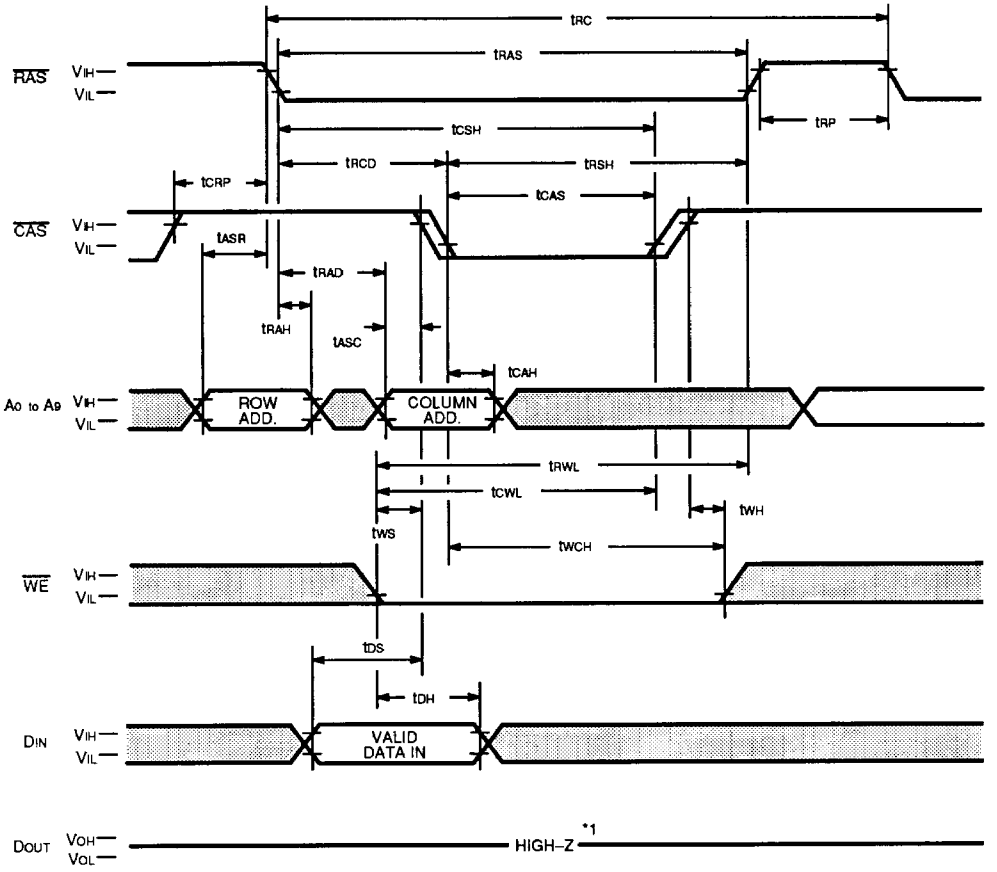
Fig. 5 – WRITE CYCLE (Early Write)



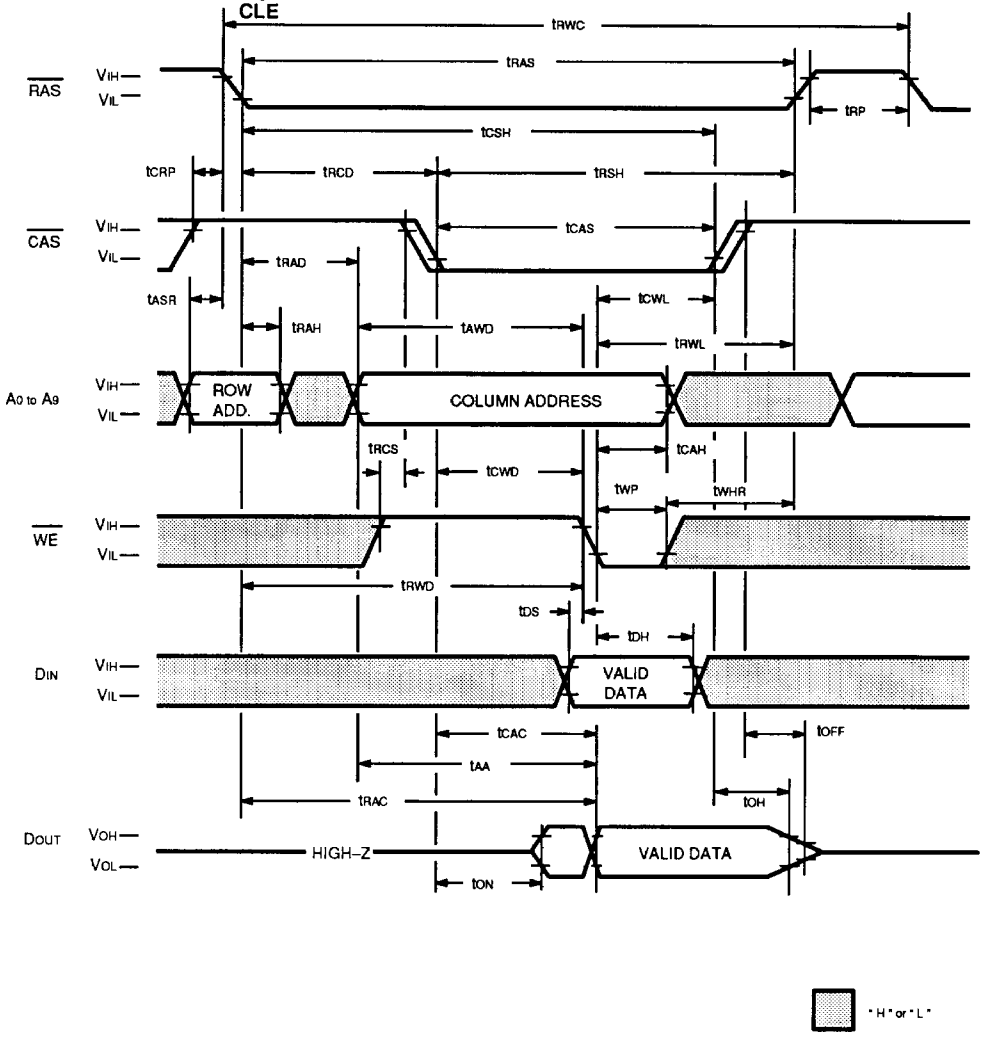
*1; If tWS ≥ tWS (min) and tWH ≥ tWH (min), DOUT is high–Z.

DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pin. The data on DIN pin is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, duringwrite cycle, tRWL, tCWL and tRAL must be satisfied the specifications.

2

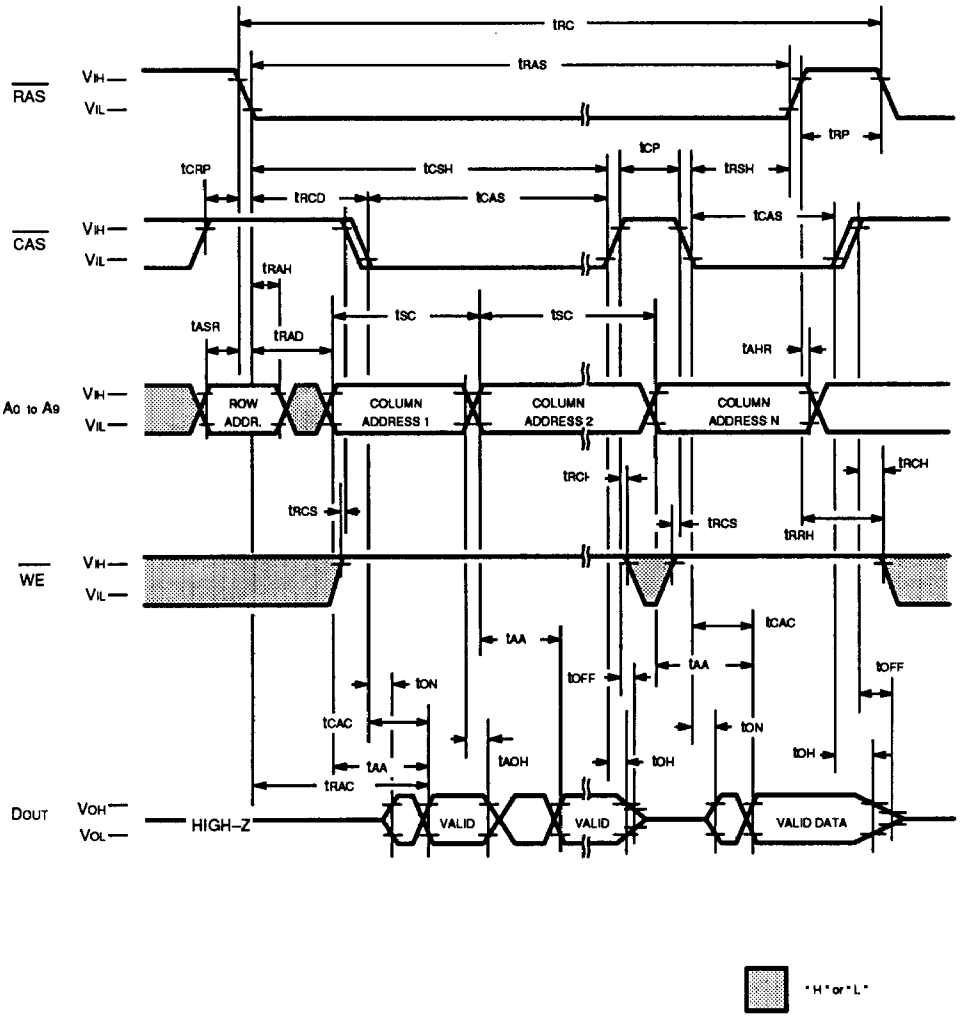
Fig. 6 – READ WRITE/READ–MODIFY–WRITE CYCLE



DESCRIPTION

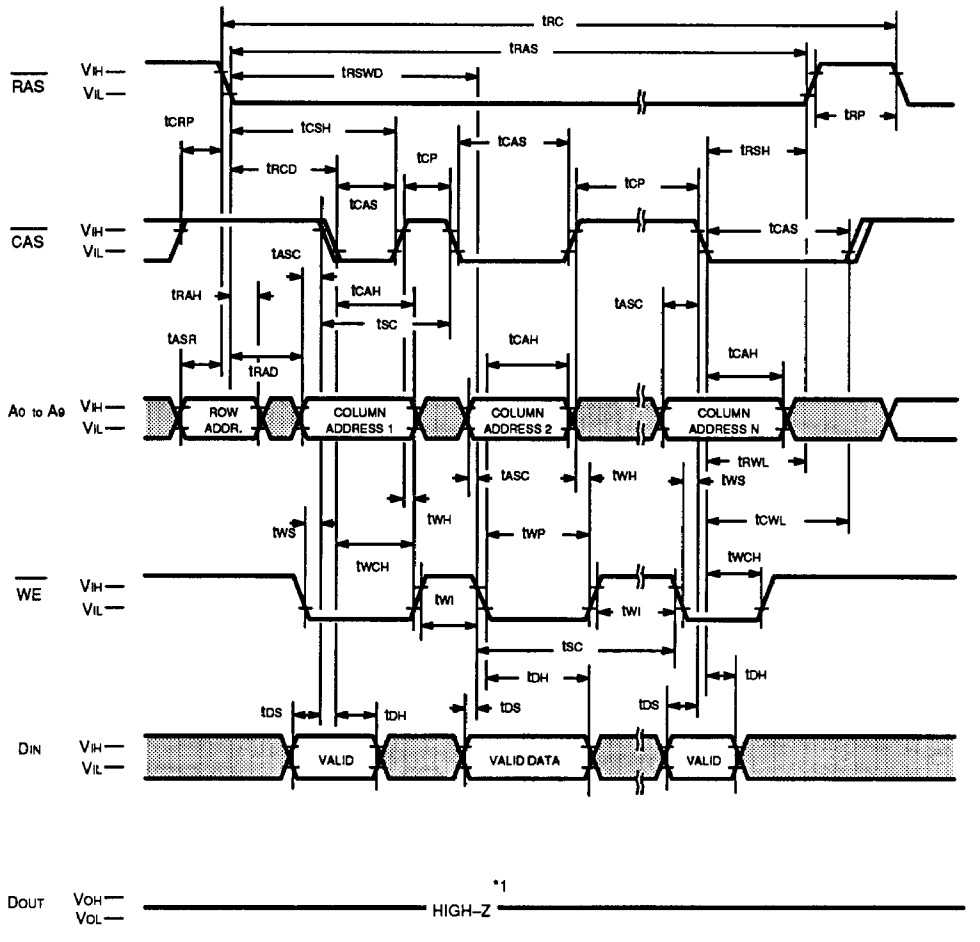
The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DOUT pin. This new data is written into the same address as read out.

Fig. 7 – STATIC COLUMN MODE READ CYCLE



2

Fig. 8 – STATIC COLUMN MODE WRITE CYCLE

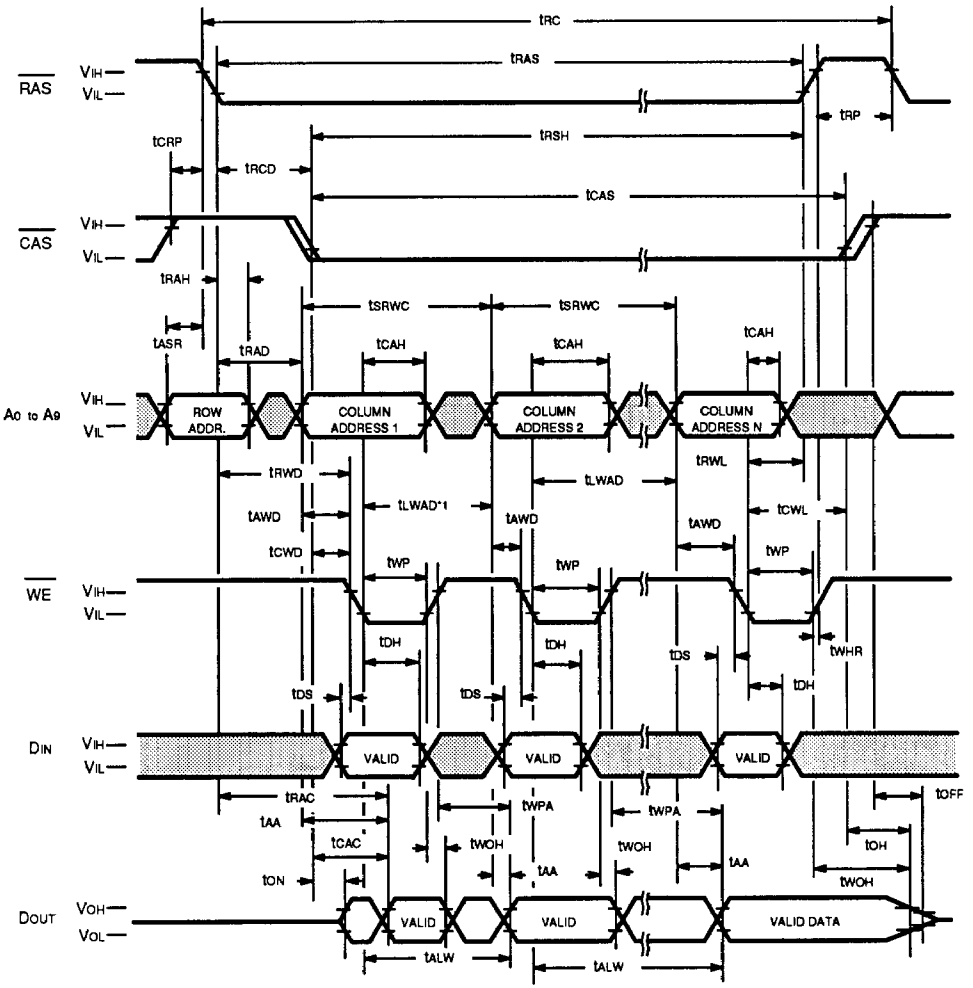


*1; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), DOUT is high–Z.

DESCRIPTION

In a static column mode write cycle, the data is written into the cell triggered by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. It is not necessary to bring both $\overline{WE}$ and $\overline{CAS}$ "L", only one signal should be brought "L" while the other signal is toggled. If both tWS and tWH are greater than their minimum limits, the data output pin is kept high impedance state through the static column mode write cycle.

Fig. 9 – STATIC COLUMN MODE READ–MODIFY–WRITE CYCLE



*1; If tLWAD (min) ≤ tLWAD ≤ tLWAD (max), tALW = tSC (min) + tAA (max).

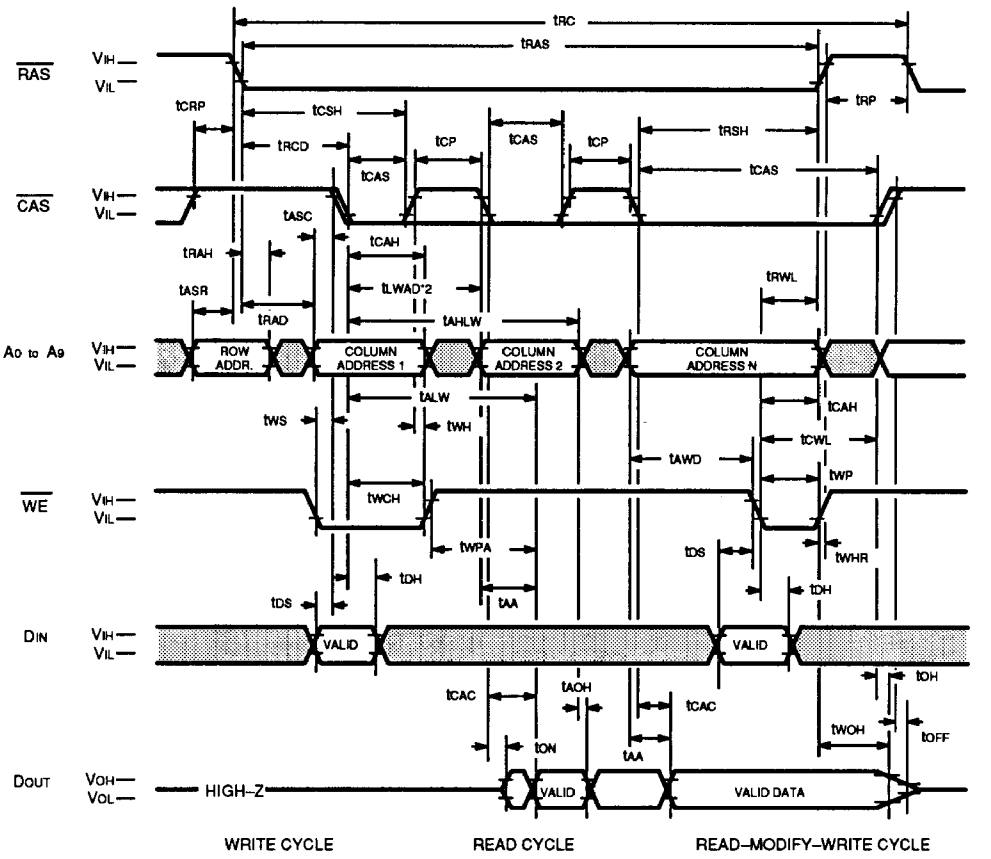
"H" or "L"

DESCRIPTION

In the static column mode read-modify-write cycle, $\overline{WE}$ goes low after tAWD from the column address inputs and tCWD from the faling edge of $\overline{CAS}$. The data and column address inputs are strobed and latched by the falling edge of $\overline{WE}$.

2

Fig. 10 – STATIC COLUMN MODE MIXED CYCLE *1



*1; This is an example of static column mode mixed cycle.
*2; If tLWAD is satisfied its min/max value, tALW = tSC (min) + tAA (max)

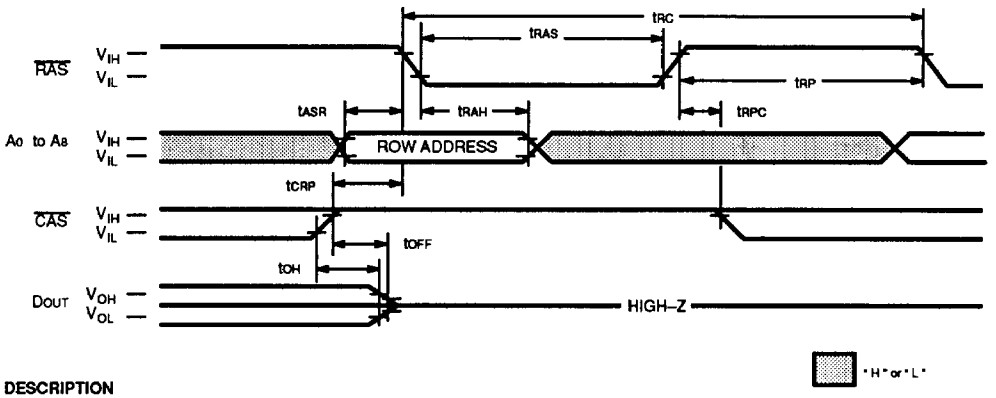
"H" or "L"

DESCRIPTION

In the static column mode, read, write, and read-modify-write cycles can be mixed in any order.
In the next read cycle of static column mode write cycle or read-modify-write cycle, the access time is determined by the following conditions.

1. tALW from the falling edge of $\overline{WE}$ or $\overline{CAS}$ at previous write cycle.
2. tAA from the column address inputs.
3. tWPA from the rising edge of $\overline{WE}$ at the read cycle.
4. tCAC from the falling edge of $\overline{CAS}$.

Fig. 11 – $\overline{RAS}$–ONLY REFRESH CYCLE
NOTE: A9, $\overline{WE}$, DIN = " H " or " L "

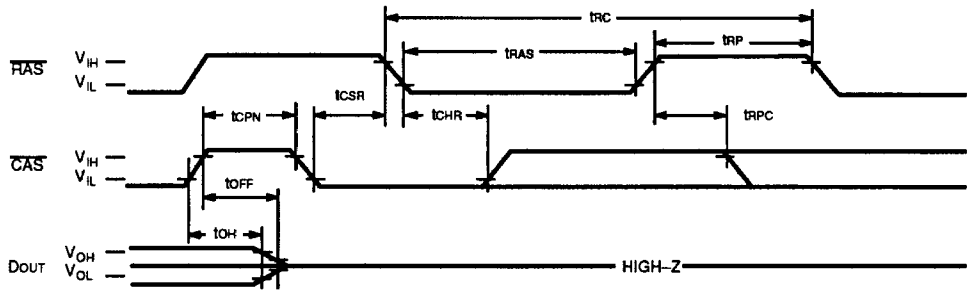


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycleat each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DOUT pin is kept in a high-impedance state.

Fig. 12 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH CYCLE
NOTE: A0 to A9, $\overline{WE}$, DIN = " H " or " L "

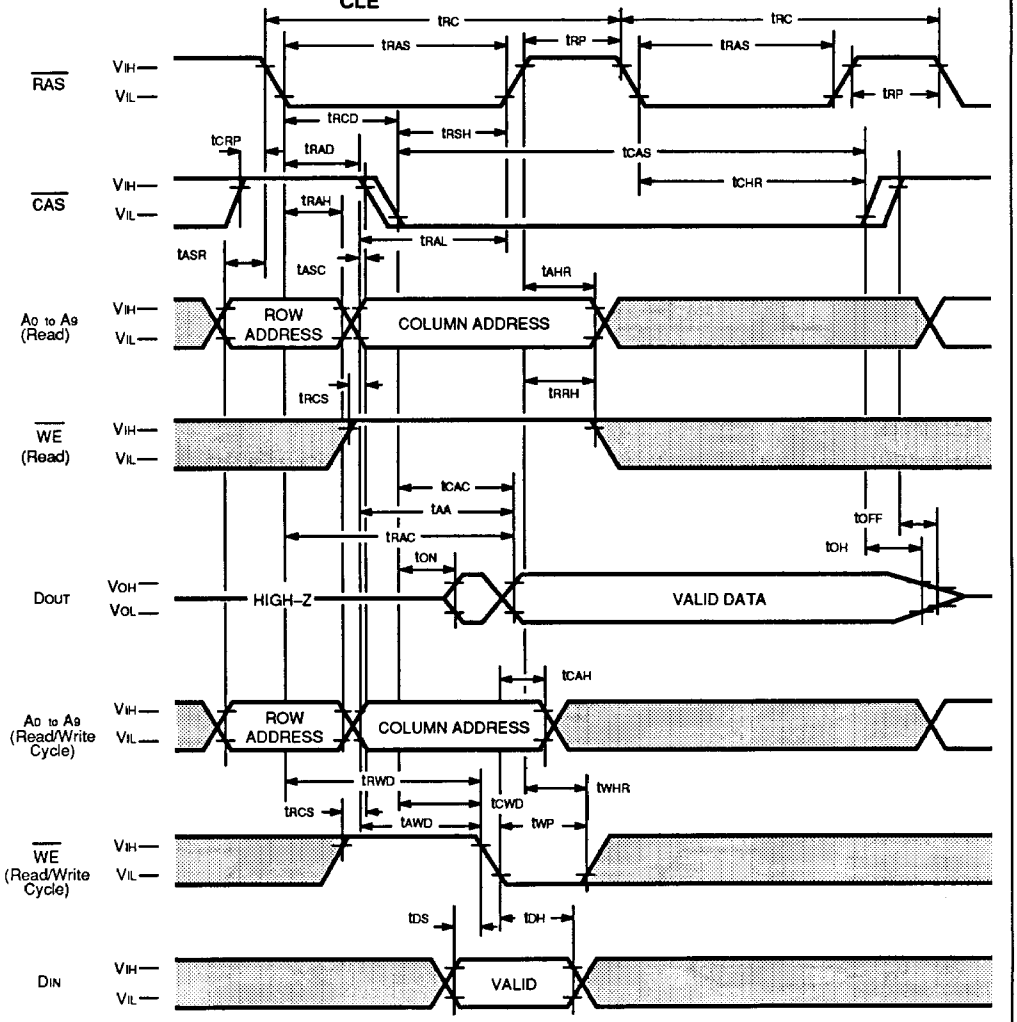


DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

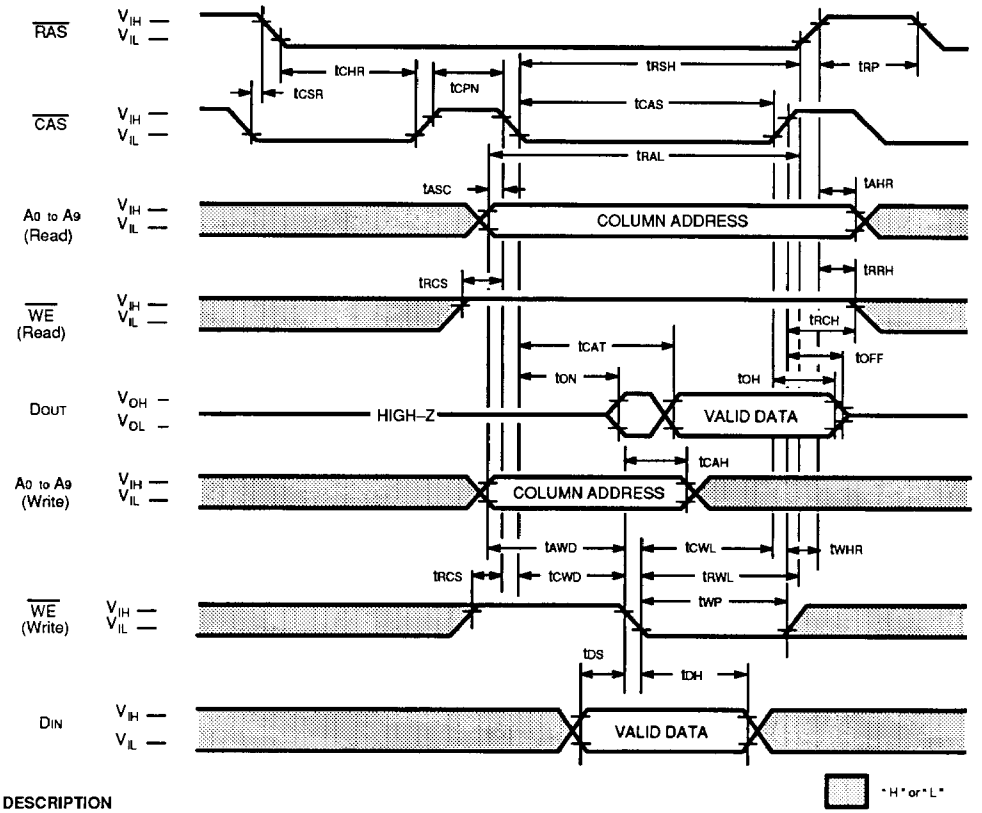
Fig. 13 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminatesthe need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 14 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A9 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A9 are defined by latching levels on A0–A9 at the second falling edge of $\overline{CAS}$.

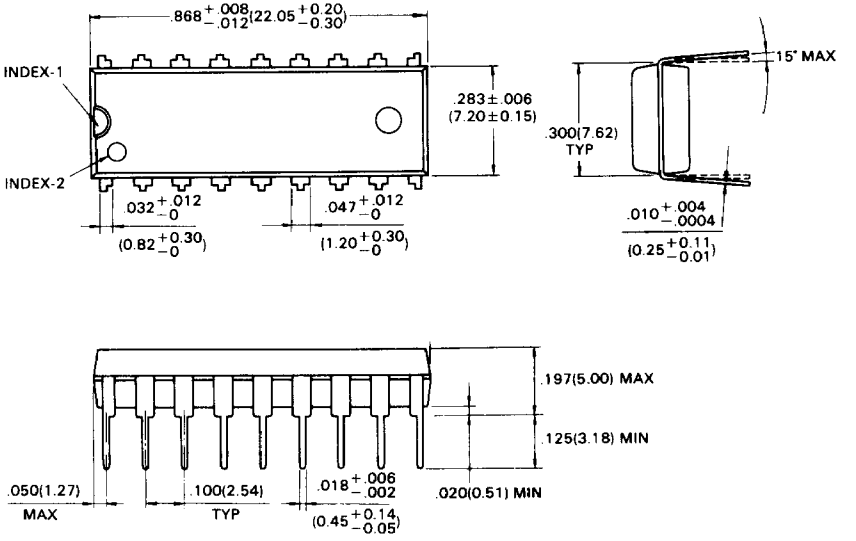
The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle is designed for use with the following procedures:

1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Use the same column address throughout the test.
3) Write zeroes (0s) to all 512 row addresses at the same column address by using normal early write cycles.
4) Read zeroes written in procedure 3 and check; simultaneously write ones (1s) to the same addresses by using internal refresh counter test read-write cycles. Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4 by using normal read cycle for all 512 memory locations.
6) Complement test pattern and repeat procedures 3, 4, and 5.

PACKAGE DIMENSIONS

(Suffix: –P)

18–LEAD PLASTIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–18P–M04)

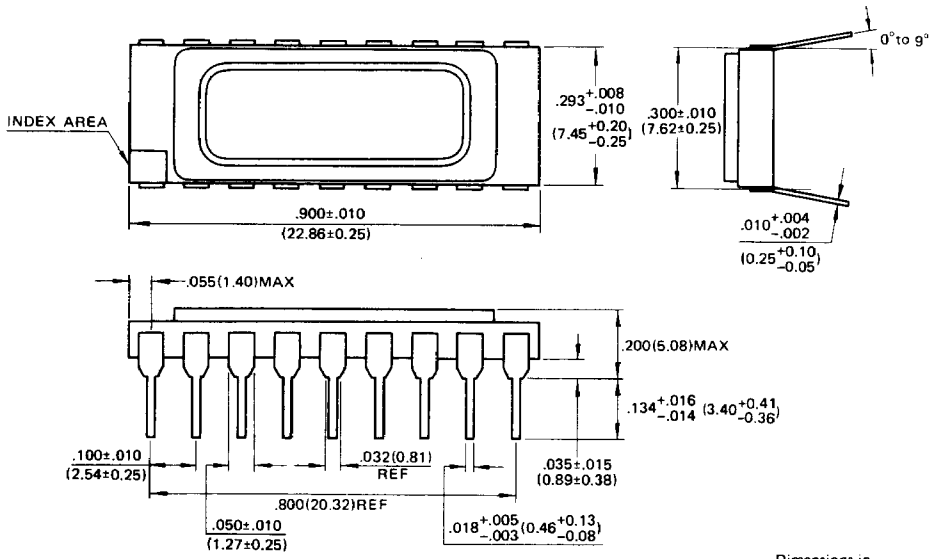


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –C)

18–LEAD CERAMIC (METAL SEAL) DUAL IN–LINE PACKAGE
(CASE No.: DIP–18C–A01)

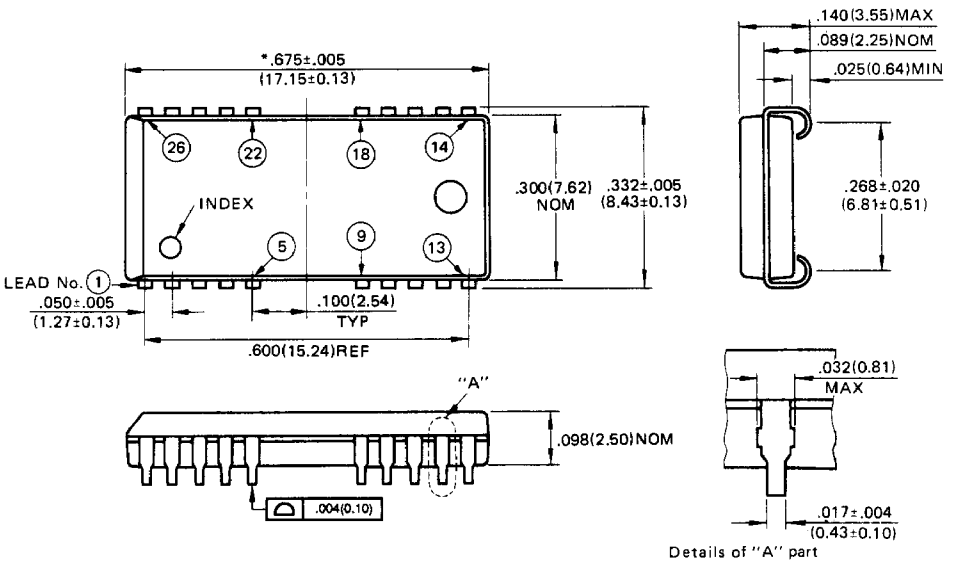


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: -PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER (SOJ-26)
(CASE No.: LCC-26P-M04)



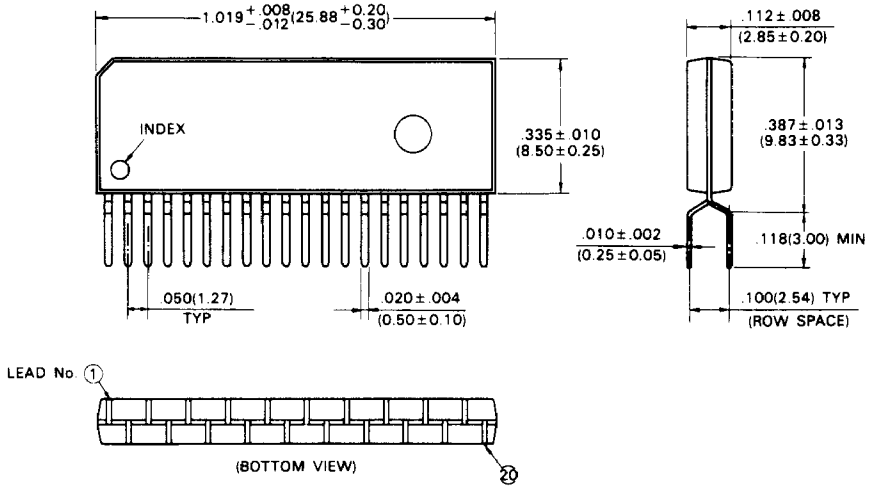
NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –PSZ)

20–LEAD PLASTIC ZIGZAG–IN–LINE PACKAGE
(CASE No.: ZIP–20P–M02)



Dimensions in
inches (millimeters)