Am29130

16-Bit Barrel Shifter

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Powerful Shifter
  - Shifts or rotates left/right with a two's-complement or a sign-magnitude shift count.
- Bit Insertion
  - Inserts a fill bit depending on the position from the shift count bits.
- All Fill
  - Fills all bits with ones/zeros.
- Expandable
  - Expands to 16n-bit shifter without any intrinsic speed penalty.
- High-Speed IMOX™-S2 Technology
  - Provides D-to-Y propagation delay of 28 ns.

GENERAL DESCRIPTION

The Am29130 is a 16-bit high-speed barrel shifter that is expandable to 16n bits without any intrinsic speed penalty.

The primary function of the device is to shift/rotate left/right with a two's-complement or sign-magnitude shift count. It also has the capability of bit insertion in the position specified in the shift count bits.

These features allow the designer to have bit manipulation and acceleration of arithmetic operations in their graphic or microcomputer systems, bit-reversal for FFT, and dynamic multiplexing capabilities in the concurrent systems. Since the Am29130 can be connected in parallel to the ALU, it also offers greater throughput with the ALU and the shifter working simultaneously.

BLOCK DIAGRAM

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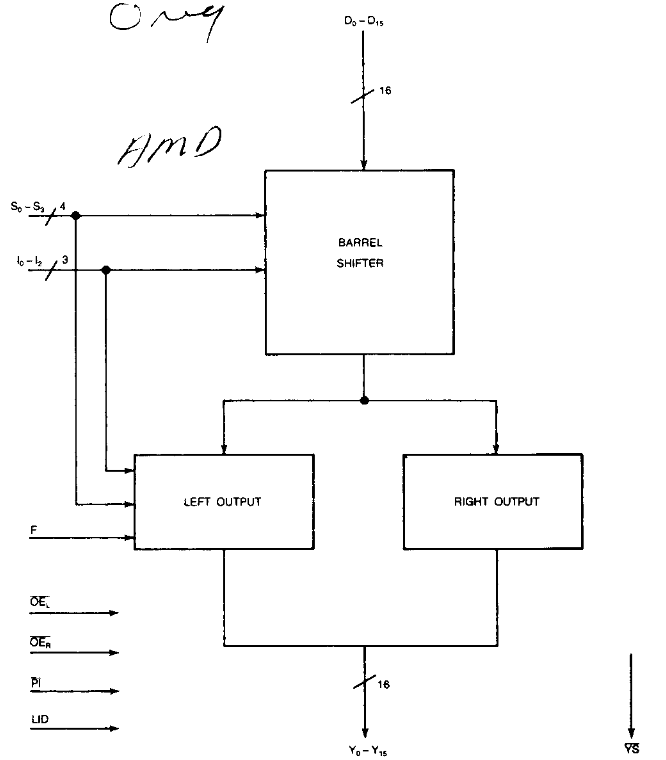

BD006570

Publication # 05179 Rev. C Amendment /0
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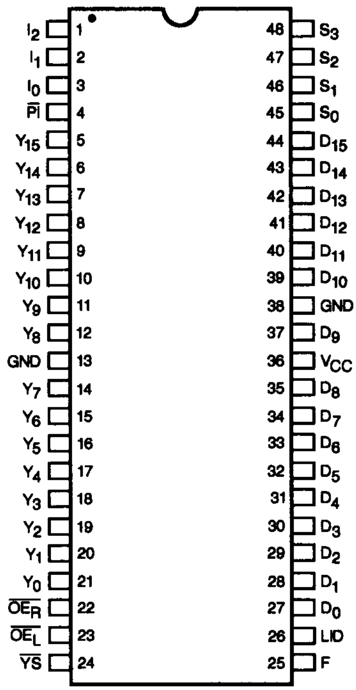
RELATED AMD PRODUCTS

Part Number	Description
Am2901C	4-Bit Bipolar Microprocessor Slice
Am29C01, Am29C01-1	4-Bit CMOS Microprocessor Slice
Am2910A	Bipolar Microprogram Controller
Am29C10A, Am29C10A-1	CMOS Microprogram Controller
Am29C101, Am29C101-1	16-Bit CMOS Microprocessor Slice
Am29114	Real-Time Interrupt Controller
Am29116, Am29L116A, Am29116A, Am29117	16-Bit Bipolar Microprocessors
Am29C116, Am29C116-1, Am29C117	16-Bit CMOS Microprocessors
Am29PL141	Fuse-Programmable Controller
Am29501A	Multiport Pipelined Processor
Am29C509	12 x 12 CMOS MAC
Am29C516, Am29C517	16 x 16 CMOS Parallel Multipliers
Am29516, Am29516A, Am29L516, Am29L516A, Am29517, Am29517A, Am29L517, Am29L517A	16 x 16 Bipolar Parallel Multipliers
Am29520A, Am29521A	Pipeline Registers
Am29524, Am29525	Pipeline Registers
Am29540	FFT Address Sequencer
Am29818	SSR Diagnostic Register

CONNECTION DIAGRAM
Top View

DIPs



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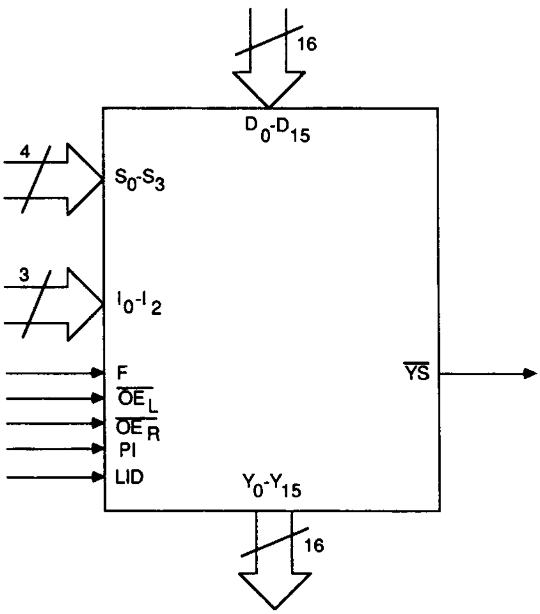
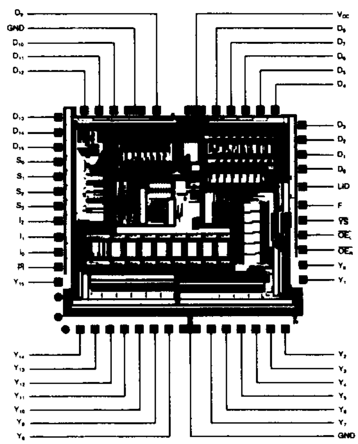
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002930

METALLIZATION AND PAD LAYOUT



Die Size: 0.164" x 0.182"
Gate Count: 514

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

AM29130 D C B

E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

C. PACKAGE TYPE
P = 48-Pin Plastic DIP (PD 048)
D = 48-Pin Sidebrazed Ceramic DIP (SD 048)

B. SPEED OPTION
Not Applicable

A. DEVICE NUMBER/DESCRIPTION
Am29130
16-Bit Barrel Shifter

Valid Combinations	
AM29130	PC, PCB, DC, DCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**

B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish

AM29130 /B X C

E. LEAD FINISH
C = Gold

D. PACKAGE TYPE
X = 48-Pin Sidebrazed Ceramic DIP (SD 048)

C. DEVICE CLASS
/B = Class B

B. SPEED OPTION
Not Applicable

A. DEVICE NUMBER/DESCRIPTION
Am29130
16-Bit Barrel Shifter

Valid Combinations	
AM29130	/BXC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$D_0 - D_{15}$ Data (Input)
The data to be operated on is fed into the device through these inputs.

F Fill Bit (Input)
The F input replaces the bit addressed by $S_0 - S_3$ with the insert fill function. It is enabled by $\overline{OE_L}/\overline{OE_R}$ for shift left/right functions. The outputs are replaced by the fill bit with the all-fill function.

$I_0 - I_2$ Instruction (Input)
The instruction inputs select the operation to be performed.

LID Location Identifier (Input, Three State)
The LID is used for bank shifting. When LID is open, the weighting of the D inputs and the Y outputs is the same. When LID is LOW, the Y outputs have a smaller weighting than the D inputs. When LID is HIGH, it is vice versa.

$\overline{OE_L}$ Left Output Enable (Input, Active LOW)
When $\overline{OE_L}$ is LOW, the left output bits are enabled. When $\overline{OE_L}$ is HIGH, the left output bits are disabled.

$\overline{OE_R}$ Right Output Enable (Input, Active LOW)
When $\overline{OE_R}$ is LOW, the right output bits are enabled. When $\overline{OE_R}$ is HIGH, the right output bits are disabled.

$\overline{PI}$ Polarity/Insert (Input)
The $\overline{PI}$ controls the polarity of the left/right output bits. When $\overline{PI}$ is LOW, the output data is complemented. When $\overline{PI}$ is HIGH, the output is unchanged. It is also used for the insert-fill function when $\overline{PI}$ is LOW and for the bypass function when $\overline{PI}$ is HIGH.

$S_0 - S_3$ Shift Count (Input)
The shift count is either a sign magnitude or a two's-complement number, depending on the instruction codes.

$\overline{YS}$ Sticky Bit (Output, Open Collector)
$\overline{YS}$ is a NOR of the bits shifted out in the shift left/right function. In the insert-fill function, the complement of the replaced bit is presented on $\overline{YS}$ (see Figure 1 for logic example).

$Y_0 - Y_{15}$ Data (Output, Three State)

FUNCTIONAL DESCRIPTION

The Am29130 expandable 16-bit barrel shifter is comprised of a barrel shifter and the left/right outputs as shown in the Block Diagram. It supports nine basic functions as listed in Table 1.

Shifter

The shift/rotate functions are implemented given a two's-complement or sign-magnitude shift count according to Table 1. I_2 controls left or right shift. I_2 equal to LOW implies a left shift/rotate function and I_2 equal to HIGH implies a right shift/rotate function. I_1 equal to LOW implies two's complement and I_1 equal to HIGH implies sign magnitude for shift-right functions. I_O controls shift or rotate functions. I_2 can be connected to the most significant bit of the shift count.

Polarity/Insert Control

In the insert-fill/bypass functions, the Am29130 does two things: 1) when $\overline{PI}$ is LOW, the fill bit is inserted on the position given by $S_0 - S_3$, and 2) when $\overline{PI}$ is HIGH, the data passes through the device unchanged. Figure 2 gives an example of the insert function when the shift count is 5. For other instructions, $\overline{PI}$ acts as polarity control. When $\overline{PI}$ is LOW, the output is the inverse of the input; when $\overline{PI}$ is HIGH, the input is passed unchanged.

Shift Count

$S_0 - S_3$ are used to control the barrel shifter. In the shift/rotate left function and shift/rotate right sign-magnitude function, $S_0 - S_3$ defines the shift count. In the shift/rotate right two's-complement functions, the two's complement of $S_0 - S_3$ defines the shift count.

Output Control

On any shift/rotate operation, $\overline{OE_L}$ and $\overline{OE_R}$ control the left and right output bits. When $\overline{OE_L}$ or $\overline{OE_R}$ is LOW, the left or right output bits are enabled.

The left output bits are defined as n bits, where $n \geqslant S_0 - S_3$, and the right output bits as m bits, where $m < S_0 - S_3$ for function code $I_2I_1I_0$ = X0X. For the function code $I_2I_1I_0$ = 11X, the left output bits are defined as n bits, where n $\geqslant$ two's complement of $S_0 - S_3$, and the right output bits as m, where m $<$ two's complement of $S_0 - S_3$.

When the Am29130 is used for 16-bit shift operations, the fill bit is enabled on the left/right output bits according to Table 2.

Tables 3-1 through 3-5, and 3-14 list the output for a 16-bit shifter for different function codes. Figures 3 and 4 show examples of rotate/shift operation.

Expandability

The Am29130 is expandable with the use of LID. For a 16-bit shifter, LID is left open. It indicates that the weighting of the input and output data is the same.

LID has its significance in using Am29130 as 16n-bit shifter. When LID is HIGH, the output data has a larger weighting than the input data. When LID is LOW, the output data has a smaller weighting than the input data. For instructions on how to use this feature, refer to the Applications section. Figure 5 shows an example of LID tied HIGH.

TABLE 1. INSTRUCTION TABLE

I_2	I_1	I_0	Function
L	L	L	Shift Left with Control Fill
L	L	H	Rotate Left
L	H	L	Insert Fill/Bypass (Note 1)
L	H	H	All Fill
H	L	L	Shift Right Two's Complement with Control Fill
H	L	H	Rotate Right Two's Complement
H	H	L	Shift Right Sign Magnitude with Control Fill
H	H	H	Rotate Right Sign Magnitude

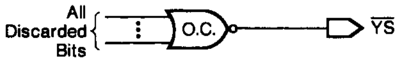
Key: H = HIGH
L = LOW

Notes: 1. Insert fill when $\overline{PI}$ is LOW; bypass when $\overline{PI}$ is HIGH.

TABLE 2. INPUT COMBINATION AND ENABLE FILL

Inputs						Outputs	
$\overline{OE_L}$	$\overline{OE_R}$	LID	I_2	I_1	I_0	Left Enable Fill	Right Enable Fill
L	L	OPEN	L	L	L	L	H
L	L	OPEN	H	X	L	H	L

Key: H = HIGH
L = LOW
X = Don't Care



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Sticky Bit Supports Pounding in Floating Point Operations

Figure 1. Sticky Bit Generator

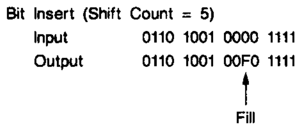

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Figure 2. Bit Insert Operation

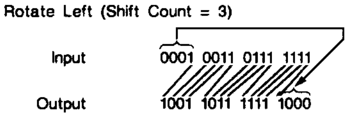

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Figure 3. Rotate Operation

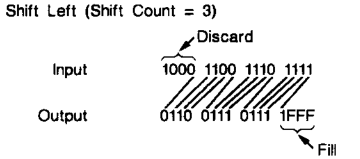

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Figure 4. Shift and Fill Operation

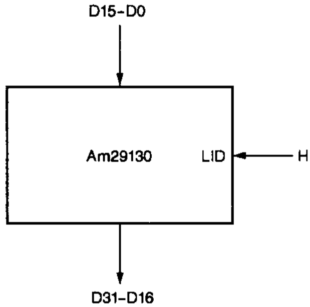

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Figure 5. Example of Location Identification

TABLE 3-1. INPUTS AND DATA OUTPUT COMBINATIONS
($I_2I_1I_0$ = 000, $\overline{OE_L} = \overline{OE_R}$ = L, LID = OPEN)

Inputs				Outputs															
S_3	S_2	S_1	S_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
L	L	L	L	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L	L	L	H	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	F
L	L	H	L	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	F	F
L	L	H	H	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	F	F	F
L	H	L	L	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	F	F	F	F
L	H	L	H	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	F	F	F	F	F
L	H	H	L	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	F	F	F	F	F	F
L	H	H	H	D8	D7	D6	D5	D4	D3	D2	D1	D0	F	F	F	F	F	F	F
H	L	L	L	D7	D6	D5	D4	D3	D2	D1	D0	F	F	F	F	F	F	F	F
H	L	L	H	D6	D5	D4	D3	D2	D1	D0	F	F	F	F	F	F	F	F	F
H	L	H	L	D5	D4	D3	D2	D1	D0	F	F	F	F	F	F	F	F	F	F
H	L	H	H	D4	D3	D2	D1	D0	F	F	F	F	F	F	F	F	F	F	F
H	H	L	L	D3	D2	D1	D0	F	F	F	F	F	F	F	F	F	F	F	F
H	H	L	H	D2	D1	D0	F	F	F	F	F	F	F	F	F	F	F	F	F
H	H	H	L	D1	D0	F	F	F	F	F	F	F	F	F	F	F	F	F	F
H	H	H	H	D0	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F

Key: H = HIGH
L = LOW
F = Fill

TABLE 3-2. INPUTS AND DATA OUTPUT COMBINATIONS ($I_2I_1I_0$ = 100, $\overline{OE_L} = \overline{OE_R}$ = L, LID = OPEN)

Inputs				Outputs															
S_3	S_2	S_1	S_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
L	L	L	L	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
L	L	L	H	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	D15
L	L	H	L	F	F	F	F	F	F	F	F	F	F	F	F	F	F	D15	D14
L	L	H	H	F	F	F	F	F	F	F	F	F	F	F	F	F	D15	D14	D13
L	H	L	L	F	F	F	F	F	F	F	F	F	F	F	F	D15	D14	D13	D12
L	H	L	H	F	F	F	F	F	F	F	F	F	F	F	D15	D14	D13	D12	D11
L	H	H	L	F	F	F	F	F	F	F	F	F	F	D15	D14	D13	D12	D11	D10
L	H	H	H	F	F	F	F	F	F	F	F	F	D15	D14	D13	D12	D11	D10	D9
H	L	L	L	F	F	F	F	F	F	F	F	D15	D14	D13	D12	D11	D10	D9	D8
H	L	L	H	F	F	F	F	F	F	F	D15	D14	D13	D12	D11	D10	D9	D8	D7
H	L	H	L	F	F	F	F	F	F	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6
H	L	H	H	F	F	F	F	F	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5
H	H	L	L	F	F	F	F	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4
H	H	L	H	F	F	F	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3
H	H	H	L	F	F	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2
H	H	H	H	F	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1

Key: H = HIGH
L = LOW
F = Fill

TABLE 3-3. INPUTS AND DATA OUTPUT COMBINATIONS ($I_2I_1I_0$ = X01, $\overline{OE_L} = \overline{OE_R}$ = L, LID = OPEN)

Inputs				Outputs															
S_3	S_2	S_1	S_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
L	L	L	L	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L	L	L	H	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15
L	L	H	L	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14
L	L	H	H	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13
L	H	L	L	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12
L	H	L	H	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11
L	H	H	L	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10
L	H	H	H	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9
H	L	L	L	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
H	L	L	H	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7
H	L	H	L	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6
H	L	H	H	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5
H	H	L	L	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4
H	H	L	H	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3
H	H	H	L	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2
H	H	H	H	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1

Key: H = HIGH
L = LOW
X = Don't Care

TABLE 3-4. INPUTS AND DATA OUTPUT COMBINATIONS
($I_2I_1I_0$ = 110, $\overline{OE_L} = \overline{OE_R}$ = L, LID = OPEN)

Inputs				Outputs															
S_3	S_2	S_1	S_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
L	L	L	L	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L	L	L	H	F	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
L	L	H	L	F	F	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2
L	L	H	H	F	F	F	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3
L	H	L	L	F	F	F	F	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4
L	H	L	H	F	F	F	F	F	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5
L	H	H	L	F	F	F	F	F	F	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6
L	H	H	H	F	F	F	F	F	F	F	D15	D14	D13	D12	D11	D10	D9	D8	D7
H	L	L	L	F	F	F	F	F	F	F	F	D15	D14	D13	D12	D11	D10	D9	D8
H	L	L	H	F	F	F	F	F	F	F	F	F	D15	D14	D13	D12	D11	D10	D9
H	L	H	L	F	F	F	F	F	F	F	F	F	F	D15	D14	D13	D12	D11	D10
H	L	H	H	F	F	F	F	F	F	F	F	F	F	F	D15	D14	D13	D12	D11
H	H	L	L	F	F	F	F	F	F	F	F	F	F	F	F	D15	D14	D13	D12
H	H	L	H	F	F	F	F	F	F	F	F	F	F	F	F	F	D15	D14	D13
H	H	H	L	F	F	F	F	F	F	F	F	F	F	F	F	F	F	D15	D14
H	H	H	H	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	D15

Key: H = HIGH
L = LOW
F = Fill

TABLE 3-5. INPUTS AND DATA OUTPUT COMBINATIONS
($I_2I_1I_0$ = 111, $\overline{OE_L} = \overline{OE_R}$ = L, LID = OPEN)

Inputs				Outputs															
S_3	S_2	S_1	S_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
L	L	L	L	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L	L	L	H	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
L	L	H	L	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2
L	L	H	H	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3
L	H	L	L	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4
L	H	L	H	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5
L	H	H	L	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6
L	H	H	H	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7
H	L	L	L	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8
H	L	L	H	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9
H	L	H	L	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10
H	L	H	H	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11
H	H	L	L	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12
H	H	L	H	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13
H	H	H	L	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14
H	H	H	H	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15

Key: H = HIGH
L = LOW

TABLE 3-6. INPUTS AND DATA OUTPUT COMBINATIONS
($I_2I_1I_0 = 000$, $\overline{OE_L} = H$, $\overline{OE_R} = L$, LID = L; $I_2I_1I_0 = 100$, $\overline{OE_L} = H$, $\overline{OE_R} = L$, LID = H)

Inputs				Outputs															
S_3	S_2	S_1	S_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
L	L	L	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	L	L	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	F
L	L	H	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	F	F
L	L	H	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	F	F	F
L	H	L	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	F	F	F	F
L	H	L	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	F	F	F	F	F
L	H	H	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	F	F	F	F	F	F
L	H	H	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	F	F	F	F	F	F	F
H	L	L	L	Z	Z	Z	Z	Z	Z	Z	Z	F	F	F	F	F	F	F	F
H	L	L	H	Z	Z	Z	Z	Z	Z	Z	F	F	F	F	F	F	F	F	F
H	L	H	L	Z	Z	Z	Z	Z	Z	F	F	F	F	F	F	F	F	F	F
H	L	H	H	Z	Z	Z	Z	Z	F	F	F	F	F	F	F	F	F	F	F
H	H	L	L	Z	Z	Z	Z	F	F	F	F	F	F	F	F	F	F	F	F
H	H	L	H	Z	Z	Z	F	F	F	F	F	F	F	F	F	F	F	F	F
H	H	H	L	Z	Z	F	F	F	F	F	F	F	F	F	F	F	F	F	F
H	H	H	H	Z	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F

Key: H = HIGH
L = LOW
F = Fill
Z = Disabled

TABLE 3-7. INPUTS AND DATA OUTPUT COMBINATIONS
($I_2I_1I_0 = 000$, $\overline{OE_L} = L$, $\overline{OE_R} = H$, LID = L; $I_2I_1I_0 = 100$, $\overline{OE_L} = L$, $\overline{OE_R} = H$, LID = H)

Inputs				Outputs															
S_3	S_2	S_1	S_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
L	L	L	L	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
L	L	L	H	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	Z
L	L	H	L	F	F	F	F	F	F	F	F	F	F	F	F	F	F	Z	Z
L	L	H	H	F	F	F	F	F	F	F	F	F	F	F	F	F	Z	Z	Z
L	H	L	L	F	F	F	F	F	F	F	F	F	F	F	F	Z	Z	Z	Z
L	H	L	H	F	F	F	F	F	F	F	F	F	F	F	Z	Z	Z	Z	Z
L	H	H	L	F	F	F	F	F	F	F	F	F	F	Z	Z	Z	Z	Z	Z
L	H	H	H	F	F	F	F	F	F	F	F	F	Z	Z	Z	Z	Z	Z	Z
H	L	L	L	F	F	F	F	F	F	F	F	Z	Z	Z	Z	Z	Z	Z	Z
H	L	L	H	F	F	F	F	F	F	F	Z	Z	Z	Z	Z	Z	Z	Z	Z
H	L	H	L	F	F	F	F	F	F	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
H	L	H	H	F	F	F	F	F	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
H	H	L	L	F	F	F	F	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
H	H	L	H	F	F	F	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
H	H	H	L	F	F	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
H	H	H	H	F	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Key: H = HIGH
L = LOW
F = Fill
Z = Disabled

TABLE 3-8. INPUTS AND DATA OUTPUT COMBINATIONS
($I_2I_1I_0$ = 100, $\overline{OE_L}$ = H, $\overline{OE_R}$ = L, LID = L; $I_2I_1I_0$ = 000, $\overline{OE_L}$ = H, $\overline{OE_R}$ = L, LID = H; $I_2I_1I_0$ = X01, $\overline{OE_L}$ = H, $\overline{OE_R}$ = L, LID = X)

Inputs				Outputs															
S_3	S_2	S_1	S_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
L	L	L	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	L	L	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	D15
L	L	H	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	D15	D14
L	L	H	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	D15	D14	D13
L	H	L	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	D15	D14	D13	D12
L	H	L	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	D15	D14	D13	D12	D11
L	H	H	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	D15	D14	D13	D12	D11	D10
L	H	H	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	D15	D14	D13	D12	D11	D10	D9
H	L	L	L	Z	Z	Z	Z	Z	Z	Z	Z	D15	D14	D13	D12	D11	D10	D9	D8
H	L	L	H	Z	Z	Z	Z	Z	Z	Z	D15	D14	D13	D12	D11	D10	D9	D8	D7
H	L	H	L	Z	Z	Z	Z	Z	Z	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6
H	L	H	H	Z	Z	Z	Z	Z	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5
H	H	L	L	Z	Z	Z	Z	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4
H	H	L	H	Z	Z	Z	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3
H	H	H	L	Z	Z	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2
H	H	H	H	Z	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1

Key: H = HIGH
L = LOW
X = Don't Care
Z = Disabled

TABLE 3-9. INPUTS AND DATA OUTPUT COMBINATIONS
($I_2I_1I_0$ = 100, $\overline{OE_L}$ = L, $\overline{OE_R}$ = H, LID = L; $I_2I_1I_0$ = 000, $\overline{OE_L}$ = L, $\overline{OE_R}$ = H, LID = H; $I_2I_1I_0$ = X01, $\overline{OE_L}$ = L, $\overline{OE_R}$ = H, LID = X)

Inputs				Outputs															
S_3	S_2	S_1	S_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
L	L	L	L	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L	L	L	H	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Z
L	L	H	L	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Z	Z
L	L	H	H	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Z	Z	Z
L	H	L	L	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Z	Z	Z	Z
L	H	L	H	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Z	Z	Z	Z	Z
L	H	H	L	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Z	Z	Z	Z	Z	Z
L	H	H	H	D8	D7	D6	D5	D4	D3	D2	D1	D0	Z	Z	Z	Z	Z	Z	Z
H	L	L	L	D7	D6	D5	D4	D3	D2	D1	D0	Z	Z	Z	Z	Z	Z	Z	Z
H	L	L	H	D6	D5	D4	D3	D2	D1	D0	Z	Z	Z	Z	Z	Z	Z	Z	Z
H	L	H	L	D5	D4	D3	D2	D1	D0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
H	L	H	H	D4	D3	D2	D1	D0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
H	H	L	L	D3	D2	D1	D0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
H	H	L	H	D2	D1	D0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
H	H	H	L	D1	D0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
H	H	H	H	D0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Key: H = HIGH
L = LOW
X = Don't Care
Z = Disabled

TABLE 3-10. INPUTS AND DATA OUTPUT COMBINATIONS
($I_2I_1I_0$ = 110, $\overline{OE_L}$ = L, $\overline{OE_R}$ = H, LID = L;
$I_2I_1I_0$ = 111, $\overline{OE_L}$ = L, $\overline{OE_R}$ = H, LID = X)

Inputs				Outputs															
S_3	S_2	S_1	S_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
L	L	L	L	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L	L	L	H	D0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	L	H	L	D1	D0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	L	H	H	D2	D1	D0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	H	L	L	D3	D2	D1	D0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	H	L	H	D4	D3	D2	D1	D0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	H	H	L	D5	D4	D3	D2	D1	D0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	H	H	H	D6	D5	D4	D3	D2	D1	D0	Z	Z	Z	Z	Z	Z	Z	Z	Z
H	L	L	L	D7	D6	D5	D4	D3	D2	D1	D0	Z	Z	Z	Z	Z	Z	Z	Z
H	L	L	H	D8	D7	D6	D5	D4	D3	D2	D1	D0	Z	Z	Z	Z	Z	Z	Z
H	L	H	L	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Z	Z	Z	Z	Z	Z
H	L	H	H	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Z	Z	Z	Z	Z
H	H	L	L	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Z	Z	Z	Z
H	H	L	H	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Z	Z	Z
H	H	H	L	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Z	Z
H	H	H	H	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Z

Key: H = HIGH
L = LOW
X = Don't Care
Z = Disabled

TABLE 3-11. INPUTS AND DATA OUTPUT COMBINATIONS
($I_2I_1I_0$ = 110, $\overline{OE_L}$ = H, $\overline{OE_R}$ = L, LID = L;
$I_2I_1I_0$ = 111, $\overline{OE_L}$ = H, $\overline{OE_R}$ = L, LID = X)

Inputs				Outputs															
S_3	S_2	S_1	S_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
L	L	L	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	L	L	H	Z	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
L	L	H	L	Z	Z	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2
L	L	H	H	Z	Z	Z	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3
L	H	L	L	Z	Z	Z	Z	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4
L	H	L	H	Z	Z	Z	Z	Z	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5
L	H	H	L	Z	Z	Z	Z	Z	Z	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6
L	H	H	H	Z	Z	Z	Z	Z	Z	Z	D15	D14	D13	D12	D11	D10	D9	D8	D7
H	L	L	L	Z	Z	Z	Z	Z	Z	Z	Z	D15	D14	D13	D12	D11	D10	D9	D8
H	L	L	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	D15	D14	D13	D12	D11	D10	D9
H	L	H	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	D15	D14	D13	D12	D11	D10
H	L	H	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	D15	D14	D13	D12	D11
H	H	L	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	D15	D14	D13	D12
H	H	L	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	D15	D14	D13
H	H	H	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	D15	D14
H	H	H	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	D15

Key: H = HIGH
L = LOW
X = Don't Care
Z = Disabled

TABLE 3-12. INPUTS AND DATA OUTPUT COMBINATIONS
($I_2I_1I_0$ = 110, $\overline{OE_L}$ = L, $\overline{OE_R}$ = H, LID = H)

Inputs				Outputs															
S_3	S_2	S_1	S_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
L	L	L	L	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
L	L	L	H	F	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	L	H	L	F	F	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	L	H	H	F	F	F	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	H	L	L	F	F	F	F	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	H	L	H	F	F	F	F	F	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	H	H	L	F	F	F	F	F	F	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	H	H	H	F	F	F	F	F	F	F	Z	Z	Z	Z	Z	Z	Z	Z	Z
H	L	L	L	F	F	F	F	F	F	F	F	Z	Z	Z	Z	Z	Z	Z	Z
H	L	L	H	F	F	F	F	F	F	F	F	F	Z	Z	Z	Z	Z	Z	Z
H	L	H	L	F	F	F	F	F	F	F	F	F	F	Z	Z	Z	Z	Z	Z
H	L	H	H	F	F	F	F	F	F	F	F	F	F	F	Z	Z	Z	Z	Z
H	H	L	L	F	F	F	F	F	F	F	F	F	F	F	F	Z	Z	Z	Z
H	H	L	H	F	F	F	F	F	F	F	F	F	F	F	F	F	Z	Z	Z
H	H	H	L	F	F	F	F	F	F	F	F	F	F	F	F	F	F	Z	Z
H	H	H	H	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	Z

Key: H = HIGH
L = LOW
F = Fill
Z = Disabled

TABLE 3-13. INPUTS AND DATA OUTPUT COMBINATIONS
($I_2I_1I_0$ = 110, $\overline{OE_L}$ = H, $\overline{OE_R}$ = L, LID = H)

Inputs				Outputs															
S_3	S_2	S_1	S_0	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
L	L	L	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
L	L	L	H	Z	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
L	L	H	L	Z	Z	F	F	F	F	F	F	F	F	F	F	F	F	F	F
L	L	H	H	Z	Z	Z	F	F	F	F	F	F	F	F	F	F	F	F	F
L	H	L	L	Z	Z	Z	Z	F	F	F	F	F	F	F	F	F	F	F	F
L	H	L	H	Z	Z	Z	Z	Z	F	F	F	F	F	F	F	F	F	F	F
L	H	H	L	Z	Z	Z	Z	Z	Z	F	F	F	F	F	F	F	F	F	F
L	H	H	H	Z	Z	Z	Z	Z	Z	Z	F	F	F	F	F	F	F	F	F
H	L	L	L	Z	Z	Z	Z	Z	Z	Z	Z	F	F	F	F	F	F	F	F
H	L	L	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	F	F	F	F	F	F	F
H	L	H	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	F	F	F	F	F	F
H	L	H	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	F	F	F	F	F
H	H	L	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	F	F	F	F
H	H	L	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	F	F	F
H	H	H	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	F	F
H	H	H	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	F

Key: H = HIGH
L = LOW
F = Fill
Z = Disabled

TABLE 3-14. INPUTS AND DATA OUTPUT COMBINATIONS ($I_2I_1I_0$ = 010, $\overline{OE_L}$ = X, $\overline{OE_R}$ = X, LID = OPEN)

Inputs					Outputs															
S_3	S_2	S_1	S_0	$\overline{PI}$	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
L	L	L	L	L	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	F
L	L	L	H	L	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	F	D0
L	L	H	L	L	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	F	D1	D0
L	L	H	H	L	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	F	D2	D1	D0
L	H	L	L	L	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	F	D3	D2	D1	D0
L	H	L	H	L	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	F	D4	D3	D2	D1	D0
L	H	H	L	L	D15	D14	D13	D12	D11	D10	D9	D8	D7	F	D5	D4	D3	D2	D1	D0
L	H	H	H	L	D15	D14	D13	D12	D11	D10	D9	D8	F	D6	D5	D4	D3	D2	D1	D0
H	L	L	L	L	D15	D14	D13	D12	D11	D10	D9	F	D7	D6	D5	D4	D3	D2	D1	D0
H	L	L	H	L	D15	D14	D13	D12	D11	D10	F	D8	D7	D6	D5	D4	D3	D2	D1	D0
H	L	H	L	L	D15	D14	D13	D12	D11	F	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
H	L	H	H	L	D15	D14	D13	D12	F	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
H	H	L	L	L	D15	D14	D13	F	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
H	H	L	H	L	D15	D14	F	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
H	H	H	L	L	D15	F	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
H	H	H	H	L	F	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	H	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Key: H = HIGH
L = LOW
F = Fill
X = Don't Care

Note: When $I_2I_1I_0$ = 010, $\overline{OE}_L = \overline{OE}_R$ = X, LID = H or L, the outputs $Y_{15} - Y_0$ are in three state.

APPLICATIONS

Using with Am29C101

The Am29130 and Am29C101 are in series in the critical paths (Figure 6). The data is operated on through Am29130 after ALU operation. This is the recommended architecture for Am29130.

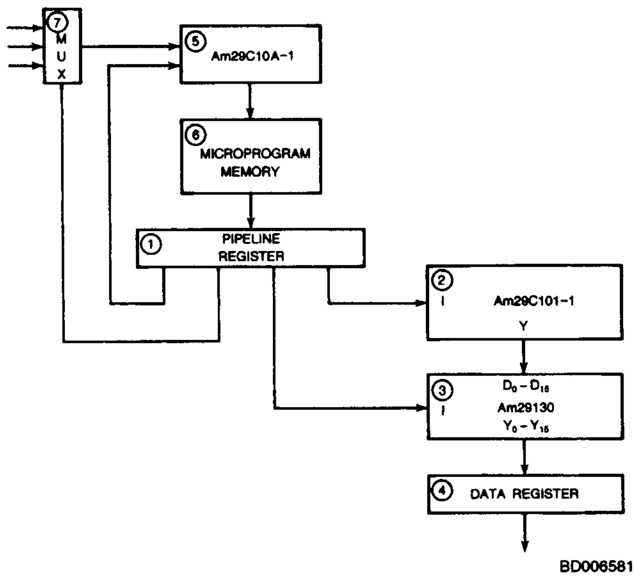


Figure 6. Am29C101-Based Architecture with Am29130

The minimum cycle time for this architecture is roughly 94 ns based on the following calculation:

Data Path

1	Register	CP – Q	11 ns
2	Am29C101-1	A – Y, C_{n+16}, OVR	37 ns
3	Am29130	D – Y	28 ns
4	Register	Setup Time	4 ns
			80 ns

Control Path

1	Register	CP – Q	11 ns
7	MUX		18 ns
5	Am29C10A-1		26 ns
6	PROM		35 ns
1	Register	Setup Time	4 ns
			94 ns

Figure 7 shows the detailed interconnection around Am29130. Notice that the sign bit of the shift count number is connected to I_2 of Am29130 to control left or right shift. The instruction bits and $\overline{PI}$ come from the pipeline register. The fill bit can be either 0, 1, or the sign bit of the data input.

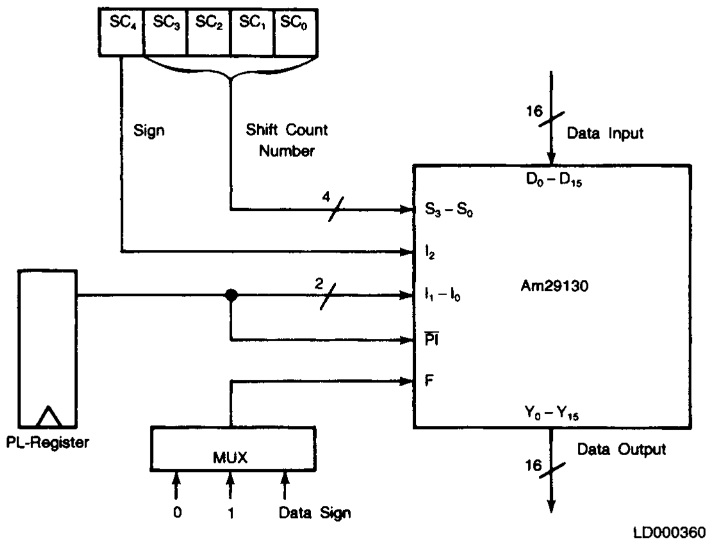


Figure 7. Am29130 System Interconnection

Using Am29130 as a 32-Bit Barrel Shifter

Four Am29130s can be used as a 32-bit barrel shifter without any inherent speed penalty. Figure 8 shows the block diagram for this scheme. LIDs for parts A_1 and A_2 are left open as these parts have unshifted weighting between the inputs and outputs. Part B_1 has the output data with a larger weighting than the input data; therefore, LID is tied HIGH. Part B_2 has the output data with a smaller weighting than the input data; therefore, LID is tied LOW.

The control logic controls the output control and polarity/insert pin of each part, as shown in Figure 8. These control outputs are produced by $I_0 - I_2$, S, $\overline{PI}$, and $\overline{EN}$, which come from the pipeline register. The control logic can be realized either by random logic or by PALs, depending on functional requirement and application. The truth table to realize the logic is described in Table 4.

Using Tables 3-1 through 3-14, one can realize the complete function of Am29130 for a 32-bit barrel shifter. Figure 9 shows an example of rotate left operation with the shift count 3. It points to the pertinent tables for each of the four Am29130s. The slashed area shows the left or right output that is enabled. Notice that part A_1 has the left output enabled, whereas B_1 has the right output enabled. Figures 10 through 12 give examples of the shift left/right, and the insert fill operations. Tables 5 and 6 give cross references for Tables 3-1 through 3-14 for 32-bit shifter.

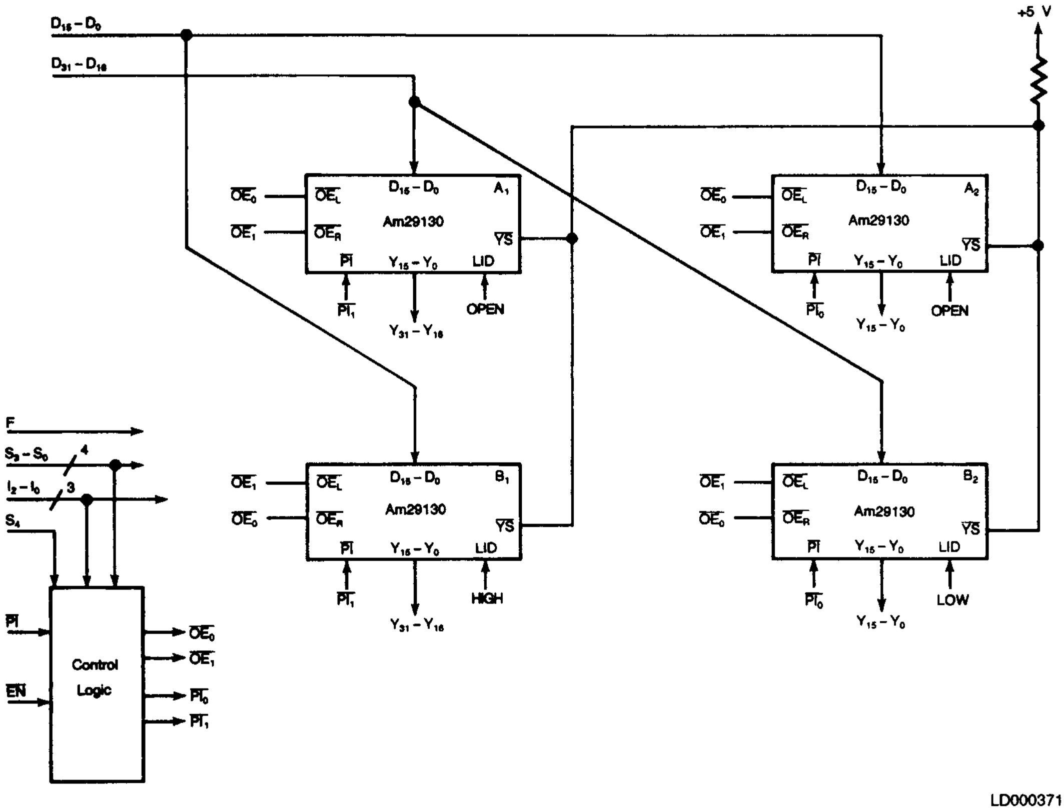


Figure 8. 32-Bit Shifting with Four Am29130s and External Control Logic

TABLE 4. TRUTH TABLE FOR 32-BIT BARREL SHIFTER

Inputs								Outputs			
$\overline{EN}$	I_2	I_1	I_0	S_3	S_2	S_1	S_0	$\overline{OE_0}$	$\overline{OE_1}$	$\overline{PI_0}$	$\overline{PI_1}$
L	L	L	X	X	X	X	X	S_4	$\overline{S_4}$	$\overline{PI}$	$\overline{PI}$
L	L	H	L	X	X	X	X	X (Note 1)	X	S_4	$\overline{S_4}$
L	L	H	H	X	X	X	X	X (Note 1)	X	$\overline{PI}$	$\overline{PI}$
L	H	L	X	X	X	X	X	S_4	$\overline{S_4}$	$\overline{PI}$	$\overline{PI}$
L	H	H	X	L	L	L	L	S_4	$\overline{S_4}$	$\overline{PI}$	$\overline{PI}$
				All Others				$\overline{S_4}$	S_4	$\overline{PI}$	$\overline{PI}$
H	H	X	X	X	X	X	X	H	H	X	X

Key: H = HIGH
L = LOW
X = Don't Care

Notes: 1. For this instruction, when LID is either HIGH or LOW, Y outputs are three stated. Therefore, parts B_1 and B_2 in Figure 8 are disabled.

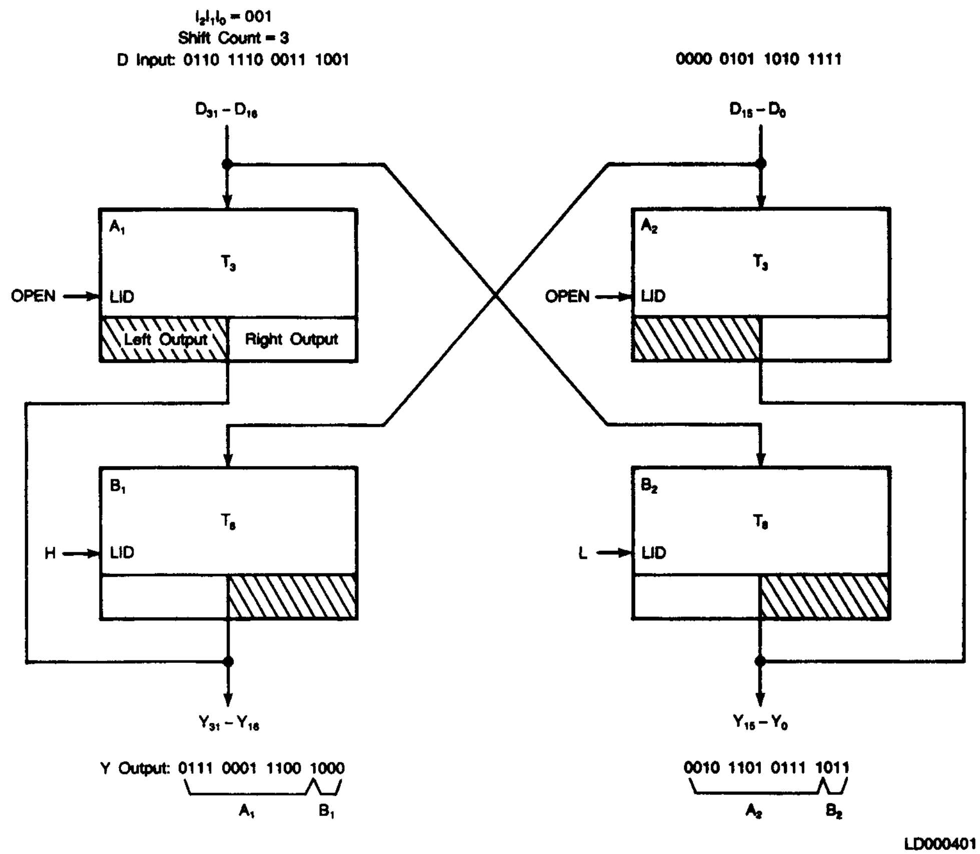


Figure 9. Example of the 32-Bit Rotate Left Operation

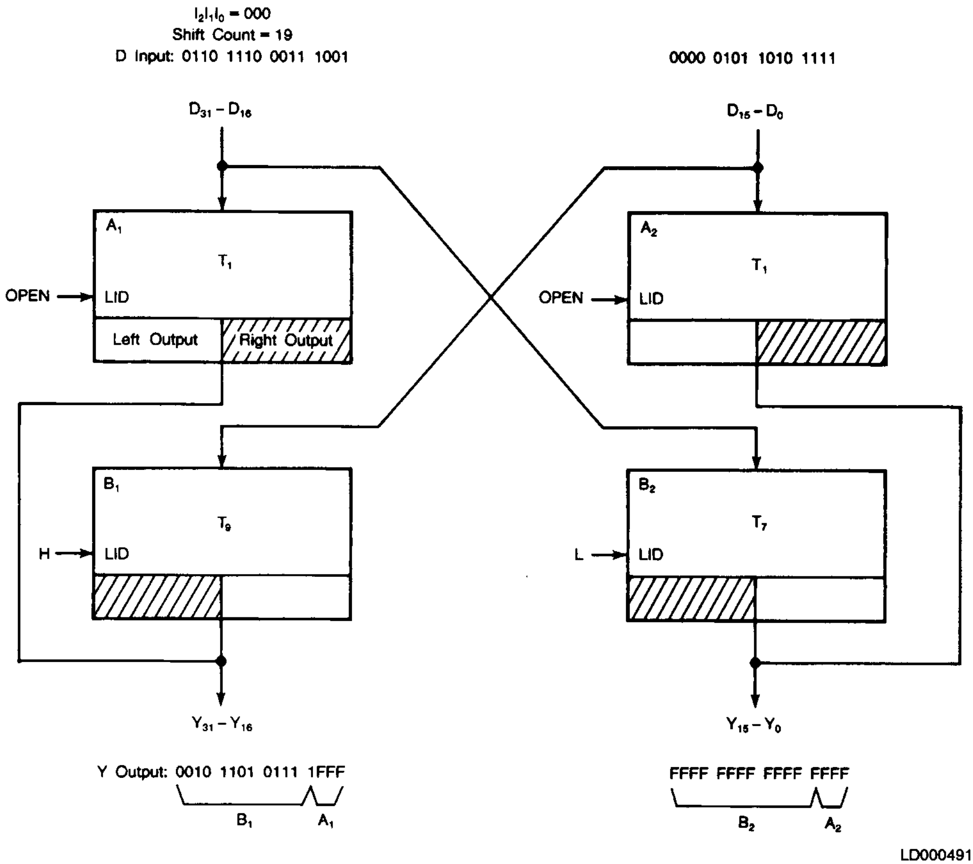


Figure 10. Example of the 32-Bit Shift Left with Fill Operation

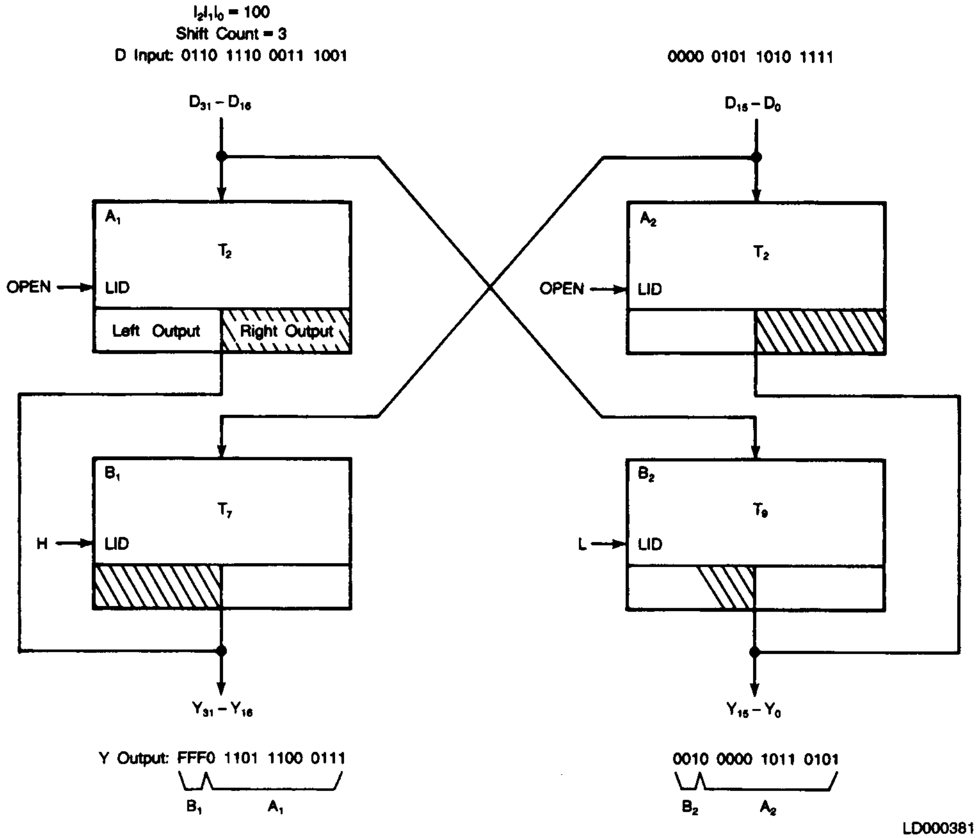


Figure 11. Example of Shift Right Two's Complement with Fill Operation

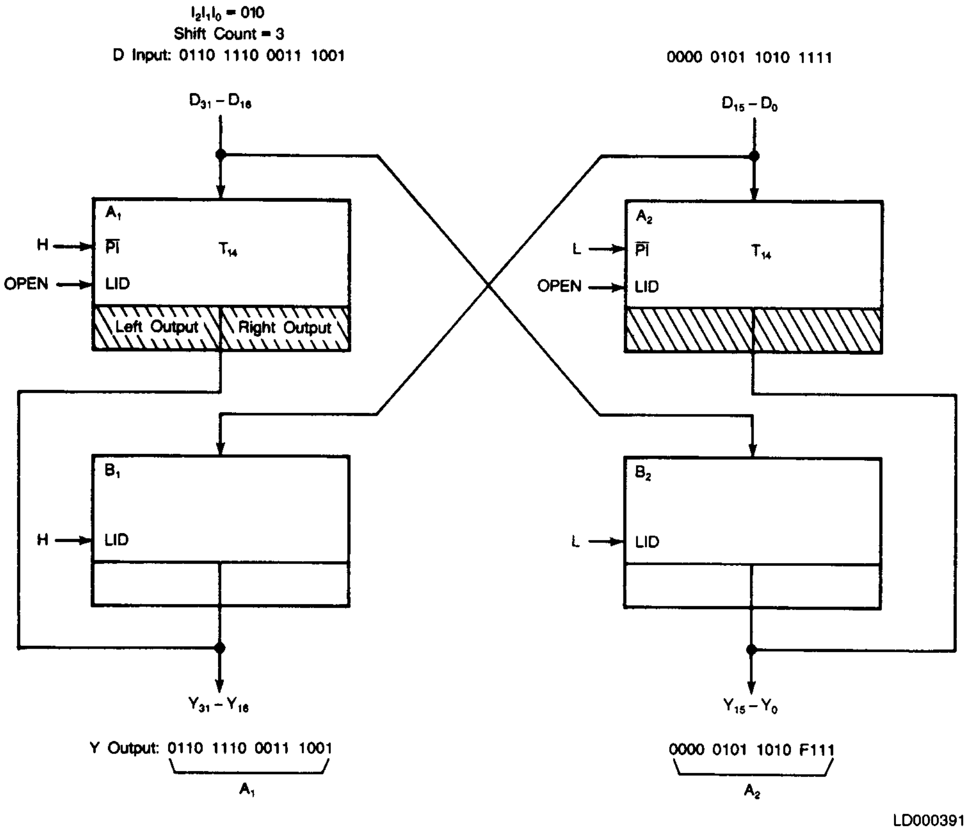


Figure 12. Example of 32-Bit Insert Fill Operation

TABLE 5. TABLE CROSS REFERENCE FOR 32-BIT OPERATIONS #1

Inputs				Outputs								Comments
				A_1		A_2		B_1		B_2		
I_2	I_1	I_0	S_4	LD	RD	LD	RD	LD	RD	LD	RD	
L	L	L	L	T1		T1			T8		T6	
			H		T1		T1	T9		T7		
L	L	H	L	T3		T3			T8		T8	
			H		T3		T3	T9		T9		
L	H	X	X	Both LD and RD from A_1 and A_2								
H	L	L	L	T2		T2			T6		T8	
			H		T2		T2	T7		T9		
H	L	H	L	T3		T3			T8		T8	
			H		T3		T3	T9		T9		
H	H	L	L	T4		T4						For $S_3 = S_2 = S_1 = S_0 = L$
			H					T12		T10		
			L		T4		T4	T12		T10		For Other Combinations
			H	T4		T4			T13		T11	
H	H	H	L	T5		T5						For $S_3 = S_2 = S_1 = S_0 = L$
			H					T10		T10		
			L		T5		T5	T10		T10		For Other Combinations
			H	T5		T5			T11		T11	

Key: LD = Left Output
RD = Right Output
H = HIGH
L = LOW
X = Don't Care

Notes: 1. T1 stands for Table 3-1
2. Example from row 1:
Output $Y_{31} - Y_{16}$ can be obtained by combining "LD of A_1" which is "LD of T1" with "RD of B_1" which is "RD of T8." Similarly, output $Y_{15} - Y_0$ can be obtained from "LD of A_2" and "RD of B_2."

TABLE 6. TABLE CROSS REFERENCE FOR 32-BIT OPERATIONS #2

Inputs						Outputs	Comments
I_2	I_1	I_0	LID	$\overline{OE}_L$	$\overline{OE}_R$	Tables	
L	L	L	OPEN	L	L	T1	
			L	H	L	T6	
			L	L	H	T7	
			H	H	L	T8	
			H	L	H	T9	
L	L	H	OPEN	L	L	T3	
			X	H	L	T8	
			X	L	H	T9	
L	H	L	OPEN	X	X	T14	
			L or H	X	X		$Y_{15}-Y_0$ are in three state
L	H	H	OPEN	X	X		$Y_{15}-Y_0$ = F,
			L or H	X	X		$Y_{15}-Y_0$ are in three state
H	L	L	OPEN	L	L	T2	
			L	H	L	T8	
			L	L	H	T9	
			H	H	L	T6	
			H	L	H	T7	
H	L	H	OPEN	L	L	T3	
			X	H	L	T8	
			X	L	H	T9	
H	H	L	OPEN	L	L	T4	
			L	H	L	T11	
			L	L	H	T10	
			H	H	L	T13	
			H	L	H	T12	
H	H	H	OPEN	L	L	T5	
			X	L	H	T10	
			X	H	L	T11	

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Ambient Temperature
  Under Bias .... −55 to +125°C
Supply Voltage to Ground Potential
  (Pin 16 to Pin 8) Continuous .... −0.5 to +7.0 V
DC Voltage Applied to Outputs for
  HIGH Output State ....−0.5 V to $+V_{CC}$ Max.
DC Input Voltage .... −0.5 V to +5.5 V
DC Output Current, Into Outputs .... 30 mA
DC Input Current .... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
  Temperature (T_A) .... 0 to +70°C
  Supply Voltage (V_{CC}) .... +4.75 V to +5.25 V

Military* (M) Devices
  Temperature (T_C) .... −55°C to +125°C
  Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

SD 048 Thermal Resistance (Typical)
  θ_{JC} = 10°C/W
  θ_{JA} = 40°C/W

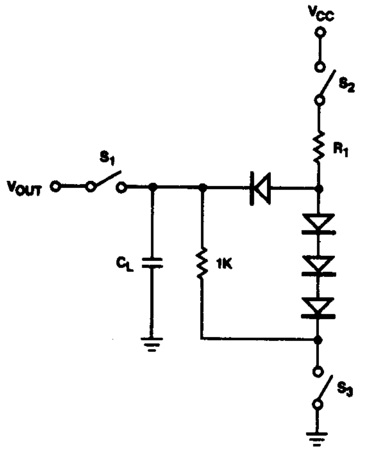
*Military Product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating ranges unless otherwise specified; Included in Group A, Subgroup 1, 2, 3 tests unless otherwise noted.

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	COM'L I_{OL} = 16 mA		0.5	V
			MIL I_{OL} = 12 mA		0.5	
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs Except LID		2.0		V
		For LID (Note 1)		4.5		
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA			−1.2	V
I_{IL}	Input LOW Current	For S_0, S_1, and I_1, V_{CC} = Max., V_{IN} = 0.5 V			−1.0	mA
		For LID, V_{CC} = Max., V_{IN} = 0.0 V			−5.0	
		For All Others, V_{CC} = Max., V_{IN} = 0.5 V			−0.5	
I_{IH}	Input HIGH Current	For S_0, S_1, and I_1, V_{CC} = Max., V_{IN} = 2.4 V			100	µA
		For LID, V_{CC} = Max., V_{IN} = V_{CC} (Max.)			5.0	mA
		For All Others, V_{CC} = Max., V_{IN} = 2.4 V			50	µA
I_{CEX}	Output Leakage Current for $\overline{YS}$ only	V_{CC} = Min., V_{OH} = 5.5 V			250	µA
I_I	Input HIGH Current	For LID, V_{CC} = Max., V_{IN} = 5.5 V			5.0	mA
		For All Others, V_{CC} = Max., V_{IN} = 5.5 V			1.0	
I_{OZH}	Off State	V_{CC} = Max.	V_O = 2.4 V		50	µA
I_{OZL}	Output Current		V_O = 0.5 V		−50	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_O = 0.5 V (Note 2)		−15	−50	mA
I_{CC}	Power Supply Current	V_{CC} = Max.	T_A = 0 to +70°C		270	mA
			T_A = +70°C		250	
			T_C = −55 to +125°C		300	
			T_C = +125°C		250	

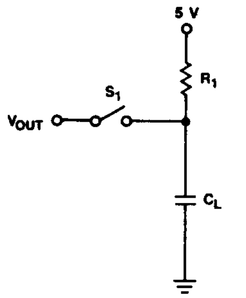
Notes: 1. LID has three levels. $V_{IH} = V_{CC}$, $V_{IL} < 0.8$ V, and OPEN.
2. No more than one output should be tested at a time. Duration of short-circuit test should not exceed one second.

SWITCHING TEST CIRCUITS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

A. Three-State Outputs



$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

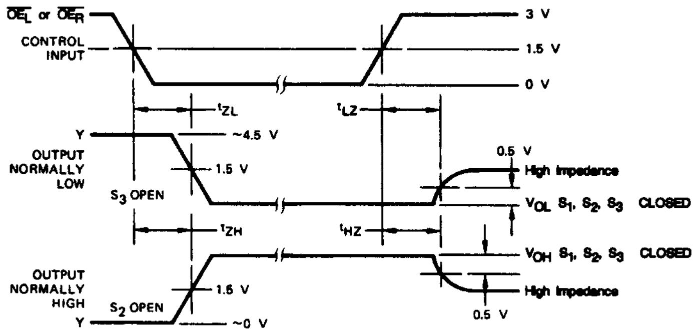
B. Open-Collector Outputs

Notes: 1. $C_L = 50$ pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. $C_L = 5.0$ pF for output disable tests.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified; Included in Group A, Subgroup 9, 10, 11 tests unless otherwise noted for all APL products.

No.	Parameter Symbol	Parameter Description	Test Conditions	Com. Min.	Com. Max.	Mil. Min.	Mil. Max.	Units
1	t_{DO}	D to Y	See Switching Test Circuit A		28		33	ns
2	t_{FO}	F to Y			28		33	
3	t_{SO}	$S_0 - S_3$ to Y			30		35	ns
4	t_{IO}	$I_0 - I_2$ to Y			30		35	ns
5	$t_{\overline{PIO}}$	$\overline{PI}$ to Y			30		35	ns
6	t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ}	$\overline{OE_L}$, $\overline{OE_R}$ to Y			29		35	ns
7	t_{IOS}	$I_0 - I_2$ to $\overline{YS}$	See Switching Test Circuit B		35		40	ns
8	t_{DOS}	D to $\overline{YS}$			35		40	ns

SWITCHING TEST WAVEFORMS



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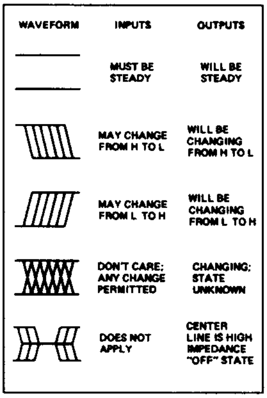
SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS



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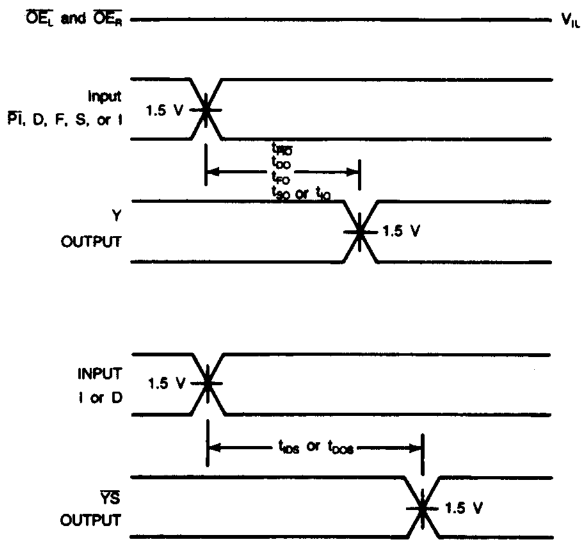

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Test Philosophy and Methods

The following points give the general philosophy which we apply to tests which must be properly engineered if they are to be implemented in an automatic enviroment. The specifics of what philosophies applied to which test are shown in the data sheet.

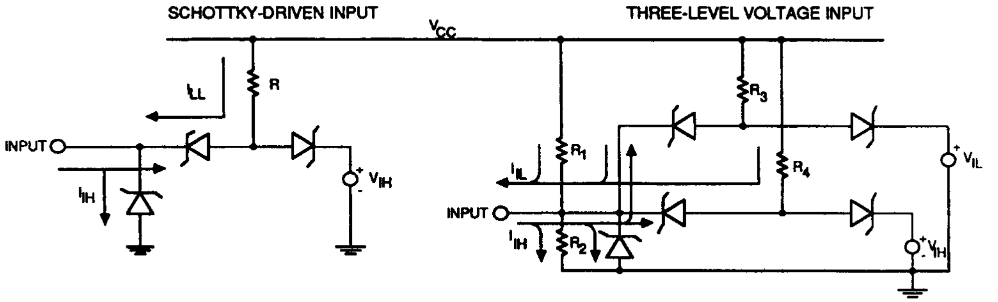
1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an output transition, ground current may change by as much as 400 mA in 5-8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0$ V and $V_{IH} \geq 3.0$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. Capacitive Loading for A.C. Testing
   Automatic testers and their associated hardware have stray capacitance which varies from one type of tester to another but is generally around 60 pF. This, of course, makes it impossible to make direct measurements of parameters which call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays" which measure the propagation delays into the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF) and engineering correlations based on data taken with a bench setup are used to predict the result at the lower capacitance.

   Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impossible to make measurements at both capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is predicted from engineering correlations based on data taken with a bench set up and the knowledge that certain D.C. measurements (I_{OH}, I_{OL}, for example) have already been taken and are within spec. In some cases, special D.C. tests are performed in order to facilitate this correlation.
7. Threshold Testing
   The noise associated with automatic testing (due to the long, inductive cables) and the high gain of the tested device when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed test system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and A.C. testing are performed at "hard" input levels rather than at V_{IL} Max. and V_{IH} Min.
8. A.C. Testing
   Occasionally, parameters are specified which cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other A.C. tests which have been performed. These correlations are arrived at by the cognizant engineer by using data from precise bench measurements in conjunction with the knowledge that certain D.C. parameters have already been measured and are within spec.

   In some cases, certain A.C. tests are redundant since they can be shown to be predicted by other tests which have already been performed. In these cases, the redundant tests are not performed.
9. Output Short-Circuit Current Testing
   When performing I_{OS} tests on devices containing RAM or registers, great care must be taken that undershoot caused by grounding the high-state output does not trigger parasitic elements which in turn cause the device to change state. In order to avoid this effect, it is common to make the measurement at a voltage (V_{output}) that is slightly above ground. The V_{CC} is raised by the same amount so that the result (as confirmed by Ohm's law and precise bench testing) is identical to the $V_{OUT} = 0$, V_{CC} = Max. case.

INPUT/OUTPUT CIRCUIT DIAGRAMS

TTL Input/Output Current Interfaces

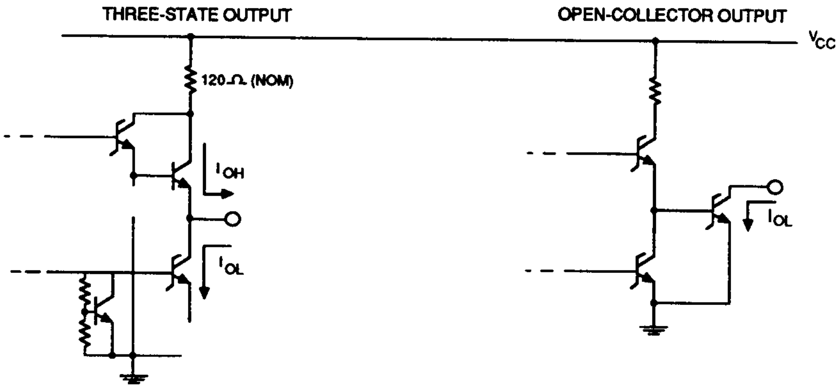


R = 25K, for all inputs except LID

	LID
R_1	3K
R_2	3K
R_3	9K
R_4	30K

TC004050

$C_I \cong 5.0$ pF, all inputs



Y_{0-15} OUTPUTS

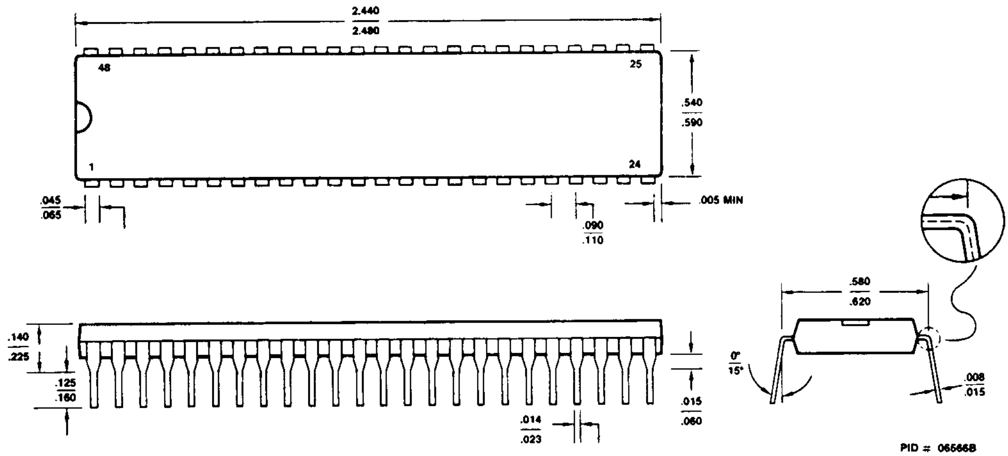
$\overline{YS}$ OUTPUT

TC004060

$C_O \cong 5.0$ pF, all outputs

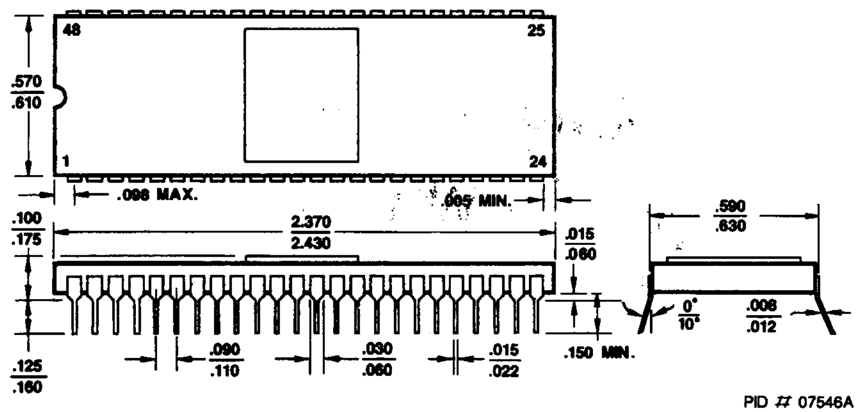
PHYSICAL DIMENSIONS*

PD 048



PID # 06566B

SD 048



PID # 07546A

*For reference only.

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