3.5" R/W MOD Read Channel Back-end Processor

GENERAL DESCRIPTION

The ML6013 is a Read Channel Back-end processor for 3.5" Rewritable Magneto-Optical drives (MOD). It works in conjunction with the ML6012 Read Channel Front-end chip to form a complete integrated Read Channel solution for 128M and 230M MOD drives supporting the ISO standards. It incorporates a full function data synchronizer with a 3:1 operating range, a full function frequency synthesizer with onboard M & N dividers. The most critical blocks on this chip are the three VCOs, one for the data synchronizer PLL, one for the frequency synthesizer PLL and the third VCO is used to generate the tracking 1/4 cell delay for (2, 7) RLL data synchronization. Careful design considerations have been incorporated to minimize the noise coupling and crosstalk among the VCOs. The system noise is highly minimized as the VCO operates at only 2X the data rate.

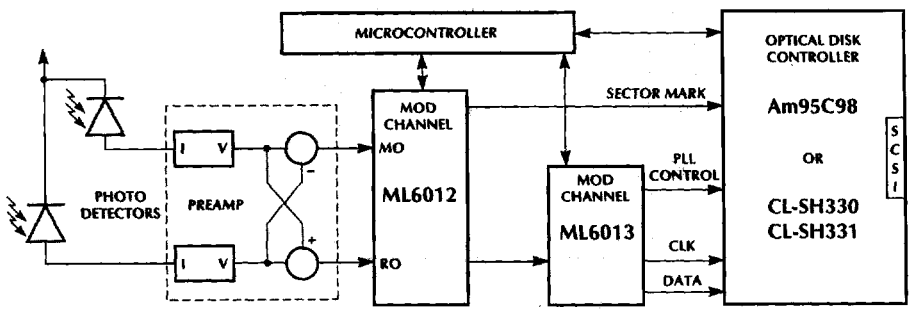
It provides 40-bits for user programmability of a number of features through a serial microprocessor interface and a bank of internal control registers. The center frequency of the VCO, window centering, M & N dividers and power management options are programmable.

The ML6013 has a typical power dissipation of 350mW in normal mode, and less than 1mW in power down mode. The ML6013 has four levels of power management control for maximum flexibility.

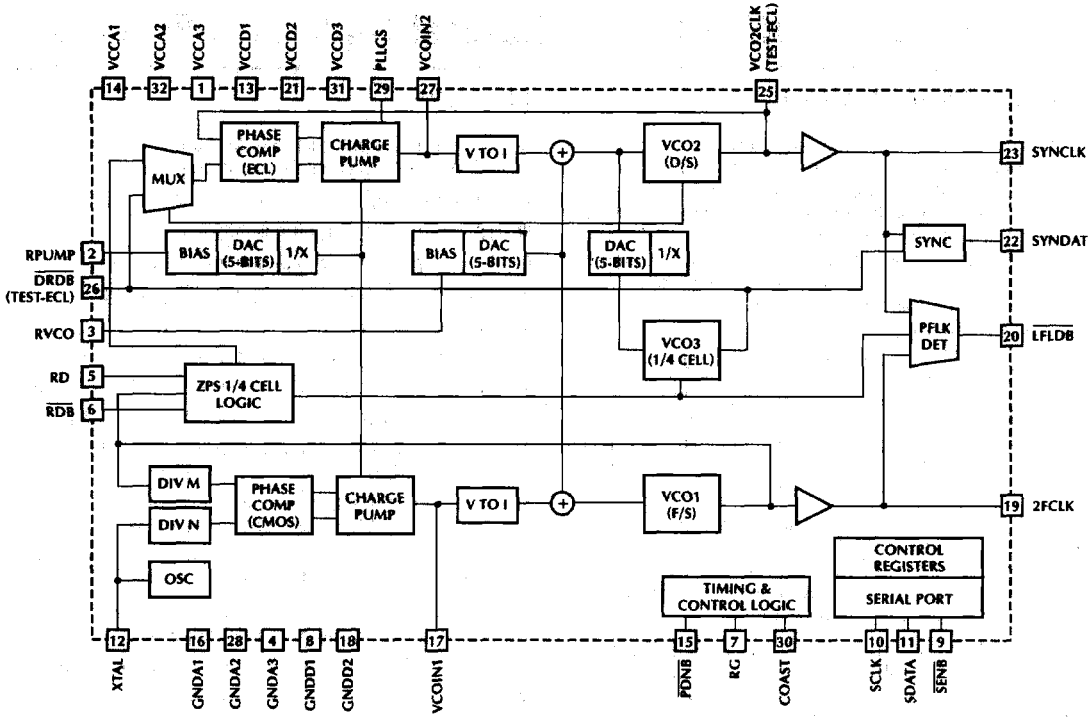
FEATURES

- Supports ISO standards for 128M and 230M R/W Magneto-Optical Drive (MOD)
- Operating supply range 4.5V to 5.5V
- Typical power dissipation is 300mW
- Sleep mode power dissipation less than 1mW
- Low profile, small area, 32-pin TQFP package
- 3:1 NRZ data rate range — 8 to 24 Mbits/s
- Fast acquisition PLL with zero phase start capability
- 3:1 VCO tuning range with 48 Mbits/s 2, 7RLL code rate
- Tracking 1/4 cell delay for handling 2, 7 RLL data
- Programmable VCO center frequency and window centering adjustment (±25% in steps of 1.6%)
- PLL based frequency synthesizer with reference crystal oscillator and M (7-bit) & N (7-bit) dividers
- High speed (20MHz) three wire serial microprocessor interface with double buffered data latches
- Four levels of programmable power management control with external power down pin support
- CMOS, TTL compatible I/O interface for lower power
- Controls provided for manual operation of PLL for recovery from defects

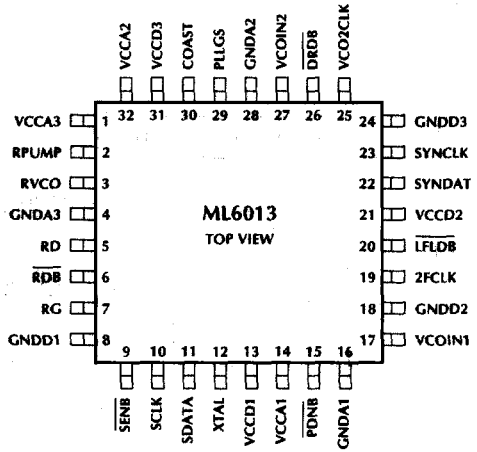
SYSTEM BLOCK DIAGRAM



BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN	NAME	FUNCTION
ECL Level Logic Inputs		
5	RD	Encoded read data from the ML6012 MOD drive read channel front-end processor. The rising edges of RD represent the flux changes on the media. (differential "+" input)
6	$\overline{RDB}$	Encoded read data from the ML6012 MOD drive read channel front-end processor. The falling edges of RDB represent the flux changes on the media. (differential "–" input)
ECL Level Logic Outputs		
(Note: These are test outputs for characterization purposes. External current sources are necessary to provide driving capability for these signals and the ECL buffer needs to be enabled from Control Register #7)		
25	VCO2CLK	Test point for Data separator VCO clock output.
26	$\overline{DRDB}$	Delayed read data output after the 1/4 cell delay. This signal is used for 1/4 cell delay characterization and window margin test. The rising edge is phase compared with the rising edge of VCO2CLK.
CMOS Level Logic Inputs		
7	RG	Read Gate signal from the disk controller. Active high signal indicates read mode. This input selects the phase detector input, switches the RRC output, initiates the data separator PLL acquisition.
12	XTAL	A parallel resonant crystal with low parasitic capacitance is connected between this pin and ground as the master clock source. An external clock can be used as an alternative.
15	$\overline{PDNB}$	Power Down Control. A low level input on this pin puts the chip in the power down (SLEEP) mode.
29	PLLGS	PLL gain select. A high level on this pin places the PLL in low-gain mode. A low places the PLL in high-gain mode.
30	COAST	A high level on this pin disables the phase detector/charge pump of the data separator PLL and allows the VCO to coast.

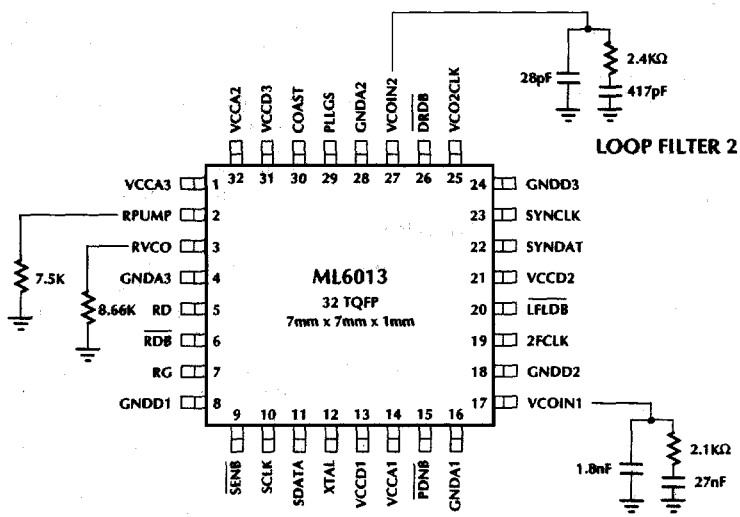
PIN	NAME	FUNCTION
CMOS Level Logic Inputs (continued)		
9	$\overline{SENB}$	Control Register Enable. Active low CMOS input. A logic low input on this pin allows the SCLK input to clock the SDATA into the control Register and a logic high on this input latches the control register contents.
10	SCLK	This is a CMOS input which clocks the Control Register. Internally this pin is gated with the $\overline{SENB}$ signal. While $\overline{SENB}$ is low, address and programming data are clocked in on the falling edges of SCLK.
11	SDATA	Control Register Data, CMOS input, clocked by SCLK.
CMOS Level Logic Outputs		
19	2FCLK	2X clock output from the frequency synthesizer.
20	$\overline{LFLDB}$	Loss of Phase/Frequency lock detected. This pin outputs a low level signal when the data separator VCO is out of lock or the incoming read data (RD) is missing for a predetermined number of clock (2FCLK) cycles.
22	SYNDAT	This is the synchronized and encoded data from the MOD drive. Data is clocked out on the falling edges of SYNCLK.
23	SYNCLK	Data synchronized clock. This pin outputs 2X (code rate) clock derived from the data separator VCO clock. In the read mode this is the recovered clock from the encoded read data.
Analog Pins		
3	RVCO	A 1% resistor connected between this pin and GNDA3 sets the VCO center frequency which is then programmed via register #3.
2	RPUMP	1% resistor connected between this pin and GNDA3 sets the nominal charge pump current.
17	VCOIN1	Frequency synthesizer PLL charge pump output and VCO input pin. A lowpass filter is connected between this pin and GNDA1.
27	VCOIN2	Data separator PLL charge pump output and VCO input pin. A lowpass filter is connected between this pin and GNDA2.

PIN DESCRIPTION

PIN	NAME	FUNCTION
Power Supplies		
13	VCCD1	5V digital supply
14	VCCA1	5V analog supply for frequency synthesizer.
21	VCCD2	5V digital supply
31	VCCD3	5V digital supply
32	VCCA2	5V analog supply for data separator.

PIN	NAME	FUNCTION
Power Supplies (continued)		
1	VCCA3	5V analog supply for miscellaneous functions.
4	GNDA3	Analog ground for miscellaneous functions
8	GNDD1	Digital Ground
16	GNDA1	Analog ground for frequency synthesizer
18	GNDD2	Digital Ground
28	GNDA2	Analog ground for data separator

TYPICAL EXTERNAL COMPONENTS



ASSUMPTIONS

T_S = 1.5µs @ F_{VCO} = 48MHz

Change pump current = 4X

K_O = 3200A/S/V

$\theta_{e,f} < 20\%$ of $\theta_{e,i}$

$\xi = 0.8$, $\omega_n T = 2.4$

ASSUMPTIONS

F_{XTAL} = 20MHz

N + 1 = 20, M + 1 = 48

K_O = 800A/S/V

$\theta_{e,f} < 1\%$ of $\theta_{e,i}$

T_S = 200µs

$\xi = 0.7$, $\omega_n T = 5$

Note: Loop filter optimized for 24Mbps NRZ operation.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

DC Supply Voltage (VCCA & VCCD) ..... –0.3 to +7V
Analog & Digital Inputs/Outputs ..... –0.3 to VCCA + 0.3V
Input Current per Pin ..... –25 to +25mA
Storage Temperature ..... –65 to +150°C
Maximum Junction Temperature ..... 125°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage Range ..... 4.75V to 5.25V
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VCCA = VCCD = 4.5 to 5.5 volts and T_A = 0 to 70°C, Note 1

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Dissipation					
V_{CC} (VCCA), (VCCD)		4.5		5.5	V
Supply Current	VCCA, VCCD = 4.5V to 5.5V, Data Rate = 24 Mbps, C_L < 15pF				
Read Mode	All circuits operational			80	mA
PLLFS Mode	Data separator, OFF			40	mA
Idle Mode	Only bias circuits & serial interface ON			10	mA
Sleep Mode	All circuits OFF, register contents retained			40	µA
Digital I/O Specifications					
High level input voltage		VCCD – 0.5		VCCD	V
Low level input voltage		GNDD		0.5	V
High level input current	V_{IN} = VCC			0.5	µA
Low level input current	V_{IN} = GND			0.5	µA
High level output voltage	$\|I_{OUT}\|$ = 2mA	VCCD – 0.5		VCCD	V
Low level output voltage	$\|I_{OUT}\|$ = 2mA			0.4	V
High impedance output current	@ V_{IN} = 100mV & VCC – 100mV	–0.5		0.5	µA
DC Characteristics					
Differential Input voltage swing	On ECL input pins RD & $\overline{RDB}$	0.8		1.6	V_{P-P}
Psuedo ECL low level output voltage	@ I_{OUT} = 3mA $\overline{DRDB}$ & VCO2CLK pins	VCCA – 2.05		VCCA – 1.45	V
Psuedo ECL high level output voltage	@ I_{OUT} = 3mA $\overline{DRDB}$ & VCO2CLK pins	VCCA – 1.7		VCCA – 1.3	V
Psuedo ECL output swing		0.15	0.25	0.35	V
Low level input current (Psuedo ECL)	Diff V_{IN} = 0V & VCC – 0.7V (RD & RDB inputs)	0.8	1.0	1.5	mA
High level input current (Psuedo ECL)	Diff V_{IN} = VCC – 0.7V & 0V (RD & RDB inputs)	0.8	1.0	1.5	mA
$V_{RD/RDB}$ common mode	Note 1	1.3	VCCD – 1.4	VCCD – 1.1	V
RPUMP bias voltage	RPUMP = 7.5 KΩ (1%)	0.7	0.75	0.8	V
RVCO bias voltage	RVCO = 7.9KΩ (1%)	0.65	0.79	0.9	V

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Synthesizer					
XTAL or input frequency	Parallel resonant type with minimum capacitance loading	5		20	MHz
M divider register		1		127	Decimal
N divider register		1		127	Decimal
VCO center frequency dynamic range (f_O)	Measure f_H @ VCOIN1 = 0.7V Measure f_L @ VCOIN1 = 2.3V Dynamic range = $(f_H - f_L)/f_1$	±17	±20		%
VCO gain	$\omega_O = 2 \times \pi \times f_O$, $K_{VCO} = \pi \times (f_1 - f_2)/100mV$ f_1 @ VCOIN1 @ f_O + 100 mV f_2 @ VCOIN1 @ f_O – 100 mV	0.25	0.35	0.44	rad/s-V
Pump current resistor	for setting pump current (±1%)		7.5		Kohms
Phase detector gain	$Kd = (I_O \times 48MHz) / (2 \times \pi \times f_O)$ $I_O = 0.75V/(2 \times R_{PUMP})$	0.80Kd	Kd	1.20Kd	A/rad
PLL loop gain	$G_O = 6.3 \times 10^6 / R_{PUMP}$	0.70 G_O	G_O	1.30 G_O	A/s x V
PLLFS RMS jitter ± 1 Sigma	Note 2			600	ps
Read Mode and Data Synchronizer					
VCO center frequency dynamic range (f_O)	Measure f_H @ VCOIN2 = 0.7V Measure f_L @ VCOIN2 = 2.3V Dynamic range = $(f_H - f_L)/f_1$	±10	±20		%
VCO gain	$\omega_O = 2 \times \pi \times f_O$, $K_{VCO} = \pi \times (f_1 - f_2)/100mV$ f_1 @ VCOIN1 @ f_O + 100 mV f_2 @ VCOIN1 @ f_O – 100 mV	0.25	0.35	0.44	rad/s – V
Phase detector gain	$Kd = (I_O \times 48MHz) / (2 \times \pi \times f_O)$ $I_O = (2 \times 0.75V)/R_{PUMP}$	0.80Kd	Kd	1.20Kd	A/rad
PLL loop gain	$G_O = 25.2 \times 10^6/R_{PUMP}$ (during preamble)	0.70G_O	G_O	1.30G_O	A/s x V
VCO ZPS error	(zero phase start)	–0.05T – 2		+0.05T + 2	ns
1/4 cell delay accuracy	relative to T/2			±5	%
Decode window centering accuracy	WC4 = 0 WC0 – 3 = 1, (Code rate = 48MHz)			±14	%
RD input pulse width	t_{WRD}	15		T	ns
RRC duty cycle	WG = 0, RG = 1	35		65	%
PLLDS RMS jitter, ± 1 Sigma	WG = 0, RG = 1, (Code rate = 48Mhz) Note 2			1	ns

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Read Mode and Data Synchronizer (continued)					
RRC to NRZout delay	t_{DNRZ1}			5	ns
RG to valid NRZout delay	t_{DNRZ2}		6TRRC		ns
Serial Microprocessor Interface					
Serial clock (SCLK) frequency		0.01		20	MHz
SCLK pulse width	t_{PW}	20			ns
SCLK to SDATA hold time	t_{HSD}	10			ns
SDATA to SCLK setup time	t_{SSD}	10			ns
SENB to SCLK setup time	t_{SSEN}	10			ns

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 2: The ±1 sigma RMS jitter is one standard deviation of the distribution of the edge transition time. The peak-to-peak is twice the value shown.

TIMING DIAGRAMS

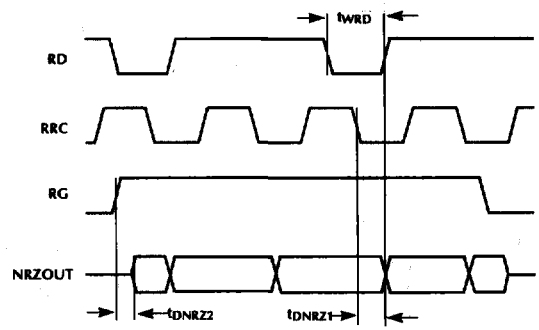


Figure 1. Read Mode Timing

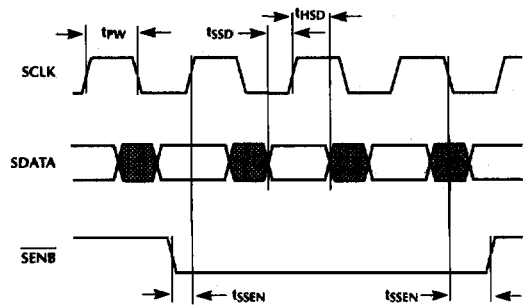


Figure 2. Serial Port Timing

FUNCTIONAL DESCRIPTION

The ML6013 is a BiCMOS MOD Read Channel Back-end Processor IC which works in conjunction with the ML6012 MOD Read Channel Front-end Processor to form a complete solution for the next generation of 3.5" Rewritable Magneto-Optical Drives (MOD). It incorporates a full function data synchronizer with a 3:1 operating range and a full function frequency synthesizer with onboard M & N dividers.

The most critical blocks on this chip are the three VCOs, one for the data synchronizer PLL, one for the frequency synthesizer PLL and the third VCO is used to generate the tracking 1/4 cell delay for (2, 7) RLL data synchronization. Careful design considerations have been incorporated to minimize the noise coupling and crosstalk among the VCOs. The highlights of the ML6013 VCO architecture are that it is a fully differential, high speed circuit with built-in switching. It provides a constant amplitude across the frequency span with on-chip timing capacitors. The system noise is highly minimized as the VCO operates at only 2X the data rate.

It provides 40-bits for user programmability of a number of features through a serial microprocessor interface and a bank of internal control registers. The control registers come up in an undetermined state on physical power-up and hence need to be initialized, to setup the ML6013 in a known state, on power-up. The control registers will retain their contents in all the power down modes, until power is physically switched off to the chip. The center frequency of the frequency synthesizer VCO is programmed with a 5-bit current DAC. The program information can be provided by the user, or it can be derived from the M & N information. The VCO control current results from the summation of this DAC based coarse control and PLL based fine control. The center frequency of the data separator VCO is programmed by duplicating the control current in the frequency synthesizer VCO as the coarse control. This leaves only the data rate variation to be fine tuned by the PLL, hence implying lower sensitivity and better jitter performance. The VCO3 period is programmed from a 5-bit current DAC, which is in turn referenced to the VCO2 control current. This will vary the 1/2 cycle of VCO3 for the required window centering programmability.

The ML6013 supports four power down modes for implementation of intelligent power management schemes. An external hardware pin is also provided to implement real time power management. In the sleep mode all sections are powered down except the serial microprocessor interface.

The ML6013 accepts the raw data in a pseudo ECL voltage level, as generated by the ML6012 and provides the synchronized data and clock outputs for the optical disk controller.

VCO ARCHITECTURE

The most critical circuit blocks in the ML6013 are the three VCOs. The first VCO is used in the frequency synthesizer PLL, the second VCO is used in the data separator PLL and the third VCO is used to generate the tracking 1/4 cell delay for (2, 7)RLL data synchronization.

The VCO architecture is optimized to minimize noise coupling from the digital sections of the chip and also the cross talk among the VCOs. The highlights of the VCO architecture are:

- High speed operation with built-in switching mechanism for optimized performance.
- Fully differential circuit configuration to achieve high level of noise immunity.
- On chip timing capacitors to control accuracy and for better noise immunity.
- Constant amplitude across frequency span.
- Symmetrical waveform (~50% duty cycle).

The operating frequency of the VCO is controlled by the tail current of the VCO which consists of two components — a fixed but programmable current (coarse), generated from a DAC which is controlled by the control register #3 and a variable current generated from the PLL. The coarse setting sets the center frequency of the VCO near the operating frequency and the negative feedback around the PLL is used to tune the VCO into the target operating frequency. To minimize the dependence on process and temperature variations the DAC current is derived using an external 1% resistor R_{VCO}. The center frequency is given by the equation:

$$f_O = \frac{m+17}{(16 \times R_{VCO} \times C)}$$

where m = 0 to 31 from control register #3

C = internal capacitor

R_{VCO} = 7.87 kΩ, 1% (recommended)

The architecture of the VCOs is such that they run at 2X the data rate. This reduces the speed requirements of the circuits and also helps in minimizing crosstalk between the VCOs, thus contributing towards overall system noise immunity. The output of the VCO is sent to a frequency doubler to generate the 4X frequency locally which is then divided by 2 or 4 to generate the synchronized 2X and 1X clocks. Zero phase start of the data separator VCO is supported for initial phase alignment.

PLL ARCHITECTURE

There are two PLLs implemented to realize the data separation (for data and clock recovery) and frequency synthesis function (required to support a zoned bit recording (ZBR) implementation). Shown below is a block diagram of the PLL which requires a first order loop filter.

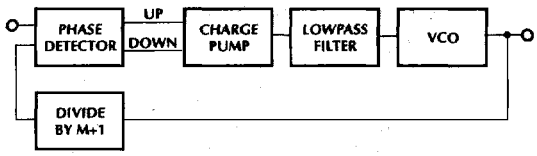


Figure 3. Block Diagram of PLL.

To design the PLL response with a well controlled loop gain value, an external 1% resistor (R_{PUMP}) is used to set the charge pump current according to the bandgap reference voltage generated on chip. The recommended value for Rpump is 7.5kΩ. The capacitor in series with the resistor in the loop filter is chosen so that typically it is 10 times the other capacitor. The resistor is chosen to yield a damping factor between 0.5 and 1 for the acquisition performance of the PLL.

FREQUENCY SYNTHESIZER PLL

In a Zone Bit Recording (ZBR) implementation, the disk is divided into a number of zones and the data rate varies from zone to zone. In order to support a ZBR implementation the appropriate frequencies need to be synthesized. VCO1 is used in the ML6013 frequency synthesizer to generate a clock with frequency f_{VCO1}. This is given by the formula:

$$f_{VCO1} = \frac{(M+1) \times f_{XTAL}}{(N+1)}$$

where M and N are 7-bit dividers, programmable through control registers #6, 5, 4. M and N should be at least 1 so that the divide ratio in both the forward and feedback paths are no less than 2, as that 50% duty cycle is guaranteed for the phase compared clocks. In a typical application the users keeps the N at a fixed value and reprograms M from zone to zone to synthesize the required frequency. A 2.5:1 span is required for most applications. The synthesized VCO1 clock is used to derive the 2FCLK clock. The VCO1 clock is also used to train VCO2 PLL during the non-read mode. The charge pump gain can be controlled through the CPG1 bit in control register #0. The default is always 1X gain. The frequency synthesizer PLL bandwidth is relatively low (~10KHz) for jitter performance.

The coarse center frequency of the frequency synthesizer VCO is programmed with a 5-bit current DAC in conjunction with control register #3. This speeds up the frequency acquisition and also minimizes the VCO sensitivity to V_{VCOIN1} and improves the jitter performance. The synthesized frequency is tuned using the M & N divider information and the crystal frequency, as given by the equation above.

PLL LOOP FILTER DESIGN FOR FREQUENCY SYNTHESIZER

To select the components for the loop filter, two parameters, ξ (damping factor) and ω_n (natural frequency) of the loop characteristic need to be specified.

It is desirable to have the damping factor ξ between 0.5 and 1 to prevent locking to harmonics while maintaining an acceptable lock time. For a high gain, second-order loop this results in minimum noise bandwidth.

The desired natural frequency ω_n of the loop is determined by satisfying the acquisition time (1% maximum phase error after phase acquisition) which is less than the minimum track-to-track seek time. This yields a settling time of approximately $t_S = 5/\omega_n$.

The formula for the filter components are shown in equations (1) and (2).

$$C_1 = \frac{K_O}{(M+1)\,\omega_n^2} \qquad (1)$$

$$R = \frac{2\xi\omega_n (M+1)}{K_O} \qquad (2)$$

where $K_O = K_D K_{VCO}$ (open loop gain)

The operating frequency F_{VCO} (code rate) is programmed by M&N registers. Equation (3) shows the programming relationship.

$$F_{VCO} = \frac{(M+1)}{(N+1)} \times F_{XTAL} \qquad (3)$$

The value of N should be fixed in the above equation and allow only the M to change for desired operating frequency.

Loop Filter Design Example:

NRZ data rate = 12 to 24 Mbps (1:2 ratio)
Code rate, F_{VCO} = 24 to 48MHz
(assumes (2, 7) RLL code)
F_{XTAL} = 20MHz
Choose N = 19, ⇒ M = 23 to 47
$K_D K_{VCO}$ = 800 A/S/V

Let the loop damping factor, ξ = 0.7 at F_{VCO} = 48MHz to allow ξ to rise at lower frequencies. Let ω_n = 25Krad/s (relatively low frequency, in the order of tens Krad/s for better jitter performance). This value produces a loop settling time = 200µs.

from eqn. (3) M + 1 = 48
from eqn. (1) C_1 = 27nF ⇒ $C_2 = C_1/15$ = 1.8nF
from eqn. (2) R = 2.1KΩ

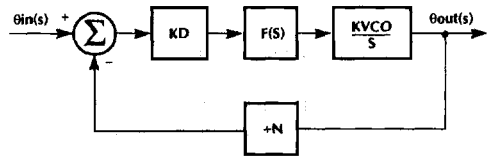
At F_{VCO} = 24MHz, M+1 = 24 which yields ξ = 1.0, and ω_n = 35Krad/s.

DATA SEPARATOR PLL

The center frequency of VCO2 is programmed by duplicating the control current in the VCO1 as the coarse control (control register #3). VCOIN2 thus has to do the fine tuning due to data rate variations (less than several percent), thus implying low sensitivity and good jitter performance. This is an important factor because the data separator PLL has higher bandwidth (of the order of 100KHz) to track the data rate variations and is hence more susceptible to noise induced jitter.

The charge pump has two modes of operation. During the non-read mode, the VCO clock is compared to the frequency synthesizer clock in every cycle, hence the charge pump should operate in the low gain mode (PLLGS = 1). After Read Gate is asserted, VCO clock is compared to the preamble data on every third clock (assuming 3T preamble pattern for (2, 7) RLL code). The charge pump should switch to the high gain mode (PLLGS = 0) to partially compensate for the loss of phase detector gain. This switching is necessary to maintain the damping factor in the PLL during the initial acquisition for guaranteed frequency lock after 24 preamble bytes. After the initial acquisition, the charge pump is switched back into the low gain mode for better jitter and noise performance.

The overall block diagram for the PLL can be described as:



where N = The ratio of the VCO frequency to the input frequency

To select the components for the loop filter, the user needs to consider the following loop requirements:

1. Residual phase error at the end of the preamble should be less than 4% of the total synchronization window (i.e. θ_e < 1ns for F_{VCO} = 48MHz or T_W = 20.8ns). This implies a large loop bandwidth so that it can quickly obtain lock within a predetermined length of the preamble field.
2. The lock-in range $\Delta\omega_L$ must be larger than the expected frequency step change due to variations in disk rotational velocity. In today's technology, the disk rotational velocity can be well controlled within ±1%.
3. The natural frequency ω_n and the damping factor ξ of the loop must be minimized to achieve maximum jitter rejection in the data field. The minimum value for the damping factor ξ will be 0.5 for adequate stability.
4. Re-lock time to the reference clock (frequency synthesizer) must be less than the minimum track-to-track seek time.

It is generally valid to assume the minimum value of ω_n is dominated by the bandwidth needed during preamble from requirement #1. This assumption will be checked in the design example.

The following loop filter design example assumes:

a. (2, 7) RLL code

b. The PLL encounters a phase offset instead of a frequency offset of the incoming data at the initial lock acquisition. The zero phase start function minimizes the initial phase offset to ±(0.2T + 2)ns where T = synchronization window.

Since the highest data rate yields the minimum amount of time that the PLL has to settle before decoding data, the settling time is calculated based on the highest data rate.

Loop Filter Design Example:

NRZ data rate = 24MHz
Code rate, F_{VCO} = 48MHz
N_{MIN} = 3 (during preamble, highest recorded frequency)
N_{MAX} = 8 (lowest recorded frequency)
Preamble length = 24 of 3T (100) pattern
T_S (settling time of PLL) = 3 x 24 ÷ 48MHz = 1.5µs
Initial phase error $\theta_{e,i}$ = 3ns
Final phase error (after T_S) $\theta_{e,f}$ < 20% of $\theta_{e,i}$
K_O = 3200 A/S/V during preamble

It is desirable to have the damping factor ξ between 0.5 and 1 during acquisition. For a high gain, second-order loop this results in minimum noise bandwidth.

Let the loop damping factor ξ = 0.9 to allow ξ to drop at N ≠ 3
As shown in figure 4, with ξ = 0.9, choosing $\omega_n T$ = 2.4 the phase error will be at most 20% of the initial phase error. Since T_S = 1.5µs, ω_n = 1.6Mrad/s.

If the previous assumption is correct, ω_n = 1.6Mrad/s should meet the loop requirements 2 and 4. First, examining requirement #2:

Let the maximum frequency step Δf = ±1% of the preamble frequency
Δf = ± 0.01 x 48MHz ÷ 3 = ±160KHz
Lock-in range is given by
$\Delta\omega_L = 2\xi\omega_n$ = 2 x 0.9 x 1.6Mrad/s = 2.88 Mrad/s

Thu, Δf_L = 458KHz > 160KHz and requirement #2 is met.

User is encouraged to check that ω_n = 1.6Mrad/s during preamble does meet the requirement #4.

Recall the equations for determining the filter components:

$$C_1 = \frac{K_O}{N \times \omega_n^2} \quad (4)$$

$$R = \frac{2\xi\omega_n N}{K_O} \quad (5)$$

from eqn. (4) $C_1 = 417pF \Rightarrow C_2 = C_1/15 = 28pF$
from eqn. (2) $R = 2.7K\Omega$

The above analysis is only shown as an example. The calculated values for filter components are most likely not optimized for all systems using the same data rate, code and preamble.

1/4 CELL DELAY & SYNCHRONIZER

The synchronizer circuit aligns the encoded read data pulses to the data separator VCO clock for the external decoder. Each rising edge of the encoded read data (RD) activates the following events:

1) It enables the 1/4 cell delay (VCO3 for half of a cycle) to generate a $\overline{DRDB}$ (delayed read data) pulse. The width of the $\overline{DRDB}$ pulse can be programmed by changing the tail current of VCO3. In normal operation, VCO3 is biased at the same current level as VCO2 so the half cycle pulse width is equivalent to 1/4 of the NRZ data period.

2) The falling edges of $\overline{DRDB}$ enable the phase detector, which operates in phase only mode during a read operation, so that the rising edges of the $\overline{DRDB}$ will be phase compared to the rising edges of VCO2 clock. The negative feedback around the PLL eventually aligns the rising edge of the $\overline{DRDB}$ to the rising edge of the VCO2 clock.

3) The falling edges of $\overline{DRDB}$ set the output of an internal Data Register (DR) flip-flop to 1, so the following rising edges of the VCO2 clock will clock it into the synchronizer. After the 1 is clocked into the synchronizer, DR is reset to 0 and the following VCO2 clocks will clock in 0's to the synchronizer until the DR is set by another read pulse.

   VCO3 period is programmed from a 5-bit current DAC which is in turn referenced to VCO2 control current. This will vary the 1/2 cycle of VCO3 for the required window centering programmability while performing window margin test.

LOSS OF PHASE/FREQUENCY LOCK DETECTOR

The loss of phase detector will bring the output $\overline{LFLDB}$ low after the encoded read data (RD) has been missing for a certain number of clock cycles due to surface defects. The internal control registers P1 and P0 determine the number of clock cycles to be used as reference. The loss of frequency detector detects if the VCO2 has locked to the harmonics of the incoming read data (in phase only mode) by comparing the frequency of VCO2 with the frequency of VCO1. The frequency detector guarantees a low output at $\overline{LFLDB}$ when it sees more than 10.5% difference in the frequency between VCO2 and VCO1 (the closest harmonic frequency that the VCO2 can lock to will be approximately ±12.5% from the operating channel frequency, 2FCLK). To allow margin for frequency offset in the recovery clock (SYNCLK) due to frequency variations, the frequency detector also guarantees no frequency offset detection if the SYNCLK is within ±3.5% of the 2FCLK.

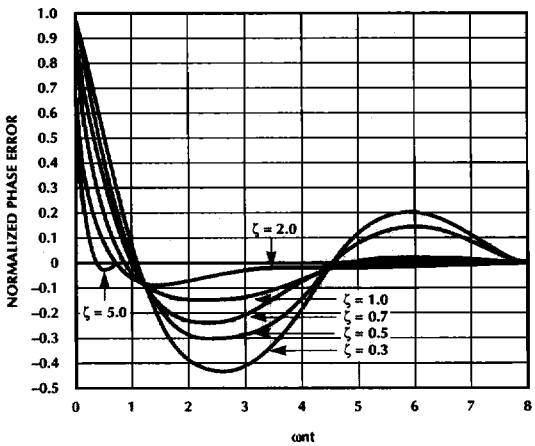


Figure 4. Transient phase error $\theta_e(t)$ due to a step in phase $\Delta\theta$.

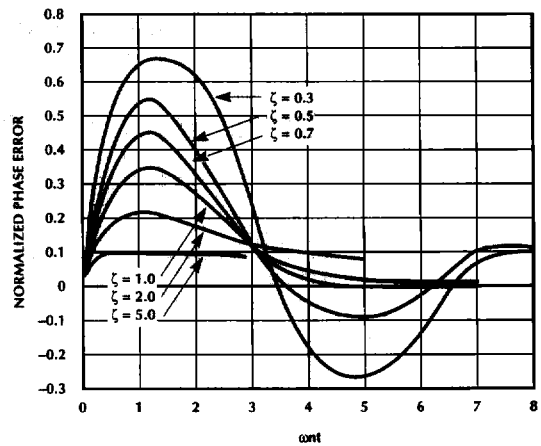


Figure 5. Transient phase error $\theta_e(t)$ due to a step in frequency $\Delta\omega$.

READ MODE OPERATION OF THE ML6013

When Read Gate (RG) is inactive low, the data separator PLL is locked to the VCO1 clock with the phase detector operating in the phase/frequency mode.

When Read Gate (RG) goes active high, (PLLGS should go low as RG goes high) the chip enters the read mode. The internal counter starts counting the number of pulses received on the RD/$\overline{\text{RDB}}$ input. After 8 RD pulses the VCO2 is stopped. VCO2 will restart at the next input transition. The zero phase start circuit eliminates the initial misalignment and speeds up the PLL acquisition. When RG is reasserted (PLLGS should stay high) after VCO2 recovers from the surface defects, zero phase start will be active immediately without counting another 8 RD pulses. When VCO2 restarts, the phase detector is switched to phase only mode with the input connected to DRD (delayed read data). The phase detector gain is also increased by 4X (CPG2 = 1) to ensure that the PLL has enough bandwidth and the right damping factor to lock within 24 preamble bytes. After 24 more RD pulses the PLL acquisition is assumed complete. The phase detector gain is then switched to the low gain mode (1X) for better jitter and noise performance. The phase detector gain will be automatically set when the PLLGS signal is not available from the controller. The 1-bit control "EXT" from the control register determines whether the PLLGS is controlled externally.

The end of the read operation is signalled by Read Gate going inactive low. VCO2 is stopped again and is restarted, synchronized with VCO1. Circuitry is implemented to ensure a glitchless transition of the clock frequencies on the RRC output.

POWER MANAGEMENT

The ML6013 provides a hardware pin ($\overline{\text{PDNB}}$) and two bits in control register #7 for multiple levels of power management control.

The major circuit blocks in the ML6013 are the serial interface, VCO1 and frequency synthesizer PLL, VCO2 and data separator PLL, VCO3, synchronizer, bias circuits and I/O circuits. The PDNB pin in conjunction with the 2 bits in control register #7 can be used to selectively turn off a combination of these blocks depending on the mode of operation. This allows the system designer to turn off sections of the chip that are not in use during a particular sequence of events, thus minimizing power dissipation at a micro management level. Table 1 shows these different power down modes and the circuit blocks affected in these different modes. Total typical power dissipation has two components — analog power dissipation which is more or less constant and digital power dissipation which varies with operating data rate.

SERIAL MICROPROCESSOR INTERFACE

The serial microprocessor interface consists of a simple three-wire serial port. Data is shifted serially into the ML6013 on the SDATA line on the falling edges of the serial shift clock, SCLK, provided the $\overline{\text{SENB}}$ pin is active (low). The data is shifted in blocks of eight bits with MSBit first. The internal registers are organized in blocks of eight bits, with the three most significant bits denoting the address, followed by the five data bits. This addressing scheme allows for a register bank of eight registers. When the chip is physically powered-up, the control registers come up in an undetermined state and hence they need to be initialized to some preset configuration, so that the behavior of the chip is predictable. The control registers retain their programmed information in all the power-down modes, except when the chip is physically powered-down. When the $\overline{\text{SENB}}$ pin goes inactive (high), the SDATA and SCLK pins are ignored and the previously shifted information is latched on the rising edge of the $\overline{\text{SENB}}$, into the appropriate register bank based on the address bits. It is recommended that the SCLK input be kept inactive low when it is in use. The SCLK input is capable of handling speeds up to 20MHz.

Table 1: Power down modes in the ML6013 with typical power dissipation

POWER DOWN MODE	SLEEP	IDLE	PLL	READ	PDWN	MAX WAKE UP TIME (ms)
PDNB pin	high	high	high	high	low	—
PM1, PM0	00	01	10	11	XX	—
VCO1 and PLLFS	off	off	on	on	off	0.5
VCO2, PLLDS VCO3 and Synchronizer	off	off	off	on	off	0.1
Bias and I/O circuits	off	on	on	on	off	0.02
XTAL Oscillator	off	on	on	on	off	100
Serial Interface	on	on	on	on	on	0
Typical analog power dissipation (mA)	<0.1	6	14	37	<0.1	—

CONTROL REGISTER DEFINITIONS

The control register bank consists of eight registers with addresses from 0 through 7. Outlined below are the detailed bit by bit definitions of the control registers 0 through 7.

CONTROL REGISTER #0

Miscellaneous Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	0	0	CPG2	CPG1	K2	K1	EXT

EXT = 0 PLLGS function is controlled internally
EXT = 1 PLLGS function is controlled externally

K1 = 0 Disable VCO1
K1 = 1 VCO1 is enabled

K2 = 0 Disable VCO2
K2 = 1 VCO2 is enabled

CPG1 = 0 Frequency synthesizer Phase detector gain is set to 1X
CPG1 = 1 Frequency synthesizer Phase detector gain is set to 2X

CPG2 = 0 Data separator phase detector gain is set to 2X during preamble acquisition
CPG2 = 1 Data separator phase detector gain is set to 4X during preamble acquisition and remains at 4X during read mode when EXT = 1 and PLLGS = 0

CONTROL REGISTER #1

Loss of Frequency Detection Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	0	1	RSVD	P1	P0	EFB	EPB

EPB = 0 Enable loss of phase lock detection
EPB = 1 Disable loss of phase lock detection

EFB = 0 Enable loss of frequency lock detection
EFB = 1 Disable loss of frequency lock detection

P1, P0 The combination of these two bits programs the number of VCO1 clock cycles that can elapse without RD present, before a loss of phase is detected in the LFLD circuit. This is shown in the table below:

P1	P0	NUMBER OF VCO1 CYCLES
0	0	12
0	1	20
1	0	22
1	1	28

CONTROL REGISTER #2

Data separator PLL window centering control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	1	0	WC4	WC3	WC2	WC1	WC0

WC4	WC3	WC2	WC1	WC0	VALUE
0	0	0	0	0	–24.0 %
0	0	0	0	1	–22.4 %
0	0	0	1	0	–20.8 %
0	0	0	1	1	–19.2 %
0	0	1	0	0	–17.6 %
0	0	1	0	1	–16.0 %
0	0	1	1	0	–14.4 %
0	0	1	1	1	–12.8 %
0	1	0	0	0	–11.2 %
0	1	0	0	1	–9.6 %
0	1	0	1	0	–8.0 %
0	1	0	1	1	–6.4 %
0	1	1	0	0	–4.8 %
0	1	1	0	1	–3.2 %
0	1	1	1	0	–1.6 %
0	1	1	1	1	0 % (center)
1	0	0	0	0	+1.6 %
1	0	0	0	1	+3.2 %
1	0	0	1	0	+4.8 %
1	0	0	1	1	+6.4 %
1	0	1	0	0	+8.0 %
1	0	1	0	1	+9.6 %
1	0	1	1	0	+11.2 %
1	0	1	1	1	+12.8 %
1	1	0	0	0	+14.4 %
1	1	0	0	1	+16.0 %
1	1	0	1	0	+17.6 %
1	1	0	1	1	+19.2 %
1	1	1	0	0	+20.8 %
1	1	1	0	1	+22.4 %
1	1	1	1	0	+24.0 %
1	1	1	1	1	+25.6 %

CONTROL REGISTER #3

VCO Coarse Center Frequency Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	1	1	CF4	CF3	CF2	CF1	CF0

CF4	CF3	CF2	CF1	CF0	F_O MHZ
0	0	0	0	0	17 MHz
0	0	0	0	1	18 MHz
0	0	0	1	0	19 MHz
0	0	0	1	1	20 MHz
0	0	1	0	0	21 MHz
0	0	1	0	1	22 MHz
0	0	1	1	0	23 MHz
0	0	1	1	1	24 MHz
0	1	0	0	0	25 MHz
0	1	0	0	1	26 MHz
0	1	0	1	0	27 MHz
0	1	0	1	1	28 MHz
0	1	1	0	0	29 MHz
0	1	1	0	1	30 MHz
0	1	1	1	0	31 MHz
0	1	1	1	1	31 MHz
1	0	0	0	0	33 MHz
1	0	0	0	1	34 MHz
1	0	0	1	0	35 MHz
1	0	0	1	1	36 MHz
1	0	1	0	0	37 MHz
1	0	1	0	1	38 MHz
1	0	1	1	0	39 MHz
1	0	1	1	1	40 MHz
1	1	0	0	0	41 MHz
1	1	0	0	1	42 MHz
1	1	0	1	0	43 MHz
1	1	0	1	1	44 MHz
1	1	1	0	0	45 MHz
1	1	1	0	1	46 MHz
1	1	1	1	0	47 MHz
1	1	1	1	1	48 MHz

CONTROL REGISTER #4

Divide by N Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	0	0	N6	N5	N4	N3	N2

CONTROL REGISTER #5

Divide by M Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	0	1	M6	M5	M4	M3	M2

CONTROL REGISTER #6

Divide by M & N and endec control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	1	0	RSVD	M1	M0	N1	N0

M & N are given by :

$$M = M6 \times 26 + M5 \times 25 + M4 \times 24 + M3 \times 23 + M2 \times 22 + M1 \times 21 + 1$$

or

$$M = 64 \times M6 + 32 \times M5 + 16 \times M4 + 8 \times M3 + 4 \times M2 + 2 \times M1 + 1$$

and

$$N = N6 \times 26 + N5 \times 25 + N4 \times 24 + N3 \times 23 + N2 \times 22 + N1 \times 21 + 1$$

or

$$N = 64 \times N6 + 32 \times N5 + 16 \times N4 + 8 \times N3 + 4 \times N2 + 2 \times N1 + 1$$

Note: The 7-bit M & N values are updated (latched) internally only when the most significant bit (M6 or N6) is written to, irrespective of changes in any other bits.

CONTROL REGISTER #7

Power Down Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	1	1	RSVD	BUF	0	PM1	PM0

BUF = 1 This bit enables the ECL output buffers so that the test signals $\overline{DRDB}$ and VCO2CLK are made available to the user.

BUF = 0 This disables the ECL output buffer, thus minimizing power dissipation.

D2 = 0 Reserved, must be programmed as "0" at all times.

Bit configuration for power down modes

PDNB	PM1	PM0	MODE
1	0	0	SLEEP
1	0	1	IDLE
1	1	0	PLL
1	1	1	READ
0	X	X	PDOWN

Note: PDOWN dissipation is the same as SLEEP mode

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6013CH	0°C to +70°C	32-Pin TQFP (H32)