SECTION 2

SPECIFICATIONS

GENERAL CHARACTERISTICS

The DSP56002 is fabricated in high-density HCMOS with TTL compatible inputs and outputs.

MAXIMUM RATINGS

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Note: In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification will never occur in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2-1 Absolute Maximum Ratings (GND = 0 V)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to +7.0	V
All Input Voltages	V_{IN}	(GND – 0.5) to (V_{CC} + 0.5)	V
Current Drain per Pin excluding V_{CC} and GND	I	10	mA
Operating Temperature Range	T_J	–40 to +105	°C
Storage Temperature	T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Table 2-2 Thermal Characteristics

Characteristic	Symbol	PQFP Value[3]	TQFP Value[3]	TQFP Value[4]	PGA Value[3]	Unit
Junction-to-ambient thermal resistance[1]	$R_{\theta JA}$ or θ_{JA}	50	48	40.6	22	°C/W
Junction-to-case thermal resistance[2]	$R_{\theta JC}$ or θ_{JC}	12.4	10.8	—	6.5	°C/W
Thermal characterization parameter	Ψ_{JT}	4.0	0.16	—	N/A	°C/W

Notes:
1. Junction-to-ambient thermal resistance is based on measurements on a horizontal-single-sided Printed Circuit Board per SEMI G38-87 in natural convection.(SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111) Measurements were made with the parts installed on thermal test boards meeting the specification EIA/JEDECSI-3.
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.
3. These are measured values. See note 1 for test board conditions.
4. These are measured values; testing is not complete. Values were measured on a non-standard four-layer thermal test board (two internal planes) at one watt in a horizontal configuration.

DC ELECTRICAL CHARACTERISTICS

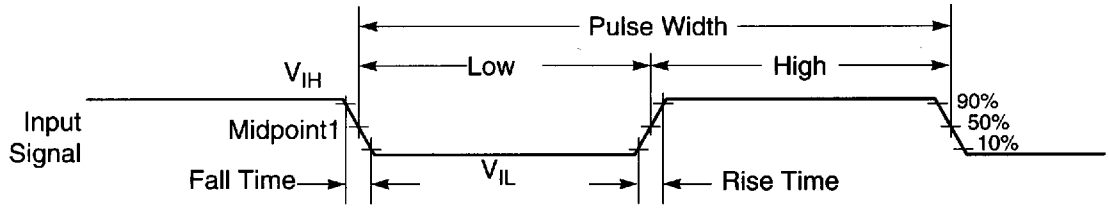
Table 2-3 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage					
•EXTAL	V_{IHC}	4.0	—	V_{CC}	V
•$\overline{\text{RESET}}$	V_{IHR}	2.5	—	V_{CC}	V
• MODA, MODB, MODC	V_{IHM}	3.5	—	V_{CC}	V
• All other inputs	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage					
• EXTAL	V_{ILC}	–0.5	—	0.6	V
• MODA, MODB, MODC	V_{ILM}	–0.5	—	2.0	V
• All other inputs	V_{IL}	–0.5	—	0.8	V
Input Leakage Current EXTAL, $\overline{\text{RESET}}$, MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, MODC/$\overline{\text{NMI}}$, $\overline{\text{DR}}$, $\overline{\text{BR}}$, $\overline{\text{WT}}$, CKP, PINIT, $\overline{\text{MCBG}}$, $\overline{\text{MCBCLR}}$, MCCLK, D20IN	I_{IN}	–1	—	1	µA
Tri-state (Off–state) Input Current (@ 2.4 V/0.4 V)	I_{TSI}	–10	—	10	µA
Output High Voltage (I_{OH} = –0.4 mA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 3.0 mA) $\overline{\text{HREQ}}$ I_{OL} = 6.7 mA, TXD I_{OL} = 6.7 mA	V_{OL}	—	—	0.4	V
Internal Supply Current at 40 MHz[1]	I_{CCI}	—	90	105	mA
• In Wait mode[2]	I_{CCW}	—	12	20	mA
• In Stop mode[2]	I_{CCS}	—	2	95	µA
Internal Supply Current at 66 MHz[1]	I_{CCI}	—	95	130	mA
• In Wait mode[2]	I_{CCW}	—	15	25	mA
• In Stop mode[2]	I_{CCS}	—	2	95	µA
Internal Supply Current at 80 MHz[1]	I_{CCI}	—	115	160	mA
• In Wait mode[2]	I_{CCW}	—	18	30	mA
• In Stop mode[2]	I_{CCS}	—	2	95	µA
PLL Supply Current[3]					
• 40 MHz		—	1.0	1.5	mA
• 66 MHz		—	1.1	1.5	mA
• 80 MHz		—	1.2	1.8	mA
CKOUT Supply Current[4]					
• 40 MHz		—	14	20	mA
• 66 MHz		—	28	35	mA
• 80 MHz		—	34	42	mA
Input Capacitance[5]	C_{IN}	—	10	—	pF

Notes:
1. **Section 4 Design Considerations** describes how to calculate the external supply current.
2. In order to obtain these results all inputs must be terminated (i.e., not allowed to float).
3. Values are given for PLL enabled.
4. Values are given for CKOUT enabled.
5. Periodically sampled and not 100% tested

AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, $\overline{\text{RESET}}$, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

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Figure 2-1 Signal Measurement Reference

INTERNAL CLOCKS

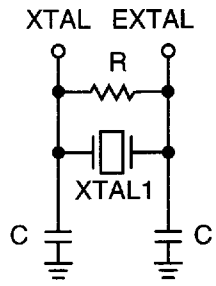
For each occurrence of T_H, T_L, T_C or I_{CYC}, substitute with the numbers in **Table 2-4**. DF and MF are PLL division and multiplication factors set in registers.

Table 2-4 Internal Clocks

Characteristics	Symbol	Expression
Internal Operation Frequency	f	
Internal Clock High Period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_H	ET_H (Min) $0.48 \times T_C$ (Max) $0.52 \times T_C$ (Min) $0.467 \times T_C$ (Max) $0.533 \times T_C$
Internal Clock Low Period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_L	ET_L (Min) $0.48 \times T_C$ (Max) $0.52 \times T_C$ (Min) $0.467 \times T_C$ (Max) $0.533 \times T_C$
Internal Clock Cycle Time	T_C	$ET_C \times DF/MF$
Instruction Cycle Time	I_{CYC}	$2 \times T_C$

EXTERNAL CLOCK (EXTAL PIN)

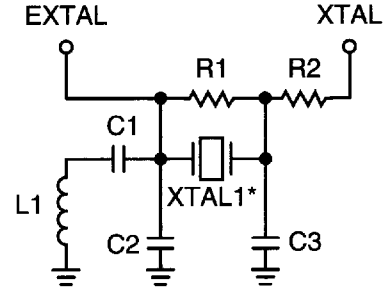
The DSP56002 system clock may be derived from the on-chip crystal oscillator as shown in **Figure 2-2**, or it may be externally supplied. An externally supplied square wave voltage source should be connected to EXTAL, leaving XTAL physically unconnected to the board or socket. The rise and fall times of this external clock should be 4 ns maximum.



Fundamental Frequency Crystal Oscillator

Suggested Component Values
R = 680 kΩ ± 10%
C = 20 pf ± 20%

Note:
1. The suggested crystal source is ICM, # 433163 - 4.00 (4 MHz fundamental, 20 pf load) or # 436163 - 30.00 (30 MHz fundamental, 20 pf load).
2. To reduce system cost, a ceramic resonator may be used instead of the crystal. Suggested source: Murata-Erie #CST4.00MGW040 (4 MHz with built-in load capacitors)



3rd Overtone Crystal Oscillator

Suggested Component Values
R1 = 470 kΩ ± 10%
R2 = 330 Ω ± 10%
C1 = 0.1 μf ± 20%
C2 = 26 pf ± 20%
C3 = 20 pf ± 10%
L1 = 2.37 μH ± 10%
XTAL = 40 MHz, AT cut, 20 pf load, 50 Ω max series resistance

Note:
1. *3rd overtone crystal.
2. The suggested crystal source is ICM, # 471163 - 40.00 (40 MHz 3rd overtone, 20 pf load).
3. R2 limits crystal current.
4. Reference Benjamin Parzen, The Design of Crystal and Other Harmonic Oscillators, John Wiley & Sons, 1983.

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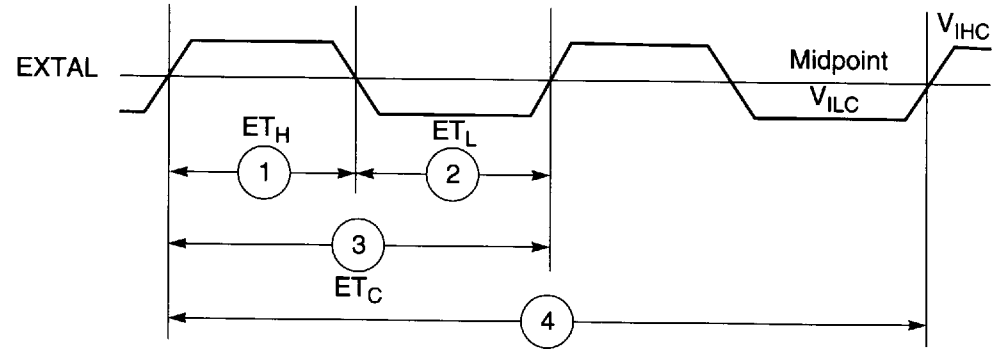
Figure 2-2 Crystal Oscillator Circuits



NOTE: The midpoint is $V_{ILC} + 0.5 (V_{IHC} - V_{ILC})$.

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Figure 2-3 External Clock Timing

Table 2-5 Clock Operation

Num	Characteristics	Symbol	40 MHz		66 MHz		80 MHz		Unit
			Min	Max	Min	Max	Min	Max	
	Frequency of Operation (EXTAL Pin)	E_f	0	40	0	66	0	80	MHz
1	Clock Input High • With PLL disabled (46.7% – 53.3% duty cycle) • With PLL enabled (42.5% – 57.5% duty cycle)	ET_H	11.7 10.5	∞ 235.5 µs	7.09 6.36	∞ 235.5 µs	5.8 5.3	∞ 235.5 µs	ns
2	Clock Input Low • With PLL disabled (46.7% – 53.3% duty cycle) • With PLL enabled (42.5% – 57.5% duty cycle)	ET_L	11.7 10.5	∞ 235.5 µs	7.09 6.36	∞ 235.5 µs	5.8 5.3	∞ 235.5 µs	ns
3	Clock Cycle Time • With PLL disabled • With PLL enabled	ET_C	25 25	∞ 409.6 µs	15.15 15.15	∞ 409.6 µs	12.5 12.5	∞ 409.6 µs	ns
4	Instruction Cycle Time = $I_{CYC} = 2T_C$ • With PLL disabled • With PLL enabled	I_{CYC}	50 50	∞ 819.2 µs	30.3 30.3	∞ 819.2 µs	25 25	∞ 819.2 µs	ns

Note: External Clock Input High and External Clock Input Low are measured at 50% of the input transition.

PHASE LOCK LOOP (PLL) CHARACTERISTICS

Table 2-6 Phase Lock Loop (PLL) Characteristics

Characteristics	Expression	Min	Max	Unit
VCO frequency when PLL enabled[1,2,3]	$MF \times E_f$	10	f	MHz
PLL external capacitor[4] (PCAP pin to V_{CCP})	$MF \times Cpcap$ @ $MF \leq 4$ @ $MF > 4$	 $MF \times 340$ $MF \times 380$	 $MF \times 480$ $MF \times 970$	 pF pF

Notes:
1. The E in ET_H, ET_L, and ET_C means external.
2. MF is the PCTL Multiplication Factor bits (MF0–MF11).
3. The maximum VCO frequency is limited to the internal operation frequency.
4. Cpcap is the value of the PLL capacitor (connected between PCAP pin and V_{CCP}) for MF = 1. The recommended value for Cpcap is: 400 pF for MF ≤ 4 and 540 pF for MF > 4.

RESET, STOP, MODE SELECT, AND INTERRUPT TIMING

C_L = 50 pF + 2 TTL loads
WS = number of Wait States (0–15) programmed into the external bus access using BCR
1 Wait State = T_C

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing (All Frequencies)

Num	Characteristics	Min	Max	Unit
9	Delay from $\overline{\text{RESET}}$ Assertion to Address High Impedance (periodically sampled and not 100% tested).	—	26	ns
10	Minimum Stabilization Duration • Internal Oscillator PLL Disabled[1] • External clock PLL Disabled[2] • External clock PLL Enabled[2]	 $75000T_C$ $25T_C$ $2500T_C$	 — — —	 ns ns ns
11	Delay from Asynchronous $\overline{\text{RESET}}$ Deassertion to First External Address Output (Internal Reset Deassertion)	$8T_C$	$9T_C + 20$	ns
12	Synchronous Reset Setup Time from $\overline{\text{RESET}}$ Deassertion to first CKOUT transition	8.5	T_C	ns
13	Synchronous Reset Delay Time from the first CKOUT transition to the First External Address Output	$8T_C$	$8T_C + 6$	ns
14	Mode Select Setup Time	21	—	ns
15	Mode Select Hold Time	0	—	ns
16	Minimum Edge-Triggered Interrupt Request Assertion Width	13	—	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing (All Frequencies) (Continued)

Num	Characteristics	Min	Max	Unit
16a	Minimum Edge-Triggered Interrupt Request Deassertion Width	13	—	ns
17	Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{NMI}$ Assertion to External Memory Access Address Out Valid • Caused by First Interrupt Instruction Fetch • Caused by First Interrupt Instruction Execution	 $5T_C + T_H$ $9T_C + T_H$	 — —	 ns ns
18	Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{NMI}$ Assertion to General Purpose Transfer Output Valid caused by First Interrupt Instruction Execution	$11T_C + T_H$	—	ns
19	Delay from Address Output Valid caused by First Interrupt Instruction Execute to Interrupt Request Deassertion for Level Sensitive Fast Interrupts[3]	—	$2\,T_C + T_L + (T_C \times WS) - 23$	ns
20	Delay from $\overline{RD}$ Assertion to Interrupt Request Deassertion for Level Sensitive Fast Interrupts[3]	—	$2T_C + (T_C \times WS) - 21$	ns
21	Delay from $\overline{WR}$ Assertion to Interrupt Request Deassertion for Level Sensitive Fast Interrupts[3] • WS = 0 • WS > 0	 — —	 $2T_C - 21$ $T_C + T_L + (T_C \times WS) - 21$	 ns ns
22	Delay from General-Purpose Output Valid to Interrupt Request Deassertion for Level Sensitive Fast Interrupts[3] —If Second Interrupt Instruction is: • Single Cycle • Two Cycles	 — —	 $T_L - 31$ $2T_C + T_L - 31$	 ns ns
23	Synchronous Interrupt Setup Time from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{NMI}$ Assertion to the second CKOUT transition	10	T_C	ns
24	Synchronous Interrupt Delay Time from the second CKOUT transition to the First External Address Output Valid caused by the First Instruction Fetch after coming out of Wait State	$13T_C + T_H$	$13T_C + T_H + 6$	ns
25	Duration for $\overline{IRQA}$ Assertion to Recover from Stop State	12	—	ns
26	Delay from $\overline{IRQA}$ Assertion to Fetch of First Interrupt Instruction (when exiting 'Stop')[1] • Internal Crystal Oscillator Clock, OMR bit 6 = 0 • Stable External Clock, OMR Bit 6 = 1 • Stable External Clock, PCTL Bit 17 = 1	 $65548T_C$ $20T_C$ $13T_C$	 — — —	 ns ns ns
27	Duration of Level Sensitive $\overline{IRQA}$ Assertion to ensure interrupt service (when exiting 'Stop')[1] • Internal Crystal Oscillator Clock, OMR bit 6 = 0 • Stable External Clock, OMR Bit 6 = 1 • Stable External Clock, PCTL Bit 17 = 1	 $65534T_C + T_L$ $6T_C + T_L$ 12	 — — —	 ns ns ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing (All Frequencies) (Continued)

Num	Characteristics	Min	Max	Unit
28	Delay from Level Sensitive $\overline{IRQA}$ Assertion to Fetch of First Interrupt Instruction (when exiting 'Stop') [1]			
	• Internal Crystal Oscillator Clock, OMR bit 6 = 0	$65548T_C$	—	ns
	• Stable External Clock, OMR bit 6 = 1	$20T_C$	—	ns
	• Stable External Clock, PCTL bit 17= 1	$13T_C$	—	ns

Notes:
1. A clock stabilization delay is required when using the on-chip crystal oscillator in two cases:
   • after power-on reset, and
   • when recovering from Stop mode.
   During this stabilization period, T_C, T_H, and T_L will not be constant. Since this stabilization period varies, a delay of $75{,}000 \times T_C$ is typically allowed to assure that the oscillator is stable before executing programs.
2. Circuit stabilization delay is required during reset when using an external clock in two cases:
   • after power-on reset, and
   • when recovering from Stop mode.
3. When using fast interrupts and $\overline{IRQA}$ and $\overline{IRQB}$ are defined as level-sensitive, then timings 19 through 22 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupt. Long interrupts are recommended when using Level-sensitive mode.

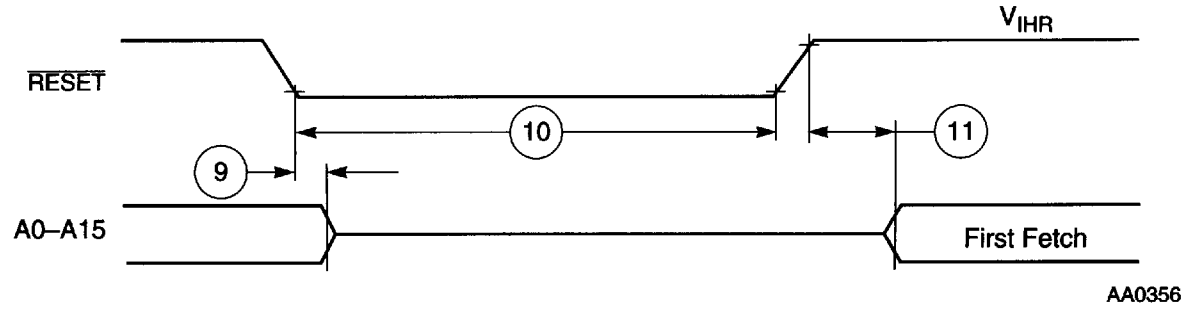


Figure 2-4 Reset Timing

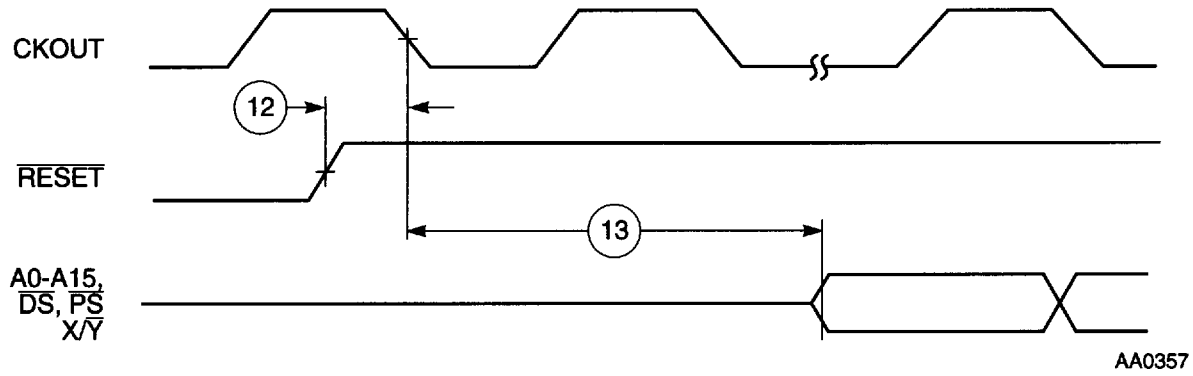


Figure 2-5 Synchronous Reset Timing

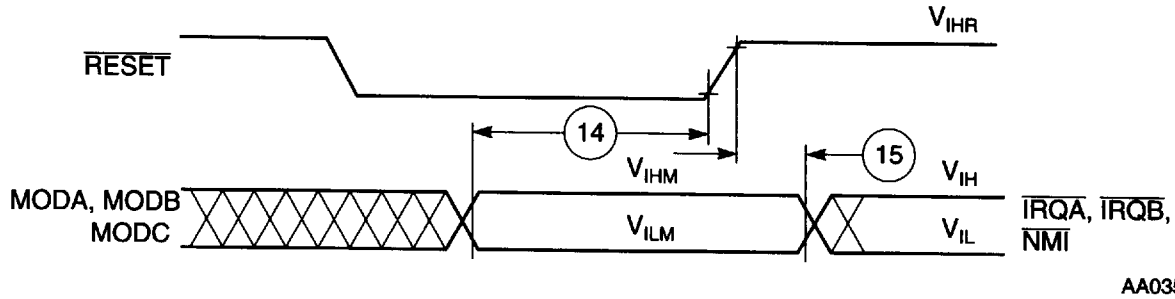


Figure 2-6 Operating Mode Select Timing

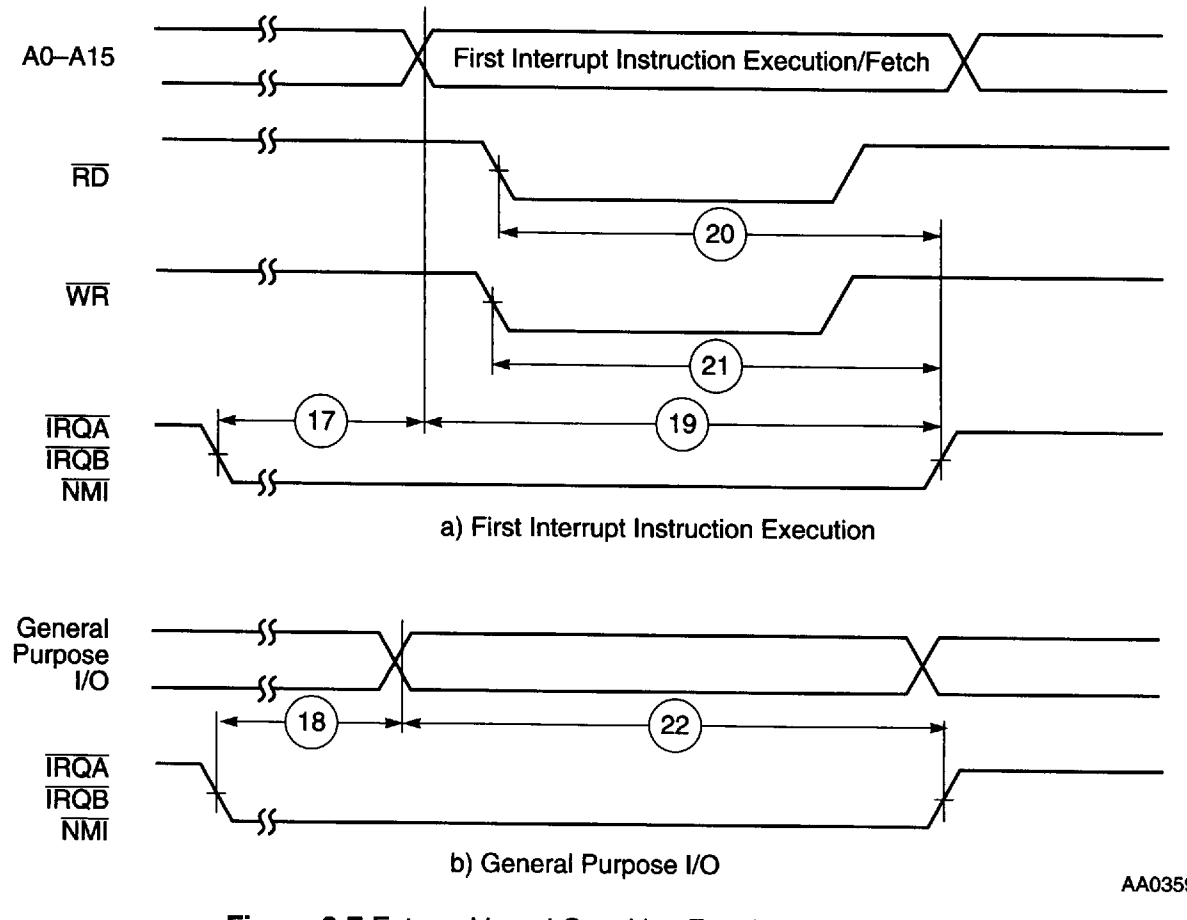


Figure 2-7 External Level-Sensitive Fast Interrupt Timing

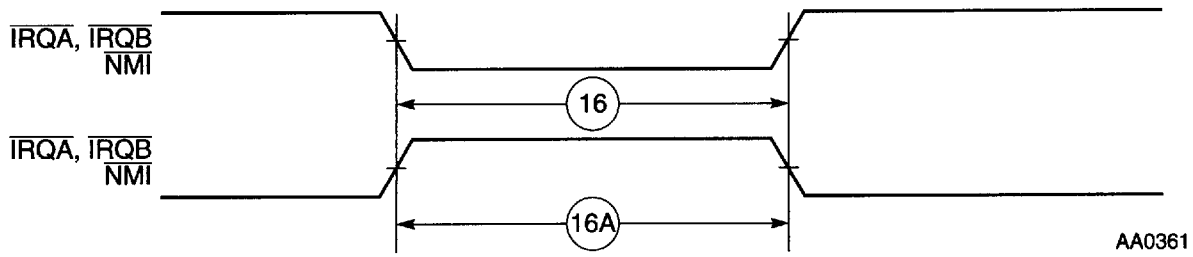


Figure 2-8 External Interrupt Timing (Negative Edge-Triggered)

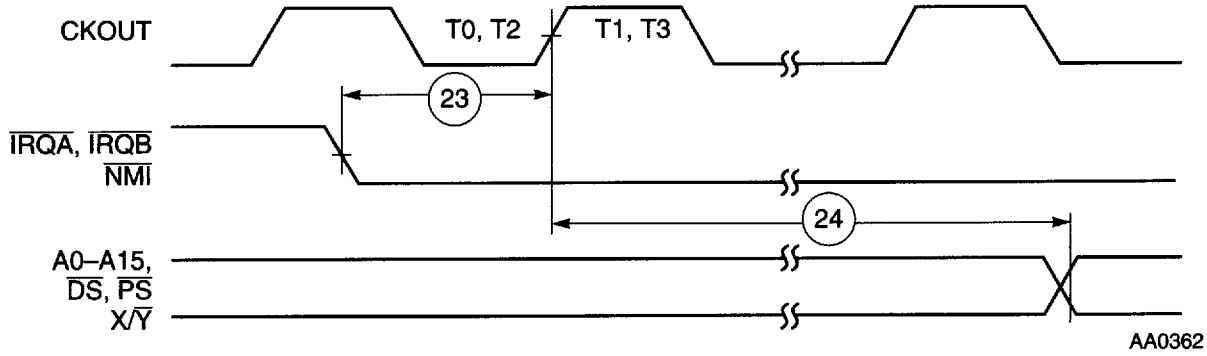


Figure 2-9 Synchronous Interrupt from Wait State Timing

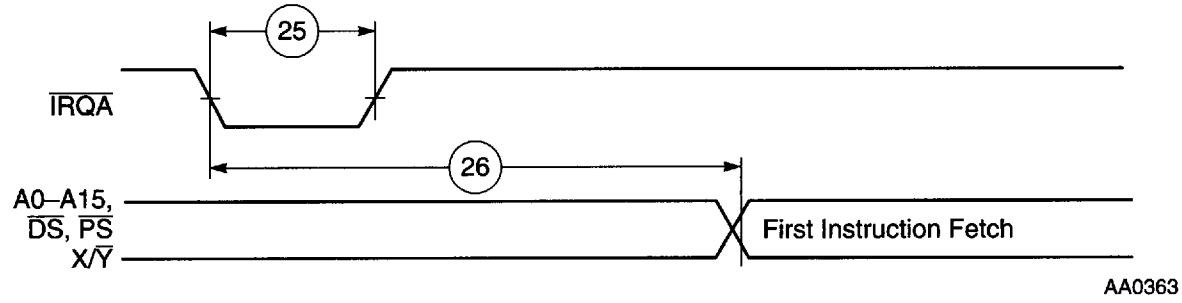


Figure 2-10 Recovery from Stop State Using IRQA

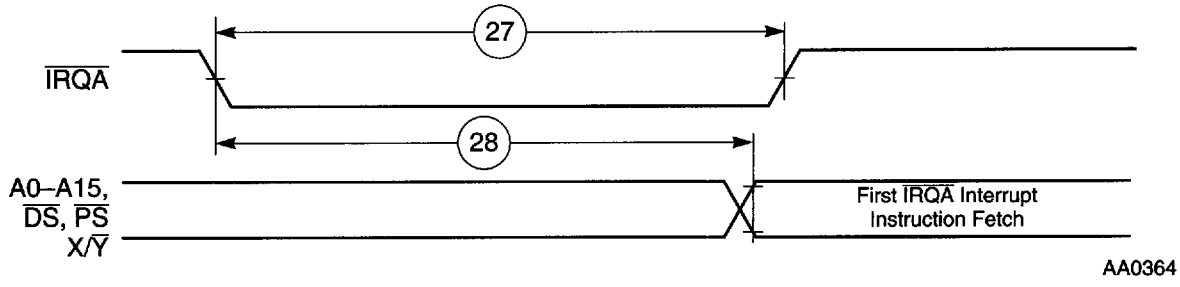


Figure 2-11 Recovery from Stop State Using IRQA Interrupt Service

HOST I/O (HI) TIMING

C_L = 50 pF + 2 TTL loads

Note: Active low lines should be "pulled up" in a manner consistent with the ac and dc specifications.

Table 2-8 Host I/O Timing (All Frequencies)

Num	Characteristics	Min	Max	Unit
31	$\overline{HEN}/\overline{HACK}$ Assertion Width[1] • CVR, ICR, ISR, RXL Read • IVR, RXH/M Read • Write	 $T_C + 31$ 26 13	 — — —	 ns
32	$\overline{HEN}/\overline{HACK}$ Deassertion Width[1] • Between Two TXL Writes[2] • Between Two CVR, ICR, ISR, RXL Reads[3]	13 $2T_C + 31$ $2T_C + 31$	— — —	ns ns ns
33	Host Data Input Setup Time Before $\overline{HEN}/\overline{HACK}$ Deassertion	4	—	ns
34	Host Data Input Hold Time After $\overline{HEN}/\overline{HACK}$ Deassertion	3	—	ns
35	$\overline{HEN}/\overline{HACK}$ Assertion to Output Data Active from High Impedance	0	—	ns
36	$\overline{HEN}/\overline{HACK}$ Assertion to Output Data Valid	—	26	ns
37	$\overline{HEN}/\overline{HACK}$ Deassertion to Output Data High Impedance[5]	—	18	ns
38	Output Data Hold Time After $\overline{HEN}/\overline{HACK}$ Deassertion[6]	2.5	—	ns
39	HR/$\overline{W}$ Low Setup Time Before $\overline{HEN}$ Assertion	0	—	ns
40	HR/$\overline{W}$ Low Hold Time After $\overline{HEN}$ Deassertion	3	—	ns
41	HR/$\overline{W}$ High Setup Time to $\overline{HEN}$ Assertion	0	—	ns
42	HR/$\overline{W}$ High Hold Time After $\overline{HEN}/\overline{HACK}$ Deassertion	3	—	ns
43	HA0–HA2 Setup Time Before $\overline{HEN}$ Assertion	0	—	ns
44	HA0–HA2 Hold Time After $\overline{HEN}$ Deassertion	3	—	ns
45	DMA $\overline{HACK}$ Assertion to $\overline{HREQ}$ Deassertion[4]	3	45	ns
46	DMA $\overline{HACK}$ Deassertion to $\overline{HREQ}$ Assertion[4,5] • For DMA RXL Read • For DMA TXL Write • All other cases	 $T_L + T_C + T_H$ $T_L + T_C$ 0	 — — —	 ns ns ns

Table 2-8 Host I/O Timing (Continued)(All Frequencies) (Continued)

Num	Characteristics	Min	Max	Unit
47	Delay from $\overline{\text{HEN}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion for RXL Read[4,5]	$T_L + T_C + T_H$	—	ns
48	Delay from $\overline{\text{HEN}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion for TXL Write[4,5]	$T_L + T_C$	—	ns
49	Delay from $\overline{\text{HEN}}$ Assertion to $\overline{\text{HREQ}}$ Deassertion for RXL Read, TXL Write [4,5]	3	58	ns

Notes:
1. See **Host Port Considerations** in **Section 4**.
2. This timing must be adhered to only if two consecutive writes to the TXL are executed without polling TXDE or $\overline{\text{HREQ}}$.
3. This timing must be adhered to only if two consecutive reads from one of these registers are executed without polling the corresponding status bits or $\overline{\text{HREQ}}$
4. $\overline{\text{HREQ}}$ is pulled up by a 1 kΩ resistor.
5. Specifications are periodically sampled and not 100% tested.
6. May decrease to 0 ns for future versions.

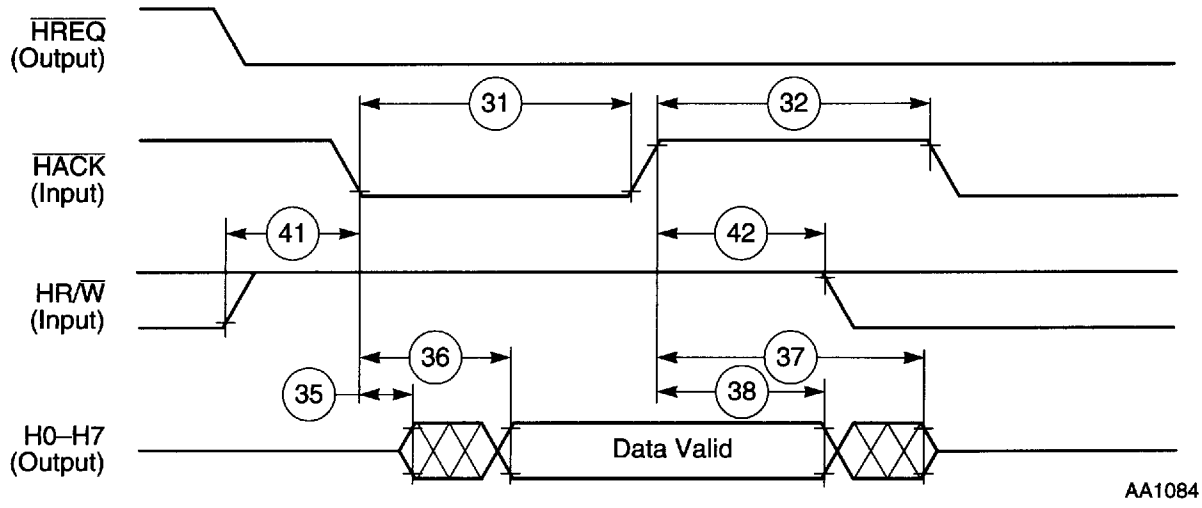


Figure 2-12 Host Interrupt Vector Register (IVR) Read

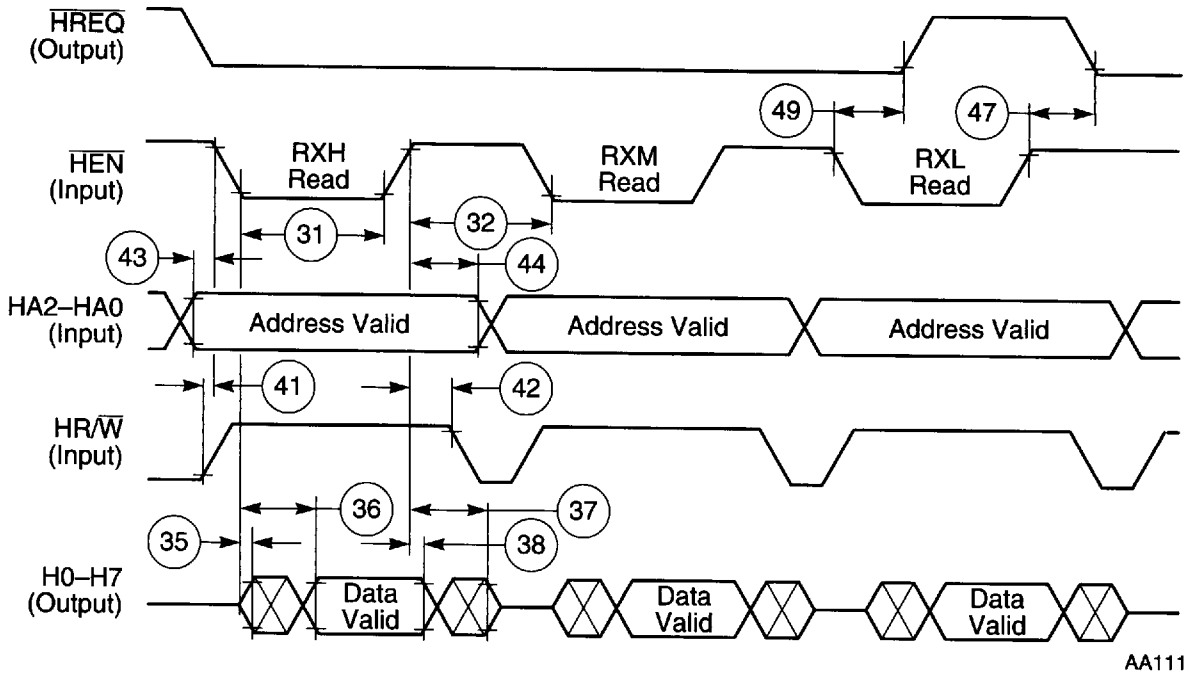


Figure 2-13 Host Read Cycle (Non-DMA Mode)

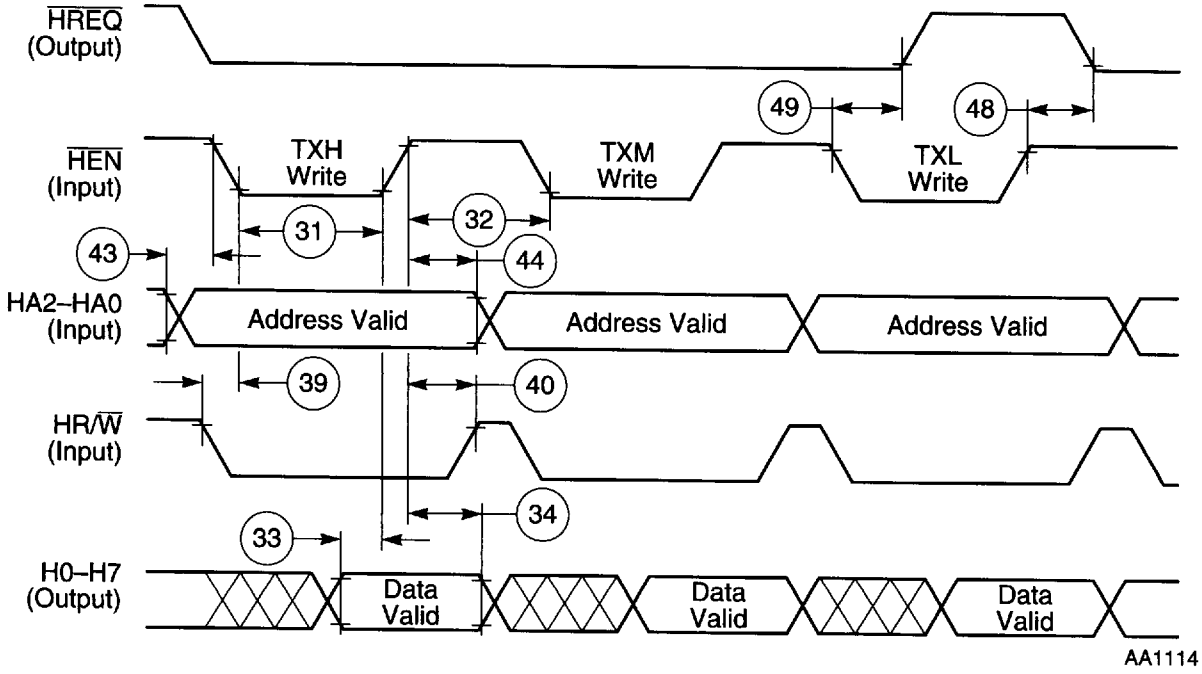


Figure 2-14 Host Write Cycle (Non-DMA Mode)

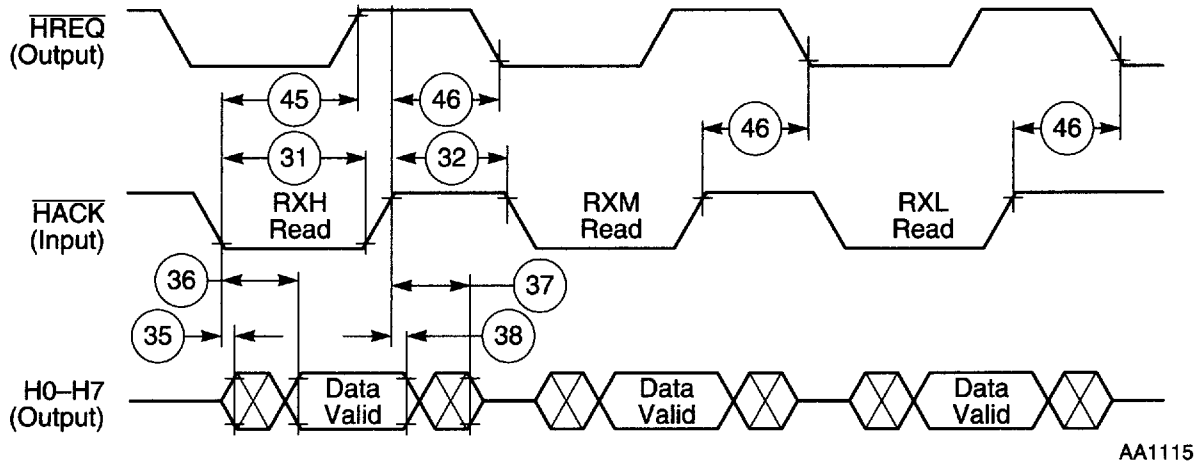


Figure 2-15 Host DMA Read Cycle

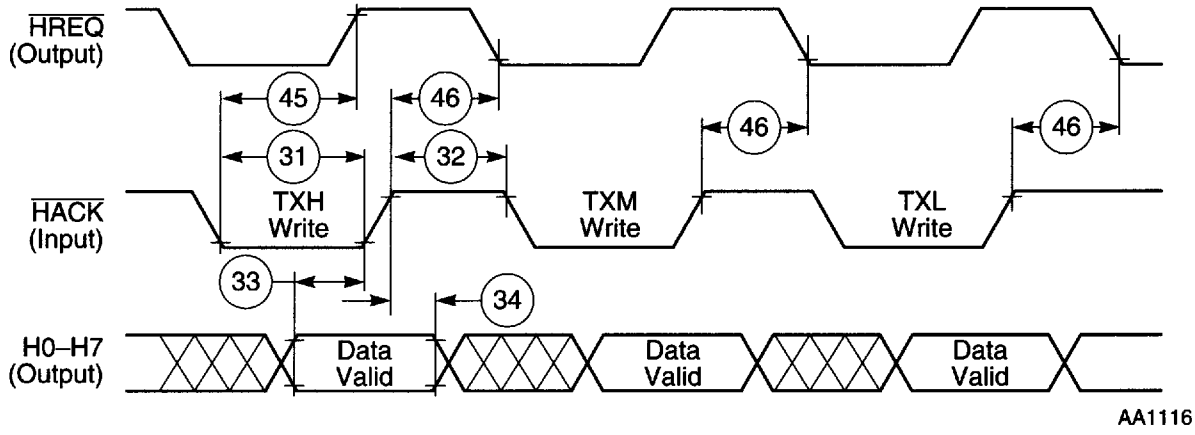


Figure 2-16 Host DMA Write Cycle

SERIAL COMMUNICATION INTERFACE (SCI) TIMING

C_L = 50 pF + 2 TTL loads
t_{SCC} = Synchronous Clock Cycle Time (For internal clock, t_{SCC} is determined by the SCI Clock Control Register and T_C.) The minimum t_{SCC} value is $8 \times T_C$.

Table 2-9 SCI Synchronous Mode Timing (All Frequencies)

Num	Characteristics	Min	Max	Unit
55	Synchronous Clock Cycle—t_{SCC}	$8T_C$	—	ns
56	Clock Low Period	$t_{SCC}/2 - 10.5$	—	ns
57	Clock High Period	$t_{SCC}/2 - 10.5$	—	ns
58	< intentionally blank >	—	—	—
59	Output Data Setup to Clock Falling Edge (Internal Clock)	$t_{SCC}/4 + T_L - 26$	—	ns
60	Output Data Hold After Clock Rising Edge (Internal Clock)	$t_{SCC}/4 - T_L - 8$	—	ns
61	Input Data Setup Time Before Clock Rising Edge (Internal Clock)	$t_{SCC}/4 + T_L + 23$	—	ns
62	Input Data Not Valid Before Clock Rising Edge (Internal Clock)	—	$t_{SCC}/4 + T_L - 5.5$	ns
63	Clock Falling Edge to Output Data Valid (External Clock)	—	32.5	ns
64	Output Data Hold After Clock Rising Edge (External Clock)	$T_C + 3$	—	ns
65	Input Data Setup Time Before Clock Rising Edge (External Clock)	16	—	ns
66	Input Data Hold Time After Clock Rising Edge (External Clock)	21	—	ns

Table 2-10 SCI Asynchronous Mode Timing—1X Clock

Num	Characteristics	Min	Max	Unit
67	Asynchronous Clock Cycle—t_{ACC}	$64T_C$	—	ns
68	Clock Low Period	$t_{ACC}/2 - 11$	—	ns
69	Clock High Period	$t_{ACC}/2 - 11$	—	ns
70	< intentionally blank >	—	—	—
71	Output Data Setup to Clock Rising Edge (Internal Clock)	$t_{ACC}/2 - 51$	—	ns
72	Output Data Hold After Clock Rising Edge (Internal Clock)	$t_{ACC}/2 - 51$	—	ns

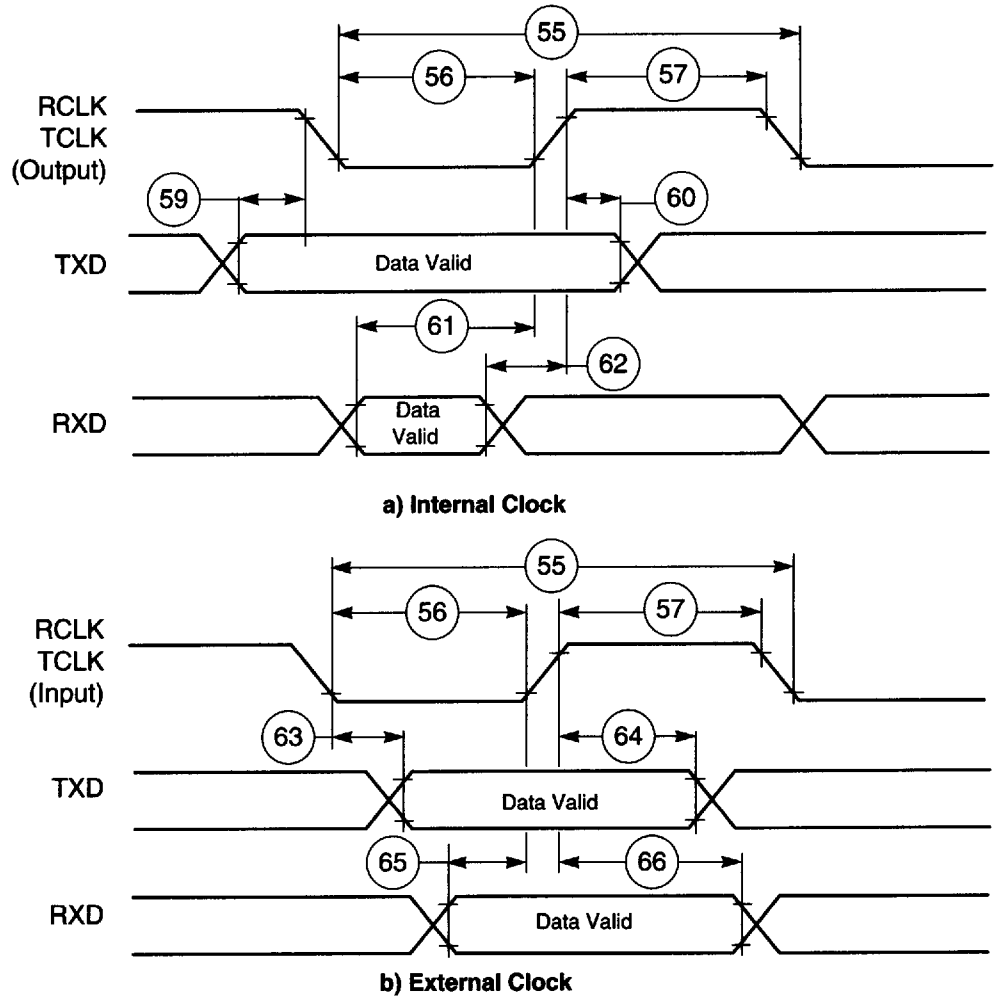
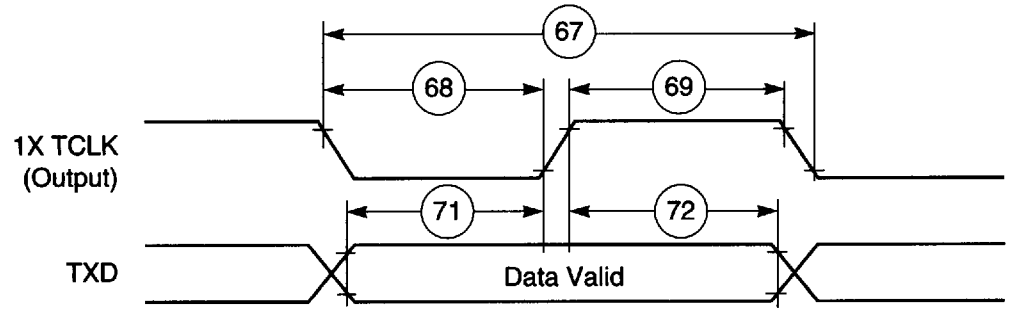


Figure 2-17 SCI Synchronous Mode Timing



Note: In the wire-OR mode, TXD can be pulled up by 1 kΩ.

Figure 2-18 SCI Asynchronous Mode Timing

SYNCHRONOUS SERIAL INTERFACE (SSI) TIMING

C_L = 50 pF + 2 TTL loads
t_{SSICC} = SSI clock cycle time
TXC (SCK Pin) = Transmit Clock
RXC (SC0 or SCK Pin) = Receive Clock
FST (SC2 Pin) = Transmit Frame Sync
FSR (SC1 or SC2 Pin) = Receive Frame Sync
i ck = Internal Clock
x ck = External Clock
g ck = Gated Clock
i ck a = Internal Clock, Asynchronous Mode (Asynchronous implies that STD and SRD are two different clocks)
i ck s = Internal Clock, Synchronous Mode (Synchronous implies that STD and SRD are the same clock)
bl = bit length
wl = word length

Table 2-11 SSI Timing

Num	Characteristics	40 MHZ or 66 MHz		80 MHz		Case	Unit
		Min	Max	Min	Max		
80	Clock Cycle–t_{SSICC}[1]	$4T_C$ $3T_C$	— —	$4T_C$ $3T_C$	— —	i ck x ck	ns
81	Clock High Period	$t_{SSICC}/2 - 10.8$ $T_C + T_L$	— —	$T_C + 5$ $T_C + 5$	— —	i ck x ck	ns
82	Clock Low Period	$t_{SSICC}/2 - 10.8$ $T_C + T_L$	— —	$T_C + 5$ $T_C + 5$	— —	i ck x ck	ns
84	RXC Rising Edge to FSR Out (bl) High	— —	40.8 25.8	— —	30 25.8	x ck i ck a	ns
85	RXC Rising Edge to FSR Out (bl) Low	— —	35.8 25.8	— —	30 25.8	x ck i ck a	ns
86	RXC Rising Edge to FSR Out (wl) High	— —	35.8 20.8	— —	30 20.8	x ck i ck a	ns
87	RXC Rising Edge to FSR Out (wl) Low	— —	35.8 20.8	— —	30 20.8	x ck i ck a	ns
88	Data In Setup Time Before RXC (SCK in Synchronous Mode) Falling Edge	3.3 15.8 13	— — —	3.3 15.8 13	— — —	x ck i ck a i ck s	ns

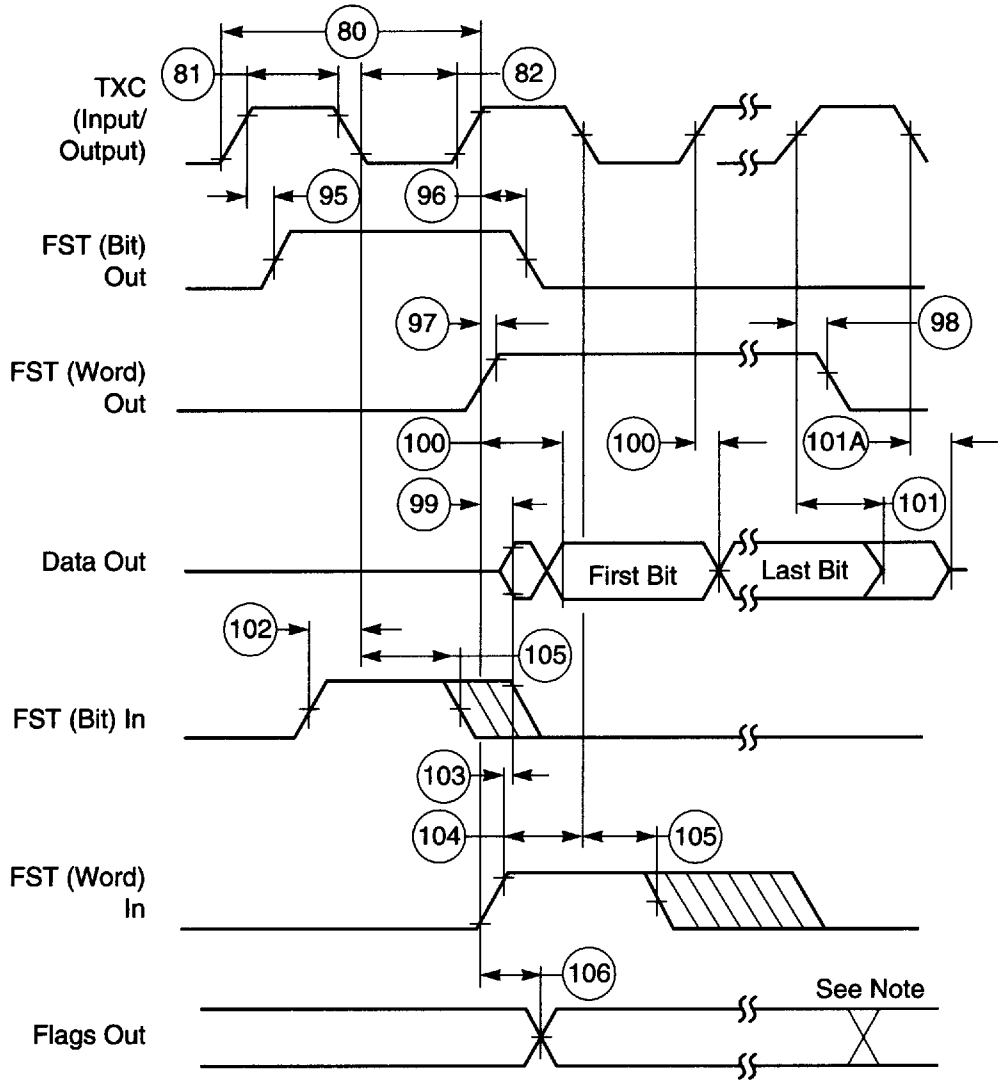
Table 2-11 SSI Timing (Continued)

Num	Characteristics	40 MHZ or 66 MHz		80 MHz		Case	Unit
		Min	Max	Min	Max		
89	Data In Hold Time After RXC Falling Edge	18 3.3	— —	18 3.3	— —	x ck i ck	ns
90	FSR Input (bl) High Before RXC Falling Edge	0.8 17.4	— —	0.8 17.4	— —	x ck i ck a	ns
91	FSR Input (wl) High Before RXC Falling Edge	3.3 18.3	— —	3.3 18.3	— —	x ck i ck a	ns
92	FSR Input Hold Time After RXC Falling Edge	18.3 3.3	— —	18.3 3.3	— —	x ck i ck	ns
93	Flags Input Setup Before RXC Falling Edge	0.8 16.7	— —	0.8 16.7	— —	x ck i ck s	ns
94	Flags Input Hold Time After RXC Falling Edge	18.3 3.3	— —	18.3 3.3	— —	x ck i ck s	ns
95	TXC Rising Edge to FST Out (bl) High	— —	31.6 15.8	— —	30 15.8	x ck i ck	ns
96	TXC Rising Edge to FST Out (bl) Low	— —	33.3 18.3	— —	30 18.3	x ck i ck	ns
97	TXC Rising Edge to FST Out (wl) High	— —	30.8 18.3	— —	30 18.3	x ck i ck	ns
98	TXC Rising Edge to FST Out (wl) Low	— —	33.3 18.3	— —	30 18.3	x ck i ck	ns
99	TXC Rising Edge to Data Out Enable from High Impedance	— —	33.3 + T_H 20.8	— —	30 20.8	x ck i ck	ns
100	TXC Rising Edge to Data Out Valid	— —	33.3 + T_H 22.4	— —	30 22.4	x ck i ck	ns
101	TXC Rising Edge to Data Out High Impedance [2]	— —	35.8 20.8	— —	30 20.8	x ck i ck	ns

Table 2-11 SSI Timing (Continued)

Num	Characteristics	40 MHZ or 66 MHz		80 MHz		Case	Unit
		Min	Max	Min	Max		
101A	TXC Falling Edge to Data Out High Impedance [2]	—	$T_C + T_H$	—	$T_C + T_H$	g ck	ns
102	FST Input (bl) Setup Time Before TXC Falling Edge	0.8 18.3	—	0.8 18.3	—	x ck i ck	ns
103	FST Input (wl) to Data Out Enable from High Impedance	—	30.8	—	30.8		ns
104	FST Input (wl) Setup Time Before TXC Falling Edge	0.8 20.0	— —	0.8 20.0	— —	x ck i ck	ns
105	FST Input Hold Time After TXC Falling Edge	18.3 3.3	— —	18.3 3.3	— —	x ck i ck	ns
106	Flag Output Valid After TXC Rising Edge	— —	32.5 20.8	— —	30 20.8	x ck i ck	ns

Notes: 1. For internal clock, External Clock Cycle is defined by I_{cyc} and SSI control register.
2. Periodically sampled and not 100% tested



Note: In the Network mode, output flag transitions can occur at the start of each time slot within the frame. In the Normal mode, the output flag state is asserted for the entire frame period.

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Figure 2-19 SSI Transmitter Timing

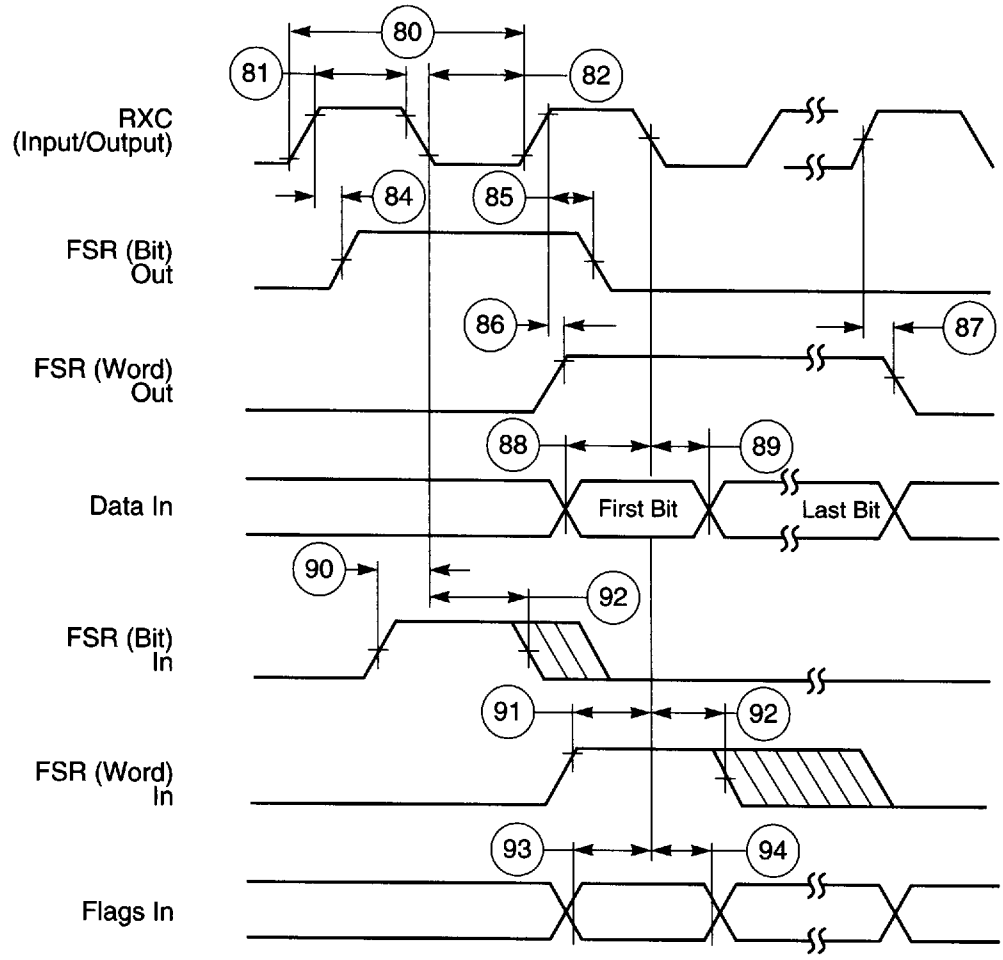

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Figure 2-20 SSI Receiver Timing

EXTERNAL BUS ASYNCHRONOUS TIMING

C_L = 50 pF + 2 TTL loads
WS = Number of Wait States (0 to 15), as determined by BCR register

Capacitance Derating: The DSP56002 External Bus Timing Specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the External Bus pins (A0–A15, D0–D23, PS, DS, RD, WR, X/Y, EXTP) derates linearly at 1 ns per 12 pF of additional capacitance from 50 pF to 250 pF of loading. Port B and C pins (HI, SCI, SSI, and Timer) derate linearly at 1 ns per 5 pF of additional capacitance from 50 pF to 250 pF of loading. Active low lines should be "pulled up" in a manner consistent with the AC and DC specifications.

Table 2-12 External Bus Asynchronous Timing

No.	Characteristics	40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
115	Delay from $\overline{BR}$ Assertion to $\overline{BG}$ Assertion							
	• With no external access from the DSP	$2T_C + T_H$	$4T_C + T_H + 14$	$2T_C + T_H$	$4T_C + T_H + 14$	$2T_C + T_H$	$4T_C + T_H + 14$	ns
	• During external read or write access	$T_C + T_H$	$4T_C + T_H + (T_C \times WS) + 14$	$T_C + T_H$	$4T_C + T_H + (T_C \times WS) + 14$	$T_C + T_H$	$4T_C + T_H + (T_C \times WS) + 14$	ns
	• During external read-modify-write access	$T_C + T_H$	$6T_C + T_H + (2T_C \times WS) + 14$	$T_C + T_H$	$6T_C + T_H + (2T_C \times WS) + 14$	$T_C + T_H$	$6T_C + T_H + (2T_C \times WS) + 14$	ns
	• During Stop mode—external bus will not be released and $\overline{BG}$ will not go low	∞	14	∞	14	∞	14	ns
	• During Wait mode	T_H	$T_C + T_H + 15$	T_H	$T_C + T_H + 15$	T_H	$T_C + T_H + 15$	ns
116	Delay from $\overline{BR}$ Deassertion to $\overline{BG}$ Deassertion	$2T_C$	$4T_C + 12.5$	$2T_C$	$4T_C + 12.5$	$2T_C$	$4T_C + 12.5$	ns

Table 2-12 External Bus Asynchronous Timing (Continued)

No.	Characteristics	40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
117	$\overline{BG}$ Deassertion Duration • During Wait mode • All other cases	 $T_C - 5.5$ $2T_C + T_H - 5.5$	 — —	 $T_C - 5.5$ $2T_C + T_H - 5.5$	 — —	 $T_C - 5.5$ $2T_C + T_H - 5.5$	 — —	 ns ns
118	Delay from Address, Data, and Control Bus High Impedance to $\overline{BG}$ Assertion	0	—	0	—	0	—	ns
119	Delay from $\overline{BG}$ Deassertion to Address and Control Bus Enabled	0	T_H	0	T_H	0	T_H	ns
120	Address Valid to $\overline{WR}$ Assertion • WS = 0 • WS > 0	 $T_L - 6$ $T_C - 6$	 — —	 $T_L - 4.5$ $T_C - 4.5$	 — —	 $T_L - 4.5$ $T_C - 4.5$	 — —	 ns ns
121	$\overline{WR}$ Assertion Width • WS = 0 • WS > 0	 $T_C - 4$ $WS \times T_C + T_L$	 — —	 $T_C - 4$ $WS \times T_C + T_L$	 — —	 $T_C - 2$ $WS \times T_C + T_L$	 — —	 ns ns
122	$\overline{WR}$ Deassertion to Address Not Valid	$T_H - 6$	—	$T_H - 4$	—	$T_H - 4$	—	ns
123	$\overline{WR}$ Assertion to Data Out Active From High Impedance • WS = 0 • WS > 0	 $T_H - 4$ 0	 — —	 $T_H - 4$ 0	 — —	 $T_H - 4$ 0	 — —	 ns ns
124	Data Out Hold Time from $\overline{WR}$ Deassertion (the maximum specification is periodically sampled, and not 100% tested)	$T_H - 7$	$T_H - 2.5$	$T_H - 5$	$T_H - 1.5$	$T_H - 5$	$T_H - 1.5$	ns
125	Data Out Setup Time to $\overline{WR}$ Deassertion • WS = 0 • WS > 0	 $T_L - 0.8$ $WS \times T_C + T_L - 0.8$	 — —	 $T_L - 0.4$ $WS \times T_C + T_L - 0.4$	 — —	 $T_L - 0.5$ $WS \times T_C + T_L - 0.5$	 — —	 ns ns

Table 2-12 External Bus Asynchronous Timing (Continued)

No.	Characteristics	40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
126	$\overline{RD}$ Deassertion to Address Not Valid	T_H	—	$T_H - 1$	—	T_H	—	ns
127	Address Valid to $\overline{RD}$ Deassertion							
	• WS = 0	$T_C + T_L - 6$	—	$T_C + T_L - 6$	—	$T_C + T_L - 6$	—	ns
	• WS > 0	$((WS + 1) \times T_C) + T_L - 6$	—	$((WS + 1) \times T_C) + T_L - 6$	—	$((WS + 1) \times T_C) + T_L - 6$	—	ns
128	Input Data Hold Time to $\overline{RD}$ Deassertion	0	—	0	—	0	—	ns
129	$\overline{RD}$ Assertion Width							
	• WS = 0	$T_C - 4$	—	$T_C - 4$	—	$T_C - 4$	—	ns
	• WS > 0	$((WS + 1) \times T_C) - 4$	—	$((WS + 1) \times T_C) - 4$	—	$((WS + 1) \times T_C) - 4$	—	ns
130	Address Valid to Input Data Valid							
	• WS = 0	—	$T_C + T_L - 9.5$	—	$T_C + T_L - 7$	—	$T_C + T_L - 6$	ns
	• WS > 0	—	$((WS+1) \times T_C) + T_L - 9.5$	—	$((WS+1) \times T_C) + T_L - 7$	—	$((WS+1) \times T_C) + T_L - 6$	ns
131	Address Valid to $\overline{RD}$ Assertion	$T_L - 4.5$	—	$T_L - 4.5$	—	$T_L - 4.5$	—	ns
132	$\overline{RD}$ Assertion to Input Data Valid							
	• WS = 0	—	$T_C - 7.5$	—	$T_C - 5.5$	—	$T_C - 5.5$	ns
	• WS > 0	—	$((WS+1) \times T_C) - 7.5$	—	$((WS+1) \times T_C) - 5.5$	—	$((WS+1) \times T_C) - 5.5$	ns
133	$\overline{WR}$ Deassertion to $\overline{RD}$ Assertion	$T_C - 7$	—	$T_C - 5$	—	$T_C - 5$	—	ns
134	$\overline{RD}$ Deassertion to $\overline{RD}$ Assertion	$T_C - 4$	—	$T_C - 2.5$	—	$T_C - 2.5$	—	ns
135	$\overline{WR}$ Deassertion to $\overline{WR}$ Assertion							
	• WS = 0	$T_C - 4$	—	$T_C - 3$	—	$T_C - 3$	—	ns
	• WS > 0	$T_C + T_H - 4$	—	$T_C + T_H - 3$	—	$T_C + T_H - 3$	—	ns

Table 2-12 External Bus Asynchronous Timing (Continued)

No.	Characteristics	40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
136	$\overline{RD}$ Deassertion to $\overline{WR}$ Assertion • WS = 0 • WS > 0	 $T_C - 4$ $T_C + T_H - 4$	 — —	 $T_C - 2.5$ $T_C + T_H - 2.5$	 — —	 $T_C - 2.5$ $T_C + T_H - 2.5$	 — —	 ns ns

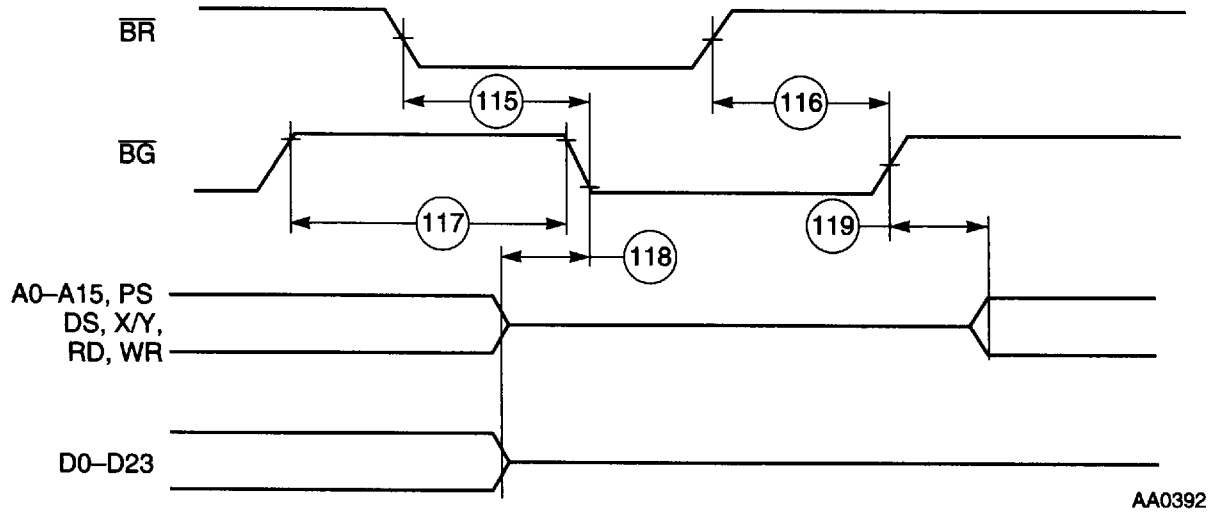
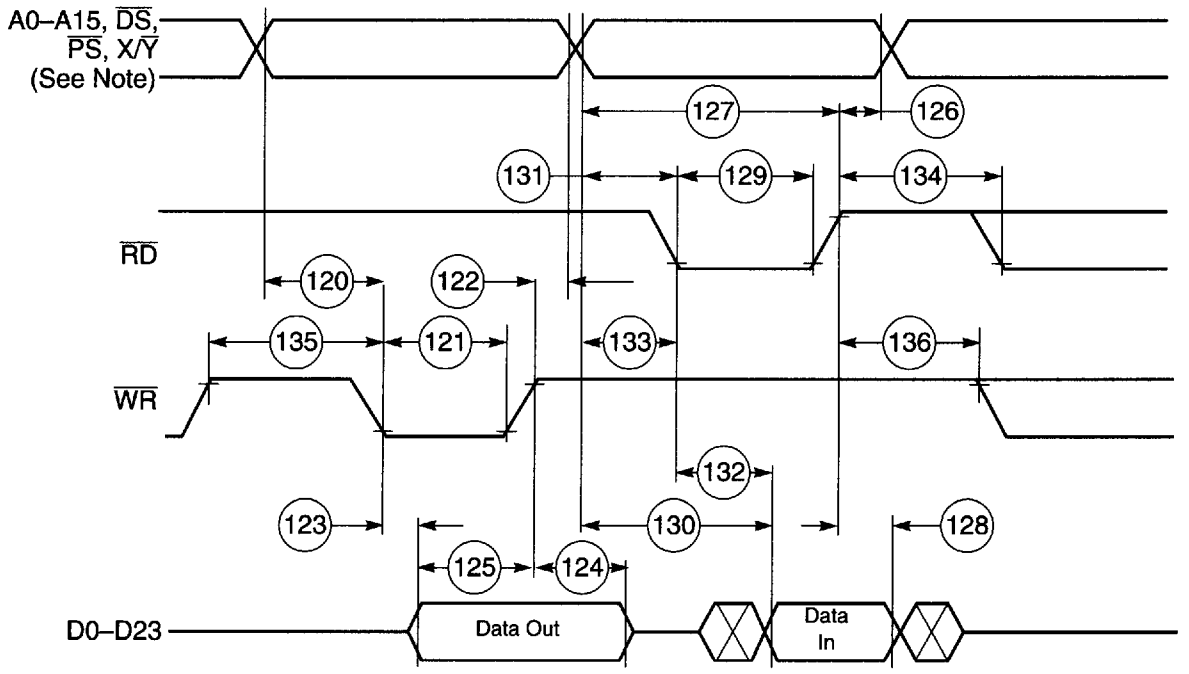


Figure 2-21 Bus Request / Bus Grant Timing

External Bus Asynchronous Timing



Note: During Read-Modify-Write instructions, the address lines do not change state.

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Figure 2-22 External Bus Asynchronous Timing

EXTERNAL BUS SYNCHRONOUS TIMING

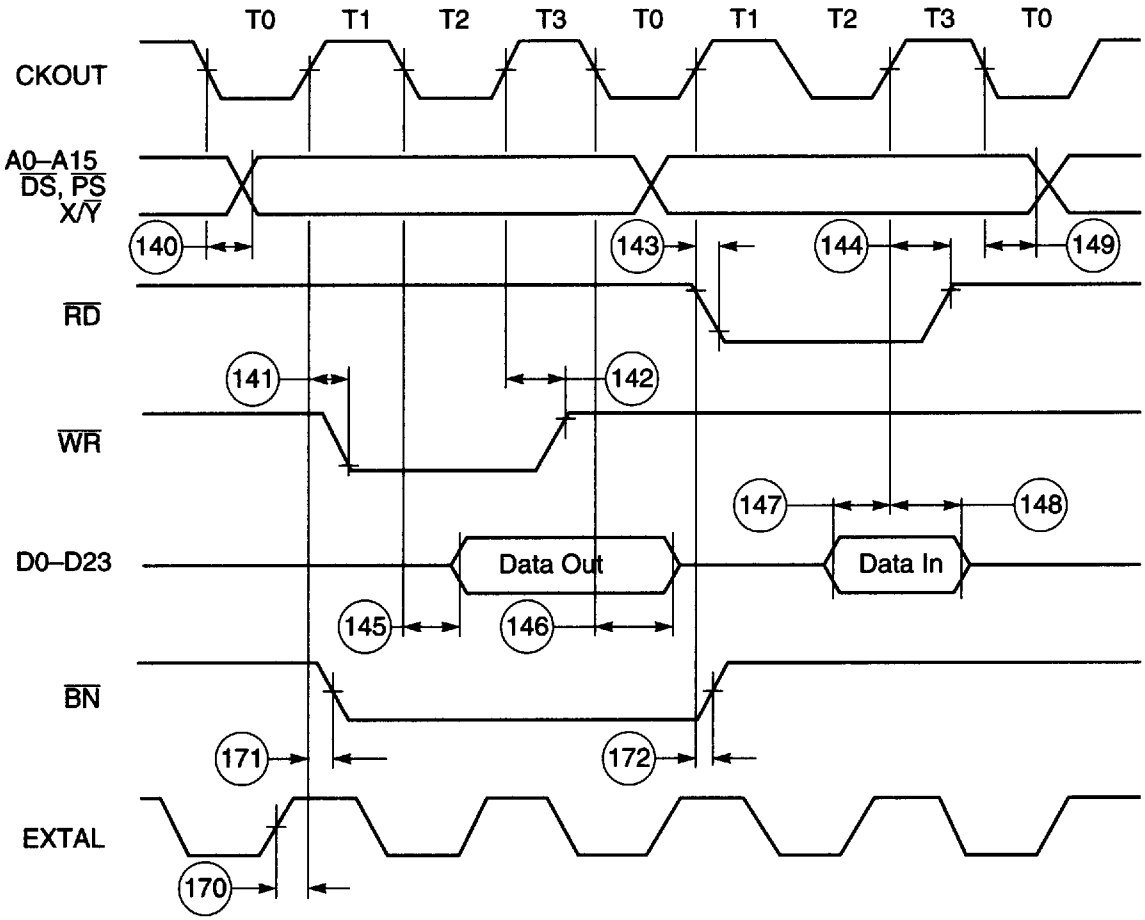
C_L = 50 pF + 2 TTL loads

Capacitance Derating: The DSP56002 external bus timing specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the external bus pins (A0–A15, D0–D23, $\overline{PS}$, $\overline{DS}$, $\overline{RD}$, $\overline{WR}$, X/$\overline{Y}$) derates linearly at 1 ns per 12 pF of additional capacitance from 50 pF to 250 pF of loading. Port B and C pins (HI, SCI, SSI, and Timer) derate linearly at 1 ns per 5 pF of additional capacitance from 50 pF to 250 pF of loading. Active-low lines should be "pulled up" in a manner consistent with the ac and dc specifications.

Table 2-13 External Bus Synchronous Timing

Num	Characteristics	40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
140	First CKOUT transition to Address Valid	—	6.2	—	5	—	5	ns
141	Second CKOUT transition to $\overline{WR}$ Assertion[1]							ns
	• WS = 0	—	4.4	—	4	—	4	ns
	• WS > 0	—	T_H + 4.4	—	T_H + 4	—	T_H + 4	
142	Second CKOUT transition to $\overline{WR}$ Deassertion	1.3	9.1	1	5	1	5	ns
143	Second CKOUT transition to $\overline{RD}$ Assertion	—	3.9	—	3.9	—	3.9	ns
144	Second CKOUT transition to $\overline{RD}$ Deassertion	0	3.4	–3	3	–3	3	ns
145	First CKOUT transition to Data-Out Valid	—	5.4	—	4.5	—	4.5	ns
146	First CKOUT transition to Data-Out Invalid[3]	0	—	0	—	0	—	ns
147	Data-In Valid to second CKOUT transition (Setup)	3.4	—	3.4	—	3.4	—	ns
148	Second CKOUT transition to Data-In Invalid (Hold)	0	—	0	—	0	—	ns
149	First CKOUT transition to Address Invalid[3]	0	—	0	—	0	—	ns

Notes:
1. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition.
2. WS are wait state values specified in the BCR.
3. First CKOUT transition to data-out invalid (specification # T146) and first CKOUT transition to address invalid (specification # T149) indicate the time after which data/address are no longer guaranteed to be valid.
4. Timings are given from CKOUT midpoint to V_{OL} or V_{OH} of the corresponding pin(s).
5. First CKOUT transition is a falling edge of CKOUT for CKP = 0.



Note: During Read-Modify-Write Instructions, the address lines do not change states. AA0395

Figure 2-23 Synchronous Bus Timing

Table 2-14 Bus Strobe/Wait Timing

No.	Characteristics	40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
150	First CKOUT transition to $\overline{BS}$ Assertion	—	5.6	—	5.6	—	5.6	ns
151	WT Assertion to first CKOUT transition (setup time)	5.3	—	5.3	—	5.3	—	ns
152	First CKOUT transition to $\overline{WT}$ Deassertion for Minimum Timing	0	$T_C - 7.9$	0	$T_C - 7.9$	0	$T_C - 6$	ns
153	$\overline{WT}$ Deassertion to first CKOUT transition for Maximum Timing (2 wait states)	7.9	—	7.9	—	6	—	ns
154	Second CKOUT transition to $\overline{BS}$ Deassertion	—	5.2	—	5.2	—	5.2	ns
155	$\overline{BS}$ Assertion to Address Valid	0	2.4	0	2.4	0	2.4	ns
156	$\overline{BS}$ Assertion to $\overline{WT}$ Assertion[1]	0	$T_C - 10.9$	0	$T_C - 10.9$	0	$T_C - 8.8$	ns
157	$\overline{BS}$ Assertion to $\overline{WT}$ Deassertion[1,3]	$(WS-1) \times T_C$	$WS \times T_C - 13.5$	$(WS-1) \times T_C$	$WS \times T_C - 13.5$	$(WS-1) \times T_C$	$WS \times T_C - 10.9$	ns
158	$\overline{WT}$ Deassertion to $\overline{BS}$ Deassertion	$T_C + T_L + 3.3$	$2 \times T_C + T_L + 7.8$	$T_C + T_L + 3.3$	$2 \times T_C + T_L + 7.8$	$T_C + T_L + 3.3$	$2 \times T_C + T_L + 7.8$	ns
159	Minimum $\overline{BS}$ Deassertion Width for Consecutive External Accesses	$T_H - 1$	—	$T_H - 1$	—	$T_H - 1$	—	ns
160	$\overline{BS}$ Deassertion to Address Invalid[2]	$T_H - 4.6$	—	$T_H - 4.6$	—	$T_H - 4.6$	—	ns
161	Data-In Valid to $\overline{RD}$ Deassertion (Set Up)	3.4	—	3.4	—	3.4	—	ns
162	$\overline{BR}$ Assertion to second CKOUT transition for Minimum Timing	9.5	T_C	9.5	T_C	9.5	T_C	ns

Table 2-14 Bus Strobe/Wait Timing (Continued)

No.	Characteristics	40 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
163	$\overline{BR}$ Deassertion to second CKOUT transition for Minimum Timing	8	T_C	8	T_C	8	T_C	ns
164	First CKOUT transition to $\overline{BG}$ Assertion	—	8.8	—	8.8	—	8.8	ns
165	First CKOUT transition to $\overline{BG}$ Deassertion	—	5.3	—	5.3	—	5.3	ns
170	EXTAL to CKOUT with PLL Disabled EXTAL to CKOUT[5] with PLL Enabled and MF < 5	3 0.3	9.7 3.7	3 0.3	9.7 3.7	3 0.3	9.7 3.7	ns ns
171	Second CKOUT transition to $\overline{BN}$ Assertion	—	5.7	—	5.7	—	5.7	ns
172	Second CKOUT transition to $\overline{BN}$ Deassertion	—	5	—	5	—	5	ns

Notes:
1. If wait states are also inserted using the BCR and if the number of wait states is greater than 2, then specification numbers T156 and T157 can be increased accordingly.
2. $\overline{BS}$ deassertion to address invalid indicates the time after which the address are no longer guaranteed to be valid.
3. The minimum number of wait states when using $\overline{BS}$/$\overline{WT}$ is two (2).
4. For read-modify-write instructions, the address lines will not change states between the read and the write cycle. However, $\overline{BS}$ will deassert before asserting again for the write cycle. If wait states are desired for each of the read and write cycle, the $\overline{WT}$ pin must be asserted once for each cycle.
5. When EXTAL frequency is less than 33 MHz, then timing T170 is not guaranteed for a period of 1000× T_C after PLOCK assertion following the events below:
   - when enabling the PLL operation by software,
   - when changing the Multiplication Factor,
   - when recovering from the Stop state if the PLL was turned off and it is supposed to turn, on
   - when exiting the Stop state.

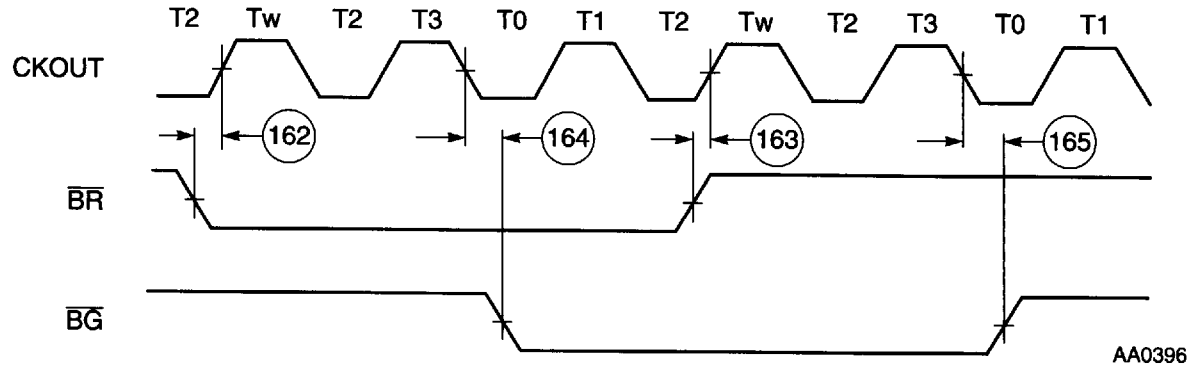
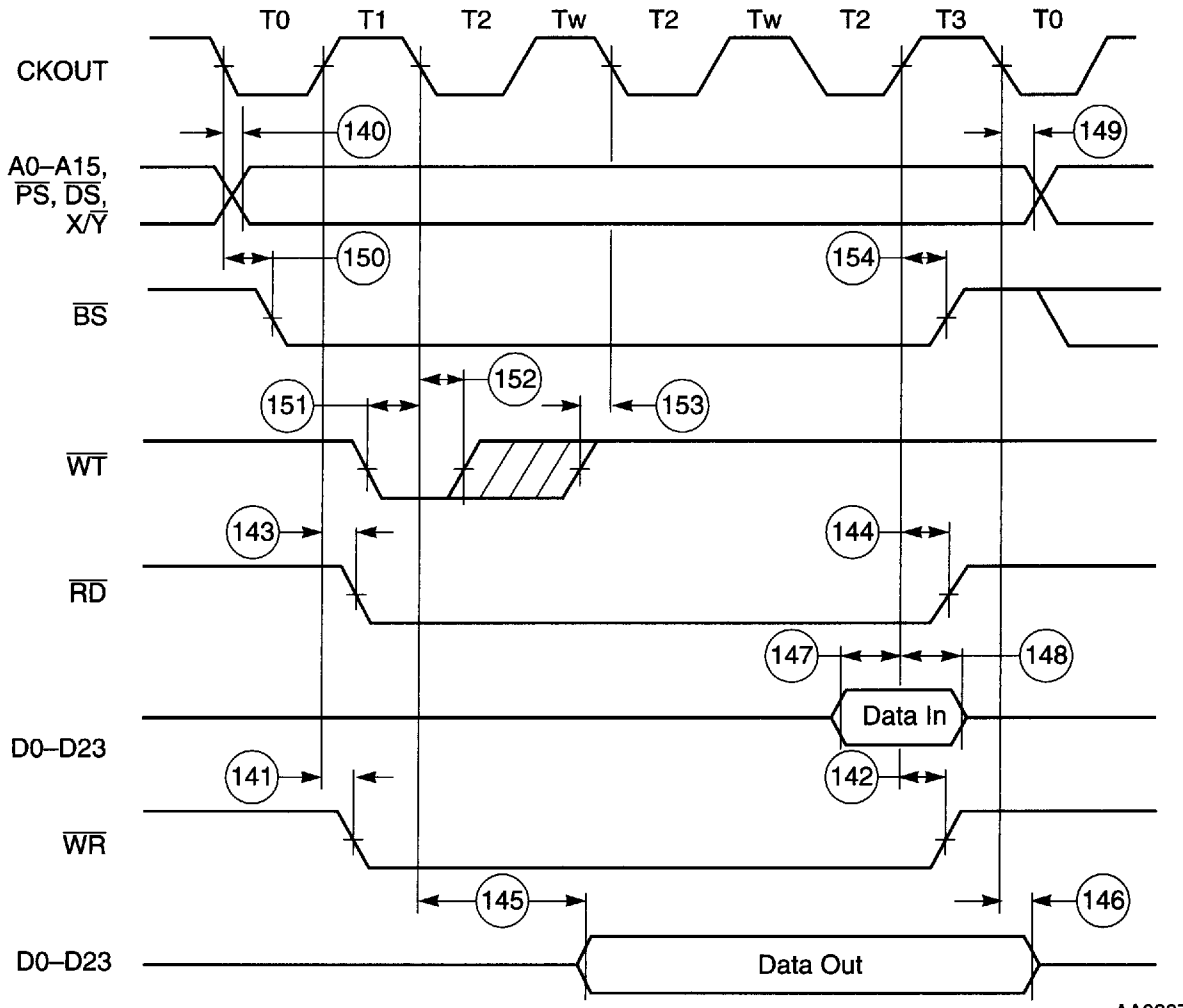
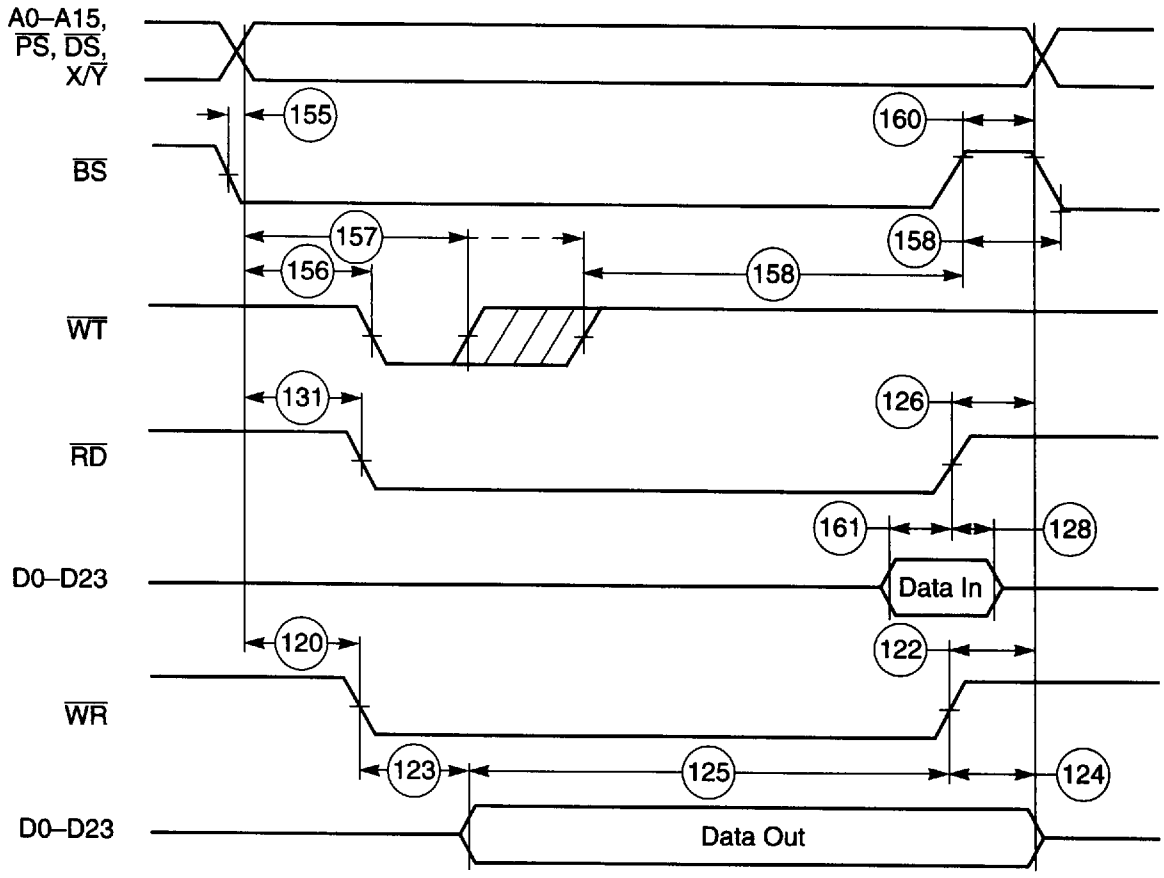


Figure 2-24 Synchronous Bus Request / Bus Grant Timing



Note: During Read-Modify-Write instructions, the address lines do not change state. However, $\overline{BS}$ will deassert before asserting again for the write cycle.

Figure 2-25 Synchronous $\overline{BS}$ / $\overline{WT}$ Timings



Note: During Read-Modify-Write instructions, the address lines do not change state. However, $\overline{BS}$ will deassert before asserting again for the write cycle.

AA0398

Figure 2-26 Asynchronous $\overline{BS}$ / $\overline{WT}$ Timings

OnCE PORT TIMING

C_L = 50 pF + 2 TTL loads

Table 2-15 OnCE Port Timing

Num	Characteristics	Min	Max	Unit
230	DSCK Low	40	—	ns
231	DSCK High	40	—	ns
232	DSCK Cycle Time	200	—	ns
233	$\overline{DR}$ Asserted to DSO ($\overline{ACK}$) Asserted	$5T_C$	—	ns
234	DSCK High to DSO Valid	—	42	ns
235	DSCK High to DSO Invalid	3	—	ns
236	DSI Valid to DSCK Low (Setup)	15	—	ns
237	DSCK Low to DSI Invalid (Hold)	3	—	ns
238	Last DSCK Low to OS0–OS1, $\overline{ACK}$ Active	$3T_C + T_L$	—	ns
239	DSO ($\overline{ACK}$) Asserted to First DSCK High	$2T_C$	—	ns
240	DSO ($\overline{ACK}$) Assertion Width	$4T_C + T_H - 3$	$5T_C + 7$	ns
241	DSO ($\overline{ACK}$) Asserted to OS0–OS1 High Impedance[2]	—	0	ns
242	OS0–OS1 Valid to second CKOUT transition	$T_C - 21$	—	ns
243	Second CKOUT transition to OS0–OS1 Invalid	0	—	ns
244	Last DSCK Low of Read Register to First DSCK High of Next Command	$7T_C + 10$	—	ns
245	Last DSCK Low to DSO Invalid (Hold)	3	—	ns
246	$\overline{DR}$ Assertion to second CKOUT transition for Wake Up from Wait state	12	T_C	ns
247	Second CKOUT transition to DSO after Wake Up from Wait state	$17T_C$	—	ns
248	$\overline{DR}$ Assertion Width • To recover from Wait state • To recover from Wait state and enter Debug mode	 15 $13T_C + 15$	 $12T_C - 15$ —	ns
249	$\overline{DR}$ Assertion to DSO ($\overline{ACK}$) Valid (enter Debug mode) After Asynchronous Recovery from Wait State	$17T_C$	—	ns
250A	$\overline{DR}$ Assertion Width to Recover from Stop state[1] • Stable External Clock, OMR Bit 6 = 0 • Stable External Clock, OMR Bit 6 = 1 • Stable External Clock, PCTL Bit 17= 1	 15 15 15	 $65548T_C + T_L$ $20T_C + T_L$ $13T_C + T_L$	 ns ns ns

Table 2-15 OnCE Port Timing

Num	Characteristics	Min	Max	Unit
250B	$\overline{DR}$ Assertion Width to Recover from Stop state and enter Debug mode[1]			
	• Stable External Clock,OMR Bit 6 = 0	$65549T_C + T_L$	—	ns
	• Stable External Clock,OMR Bit 6 = 1	$21T_C + T_L$	—	ns
	• Stable External Clock,PCTL Bit 17= 1	$14T_C + T_L$	—	ns
251	$\overline{DR}$ Assertion to DSO ($\overline{ACK}$) Valid (enter Debug mode) after recovery from Stop state[1]			
	• Stable External Clock, OMR Bit 6 = 0	$65553T_C + T_L$	—	ns
	• Stable External Clock, OMR Bit 6 = 1	$25T_C + T_L$	—	ns
	• Stable External Clock, PCTL Bit 17= 1	$18T_C + T_L$	—	ns

Notes: 1. A clock stabilization delay is required when using the on-chip crystal oscillator in two cases:
- after power-on Reset, and
- when recovering from Stop mode.

During this stabilization period, T_C, T_H, and T_L will not be constant. Since this stabilization period varies, a delay of $75{,}000 \times T_C$ is typically allowed to assure that the oscillator is stable before executing programs. While it is possible to set OMR bit 6 = 1 when using the internal crystal oscillator, it is not recommended and these specifications do not guarantee timings for that case.

2. The maximum specified is periodically sampled and not 100% tested.

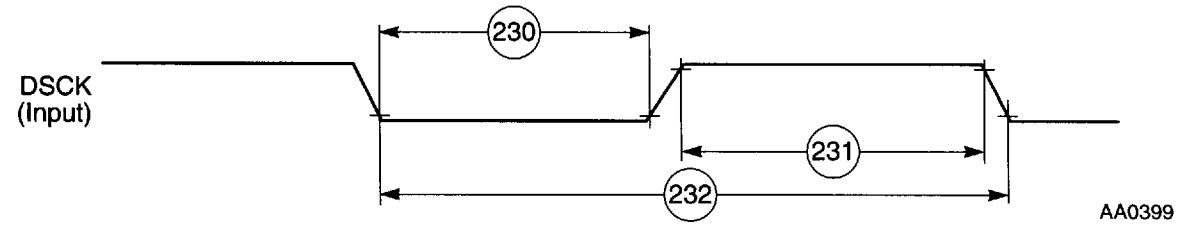


Figure 2-27 OnCE Serial Clock Timing

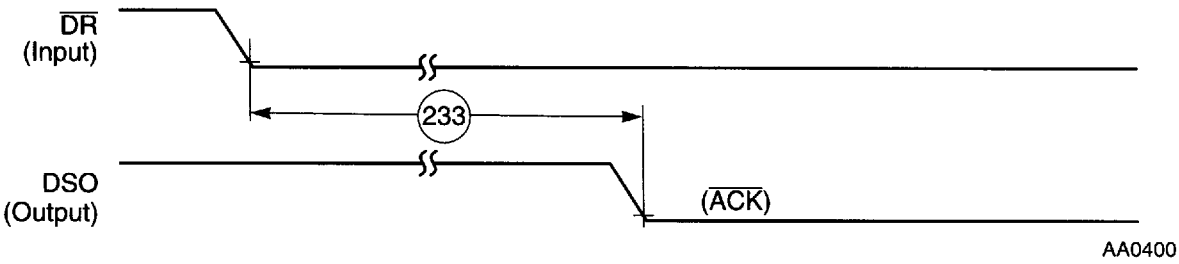
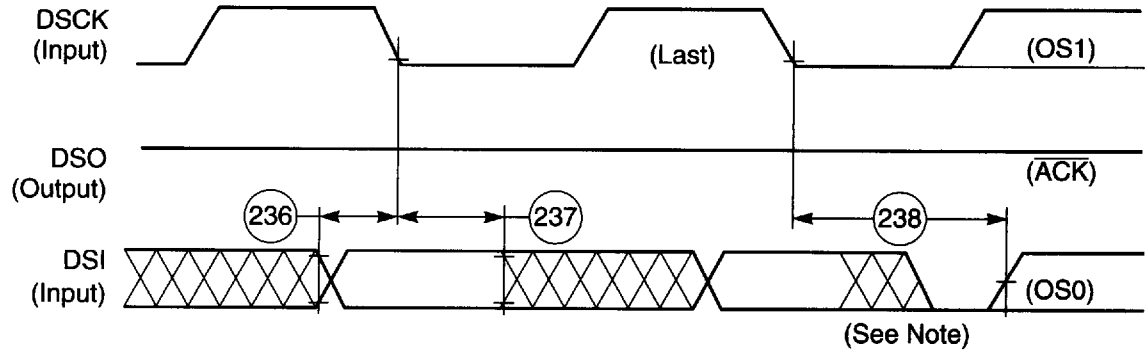


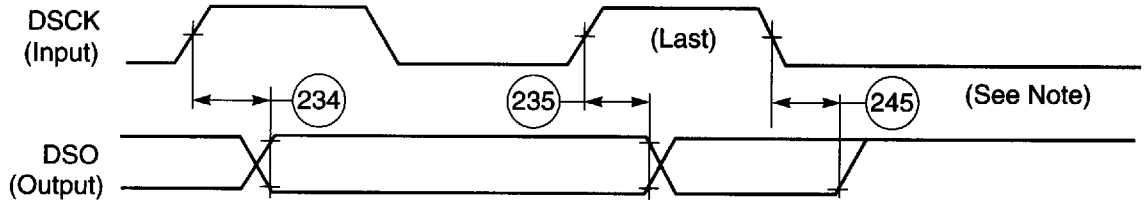
Figure 2-28 OnCE Acknowledge Timing



Note: High Impedance, external pull-down resistor

AA0501

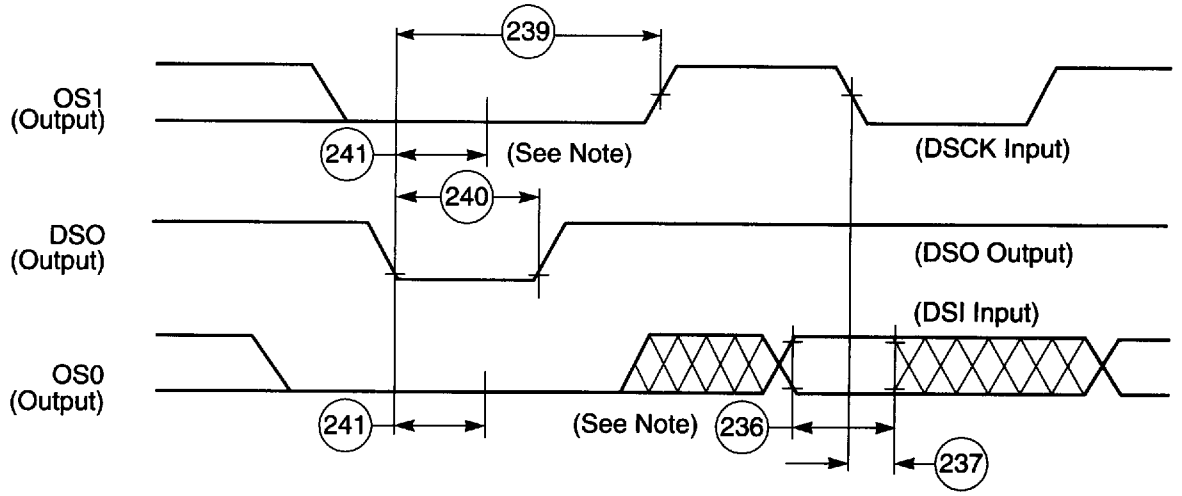
Figure 2-29 OnCE Data I/O To Status Timing



Note: High Impedance, external pull-down resistor

AA0502

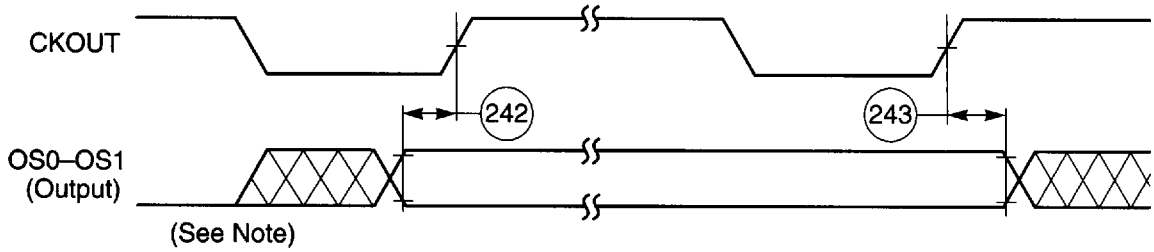
Figure 2-30 OnCE Read Timing



Note: High Impedance, external pull-down resistor

AA0503

Figure 2-31 OnCE Data I/O To Status Timing



Note: High Impedance, external pull-down resistor

Figure 2-32 OnCE CKOUT To Status Timing

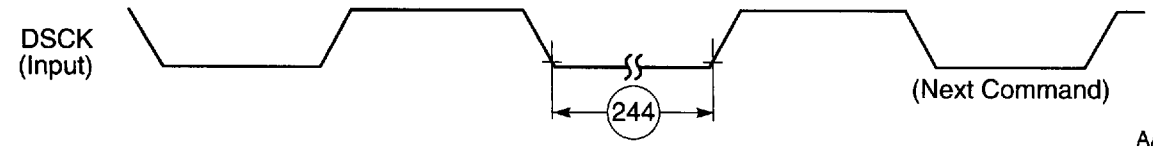


Figure 2-33 OnCE Read Register to Next Command Timing

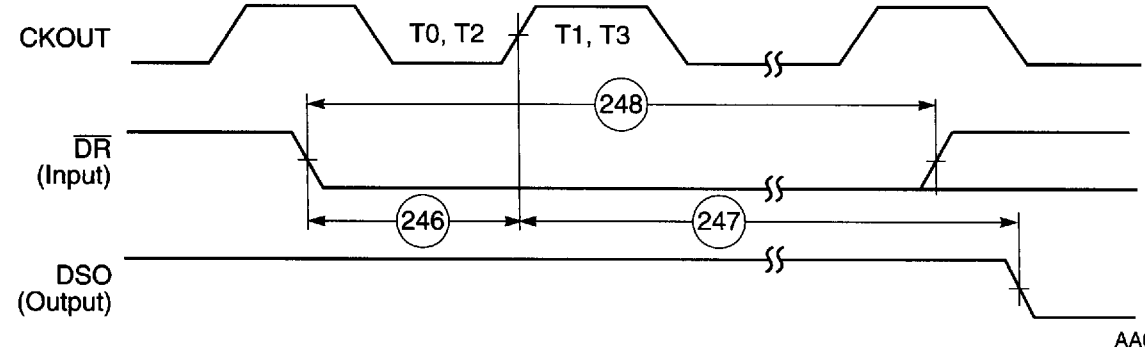


Figure 2-34 Synchronous Recovery from Wait State

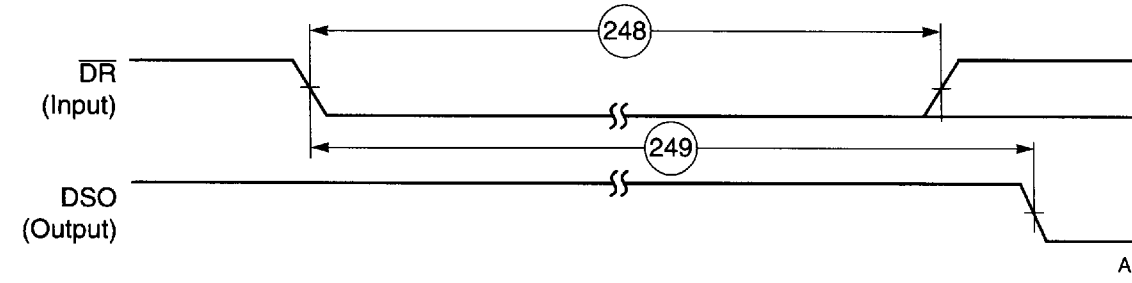


Figure 2-35 Asynchronous Recovery from Wait State

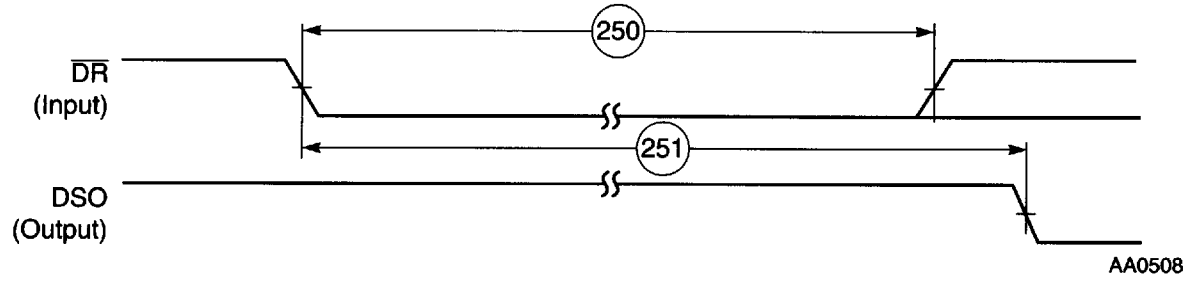


Figure 2-36 Asynchronous Recovery from Stop State

TIMER TIMING

C_L = 50 pF + 2 TTL loads

Table 2-16 Timer Timing

Num	Characteristics	Min	Max	Unit
260	TIO Low	$2T_C + 7$	—	ns
261	TIO High	$2T_C + 7$	—	ns
262	Synchronous Timer Setup Time from TIO (input) Assertion to CKOUT Rising Edge	10	T_C	ns
263	Synchronous Timer Delay Time from CKOUT Rising Edge to the External Memory Access Address Out Valid Caused by First Interrupt Instruction Execution	$5T_C + T_H$	—	ns
264	CKOUT Rising Edge to TIO (output) Assertion	0	8	ns
265	CKOUT Rising Edge to TIO (output) Deassertion	0	8	ns
266	CKOUT Rising Edge to TIO (General Purpose Output)	0	8	ns

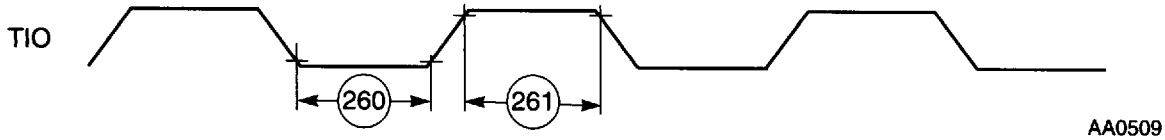


Figure 2-37 TIO Timer Event Input

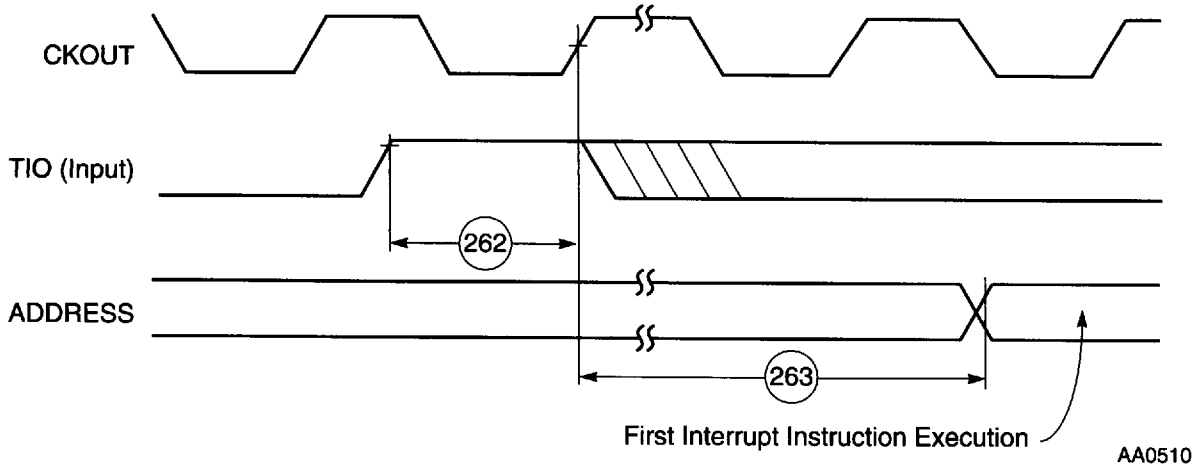


Figure 2-38 Timer Interrupt Generation

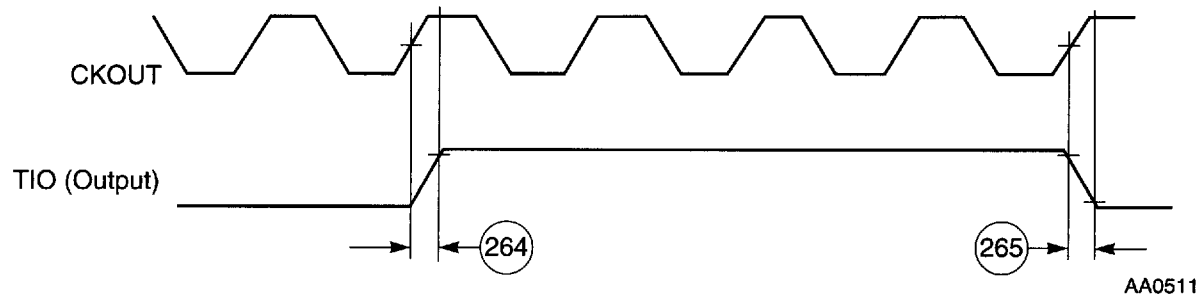


Figure 2-39 External Pulse Generation

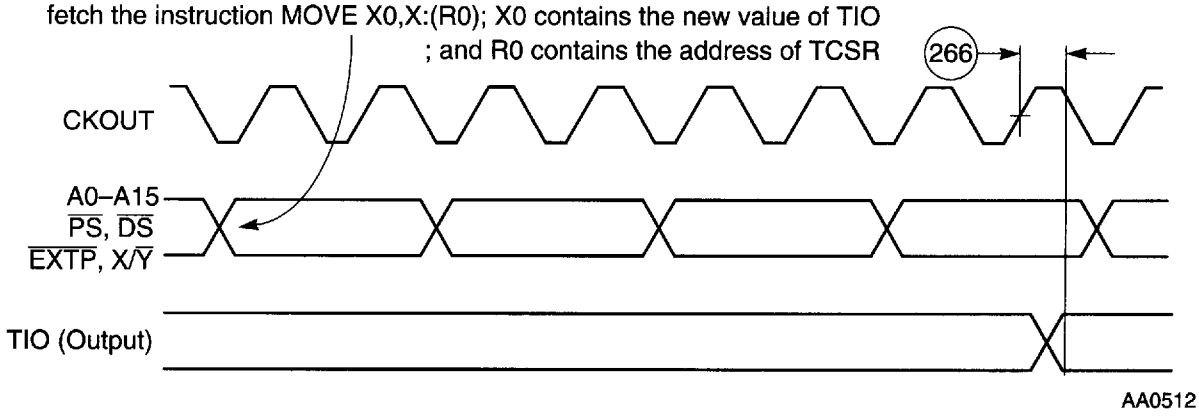


Figure 2-40 GPIO Output Timing