82375EB/82375SB PCI-EISA BRIDGE (PCEB)

- Provides the Bridge Between the PCI Local Bus and EISA Bus
- 100% PCI and EISA Compatible
  - PCI and EISA Master/Slave Interface
  - Directly Drives 10 PCI Loads and 8 EISA Slots
  - Supports PCI from 25 to 33 MHz
- Data Buffers Improve Performance
  - Four 32-bit PCI-to-EISA Posted Write Buffers
  - Four 16-byte EISA-to-PCI Read/Write Line Buffers
  - EISA-to-PCI Read Prefetch
  - EISA-to-PCI and PCI-to-EISA Write Posting
- Data Buffer Management Ensures Data Coherency
  - Flush Posted Write Buffers
  - Flush or Invalidate Line Buffers
  - System-Wide Data Buffer Coherency Control
- Burst Transfers on both the PCI and EISA Buses
- 32-Bit Data Paths
- Integrated EISA Data Swap Buffers
- Arbitration for PCI Devices
  - Supports Six PCI Masters
  - Fixed, Rotating, or a Combination of the Two
  - Supports External PCI Arbiter and Arbiter Cascading
- PCI and EISA Address Decoding and Mapping
  - Positive Decode of Main Memory Areas (MEMCS# Generation)
  - Four Programmable PCI Memory Space Regions
  - Four Programmable PCI I/O Space Regions
- Programmable Main Memory Address Decoding
  - Main Memory Sizes up to 512 MBytes
  - Access Attributes for 15 Memory Segments in First 1 MByte of Main Memory
  - Programmable Main Memory Hole
- Integrated 16-bit BIOS Timer
- Only Available as Part of a Supported Kit

The 82375EB/SB PCI-EISA Bridge (PCEB) provides the master/slave functions on both the PCI Local Bus and the EISA Bus. Functioning as a bridge between the PCI and EISA buses, the PCEB provides the address and data paths, bus controls, and bus protocol translation for PCI-to-EISA and EISA-to-PCI transfers. Extensive data buffering in both directions increases system performance by maximizing PCI and EISA Bus efficiency and allowing concurrency on the two buses. The PCEB's buffer management mechanism ensures data coherency. The PCEB integrates central bus control functions including a programmable bus arbiter for the PCI Bus and EISA data swap buffers for the EISA Bus. Integrated system functions include PCI parity generation, system error reporting, and programmable PCI and EISA memory and I/O address space mapping and decoding. The PCEB also contains a BIOS Timer that can be used to implement timing loops. The PCEB is intended to be used with the EISA System Component (ESC) to provide an EISA I/O subsystem interface.

This document describes both the 82375EB and 82375SB components. Unshaded areas describe the 82375EB. Shaded areas, like this one, describe the 82375SB operations that differ from the 82375EB.

This complete document is available from Intel's World Wide Website and/or U.S. Literature Center:

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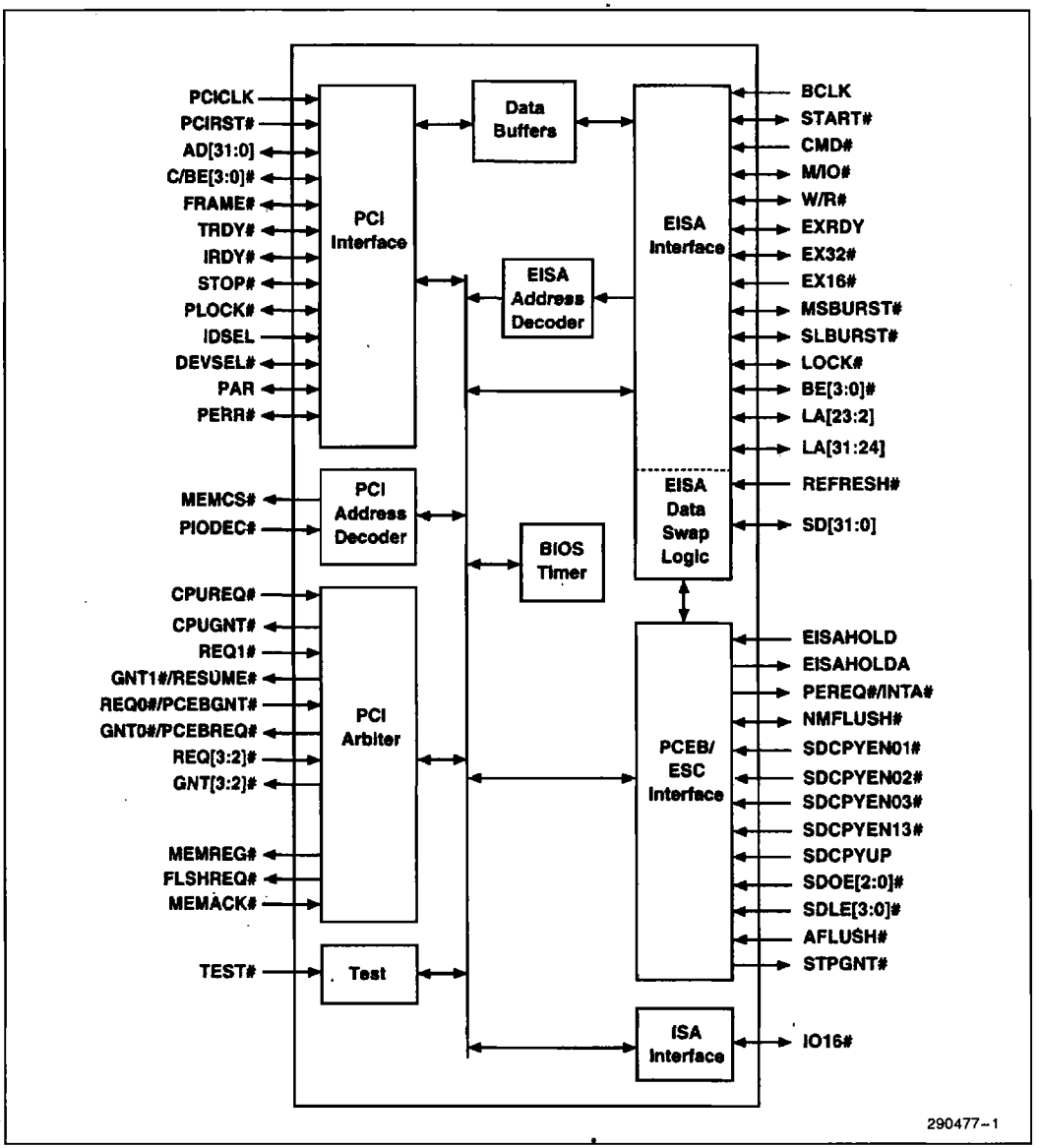
March 1996 Order Number: 290477-004



PCEB Simplified Block Diagram