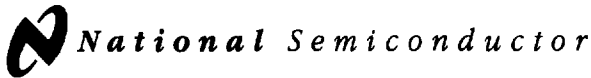


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DS26C32AT/DS26C32AM

Quad Differential Line Receiver

General Description

The DS26C32A is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

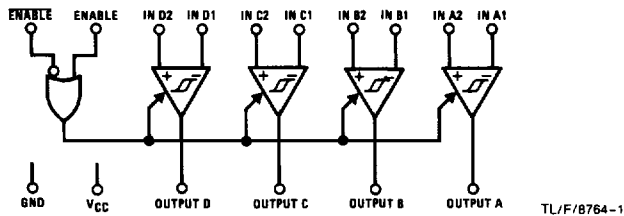
The DS26C32A has an input sensitivity of 200 mV over the common mode input voltage range of $\pm 7V$. The DS26C32A features internal pull-up and pull-down resistors which prevent output oscillation on unused channels.

The DS26C32A provides an enable and disable function common to all four receivers, and features TRI-STATE® outputs with 6 mA source and sink capability. This product is pin compatible with the DS26LS32A and the AM26LS32.

Features

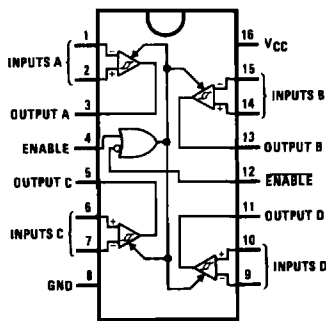
- CMOS design for low power
- $\pm 0.2V$ sensitivity over input common mode voltage range
- Typical propagation delays: 19 ns
- Typical input hysteresis: 60 mV
- Inputs won't load line when $V_{CC} = 0V$
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses
- Available in Surface Mount
- Mil-Std-883C compliant

Logic Diagram



Connection Diagrams

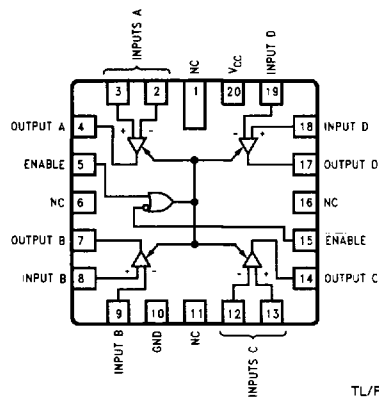
Dual-In-Line Package



TL/F/8764-2

Top View

20-Lead Ceramic Leadless Chip Carrier



TL/F/8764-12

Order Number DS26C32ATJ, DS26C32ATM or DS26C32ATN

See NS Package J16A, M16A or N16E
For Complete Military 883 Specifications,
See RETS Data Sheet.

Order Number DS26C32AME/883, DS26C32AMJ/883 or DS26C32AMW/883

See NS Package E20A, J16A or W16A

Truth Table

ENABLE	ENABLE	Input	Output
L	H	X	Z
All Other Combinations of Enable Inputs		$V_{ID} \geq V_{TH} (Max)$	H
		$V_{ID} \leq V_{TH} (Min)$	L
		Open	H

Z = TRI-STATE

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Common Mode Range (V_{CM})	$\pm 14V$
Differential Input Voltage (V_{DIFF})	$\pm 14V$
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	$-65^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (Soldering 4 sec.)	$260^{\circ}C$
Maximum Power Dissipation at $25^{\circ}C$ (Note 5)	
Ceramic "J" Pkg.	2308 mW
Plastic "N" Pkg.	1645 mW
SOIC "M" Pkg.	1190 mW
Ceramic "E" Pkg.	2108 mW
Ceramic "W" Pkg.	1215 mW

Maximum Current Per Output ± 25 mA

This device does not meet 2000V ESD rating. (Note 4)

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature Range (T_A)			
DS26C32AT	-40	$+85$	$^{\circ}C$
DS26C32AM	-55	$+125$	$^{\circ}C$
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$	-200	35	+200	mV	
R_{IN}	Input Resistance	$V_{IN} = -7V, +7V$ (Other Input = GND)	DS26C32AT	5.0	6.8	10	k Ω
			DS26C32AM	4.5	6.8	11	k Ω
I_{IN}	Input Current	$V_{IN} = +10V$, Other Input = GND	DS26C32AT		+1.1	+1.5	mA
			DS26C32AM		+1.1	+1.8	mA
		$V_{IN} = -10V$, Other Input = GND	DS26C32AT		-2.0	-2.5	mA
			DS26C32AM		-2.0	-2.7	mA
V_{OH}	Minimum High Level Output Voltage	$V_{CC} = \text{Min}$, $V_{DIFF} = +1V$ $I_{OUT} = -6.0$ mA	3.8	4.2		V	
V_{OL}	Maximum Low Level Output Voltage	$V_{CC} = \text{Max}$, $V_{DIFF} = -1V$ $I_{OUT} = 6.0$ mA		0.2	0.3	V	
V_{IH}	Minimum Enable High Input Level Voltage		2.0			V	
V_{IL}	Maximum Enable Low Input Level Voltage				0.8	V	
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, ENABLE = V_{IL} , ENABLE = V_{IH}		± 0.5	± 5.0	μA	
I_I	Maximum Enable Input Current	$V_{IN} = V_{CC}$ or GND			± 1.0	μA	
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max}$, $V_{DIF} = +1V$	DS26C32AT	16	23	mA	
			DS26C32AM	16	25	mA	
V_{HYST}	Input Hysteresis	$V_{CM} = 0V$		60		mV	

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max		Units
					DS26C32AT	DS26C32AM	
t_{PLH} , t_{PHL}	Propagation Delay Input to Output	$C_L = 50 \text{ pF}$ $V_{DIFF} = 2.5V$ $V_{CM} = 0V$	10	19	30	35	ns
t_{RISE} , t_{FALL}	Output Rise and Fall Times	$C_L = 50 \text{ pF}$ $V_{DIFF} = 2.5V$ $V_{CM} = 0V$		4	9	9	ns
t_{PLZ} , t_{PHZ}	Propagation Delay ENABLE to Output	$C_L = 50 \text{ pF}$ $R_L = 1000\Omega$ $V_{DIFF} = 2.5V$		13	22	29	ns
t_{PZL} , t_{PZH}	Propagation Delay ENABLE to Output	$C_L = 50 \text{ pF}$ $R_L = 1000\Omega$ $V_{DIFF} = 2.5V$		13	23	29	ns

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Unless otherwise specified, Min/Max limits apply over recommended operating conditions. All typicals are given for $V_{CC} = 5V$ and $T_A = 25^\circ\text{C}$.

Note 4: ESD Rating: HBM (1.5 k Ω , 100 pF)
Inputs $\geq 2000V$
All other pins $\geq 1000V$
EIAJ (0 Ω , 200 pF) $\geq 350V$

Note 5: Ratings apply to ambient temperature at 25°C . Above this temperature derate N Package 13.16 mW/ $^\circ\text{C}$, J Package 15.38 mW/ $^\circ\text{C}$, M Package 9.52 mW/ $^\circ\text{C}$, E Package 12.04 mW/ $^\circ\text{C}$, and W package 6.94 mW/ $^\circ\text{C}$.

Comparison Table of Switching Characteristics into "LS-Type" Load

(Figures 4, 5, and 6) (Note 6)

Symbol	Parameter	Conditions	DS26C32A	DS26LS32A	Units
			Typ	Typ	
t_{PLH} t_{PHL}	Input to Output	$C_L = 15 \text{ pF}$	17 19	23 23	ns ns
t_{LZ} t_{HZ}	ENABLE to Output	$C_L = 5 \text{ pF}$	13 12	15 20	ns ns
t_{ZL} t_{ZH}	ENABLE to Output	$C_L = 15 \text{ pF}$	13 13	14 15	ns ns

Note 6: This table is provided for comparison purposes only. The values in this table for the DS26C32A reflect the performance of the device, but are not tested or guaranteed.

Test and Switching Waveforms

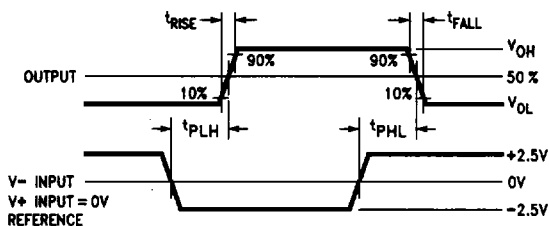
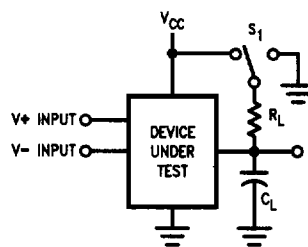


FIGURE 1. Propagation Delay

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C_L includes load and test jig capacitance.
 S₁ = V_{CC} for t_{PZL} and t_{PLZ} measurements.
 S₁ = Gnd for t_{PZH} and t_{PHZ} measurements.

FIGURE 2. Test Circuit for TRI-STATE Output Tests

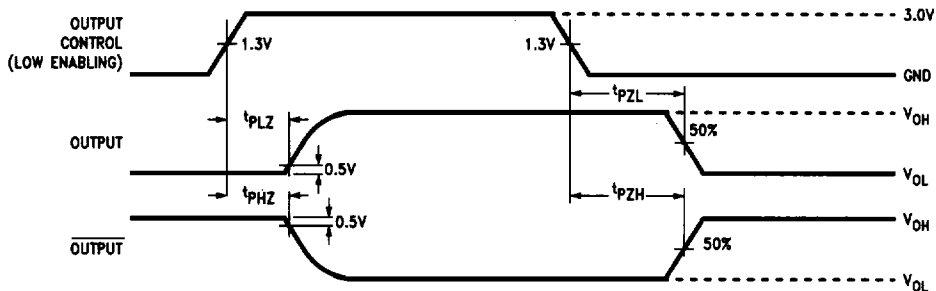
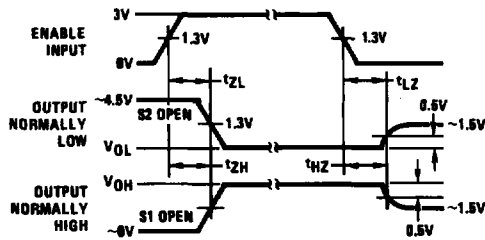
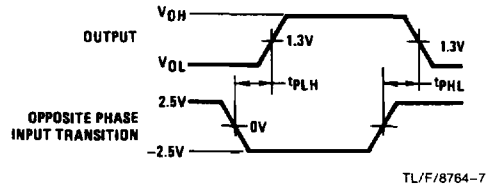
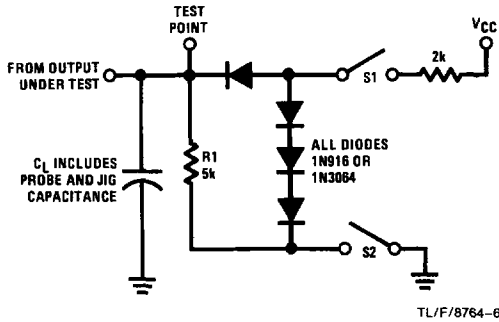


FIGURE 3. TRI-STATE Output Enable and Disable Waveforms

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AC Test Circuit and Switching Time Waveforms



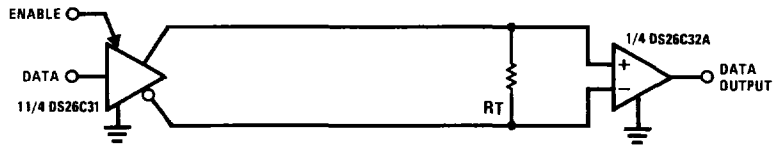
Note 7: Diagram shown for ENABLE low.

Note 8: S1 and S2 of load circuit are closed except where shown.

Note 9: Pulse generator for all pulses: Rate \leq 1.0 MHz; $Z_O = 50\Omega$; $t_r \leq 15$ ns; $t_f \leq 6.0$ ns.

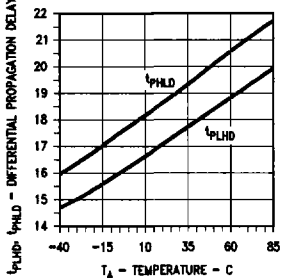
Typical Applications

Two-Wire Balanced Systems, RS-422

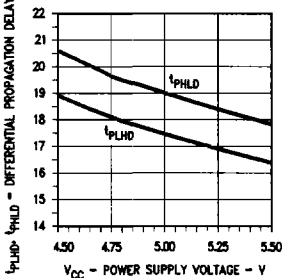


Typical Performance Characteristics

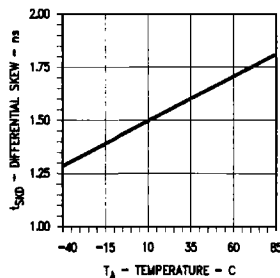
Differential Propagation Delay vs Temperature



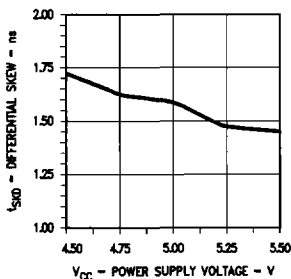
Differential Propagation Delay vs Power Supply Voltage



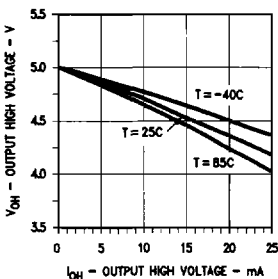
Differential Skew vs Temperature



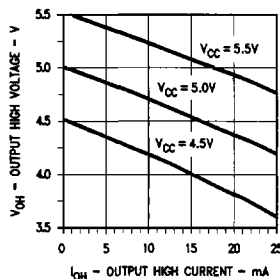
Differential Skew vs Power Supply Voltage



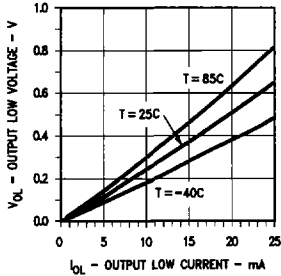
Output High Voltage vs Output High Current



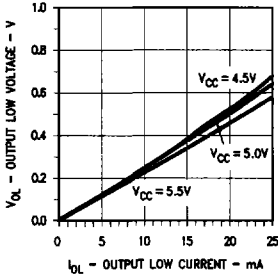
Output High Voltage vs Output High Current



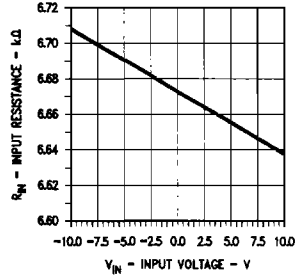
Output Low Voltage vs Output Low Current



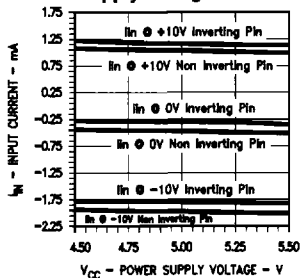
Output Low Voltage vs Output Low Current



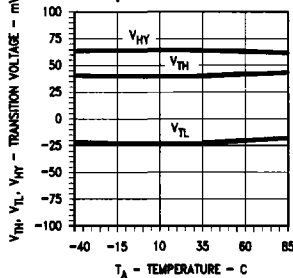
Input Resistance vs Input Voltage



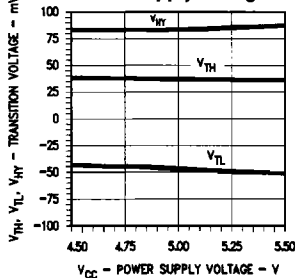
Input Current vs Power Supply Voltage



Hysteresis & Differential Transition Voltage vs Temperature

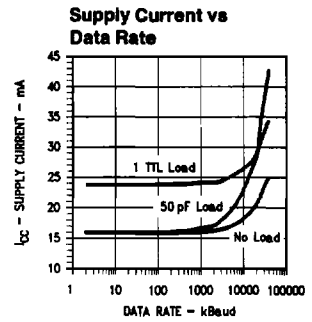
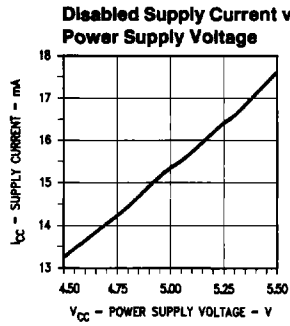
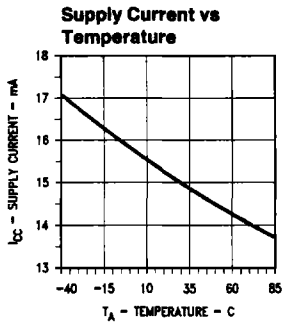


Hysteresis & Differential Transition Voltage vs Power Supply Voltage



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Typical Performance Characteristics (Continued)



TL/F/8764-11