MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

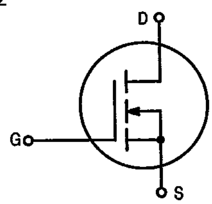
MRF163

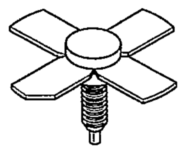
The RF MOSFET Line
RF Power Field Effect Transistor
N-Channel Enhancement-Mode

25 W, to 400 MHz
N-CHANNEL MOS
BROADBAND RF POWER
FET

. . . designed for wideband large-signal output and driver applications up to 400 MHz range.

- Guaranteed 28 Volt, 400 MHz Performance
  Output Power = 25 Watts
  Minimum Gain = 10 dB
  Efficiency — 50% (Typical)
- Small-Signal and Large-Signal Characterization
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 2.5 dB (Typ) at 500 mA, 400 MHz
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques





CASE 244, STYLE 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	87.5 0.5	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{θJC}$	2.0	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	4.0	mAdc
Gate-Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 500 mA)	g_{fs}	500	750	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	48	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	54	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	11	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DS} = 28 Vdc, I_D = 500 mA, f = 400 MHz, Z_S = 3.23 + j2.57 Ω, Z_L = 2.11 + j2.97 Ω)	NF	—	2.5	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 25 W, f = 400 MHz, I_{DQ} = 25 mA)	G_{ps}	10	12	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 25 W, f = 400 MHz, I_{DQ} = 25 mA)	η	45	50	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 25 W, f = 400 MHz, I_{DQ} = 25 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

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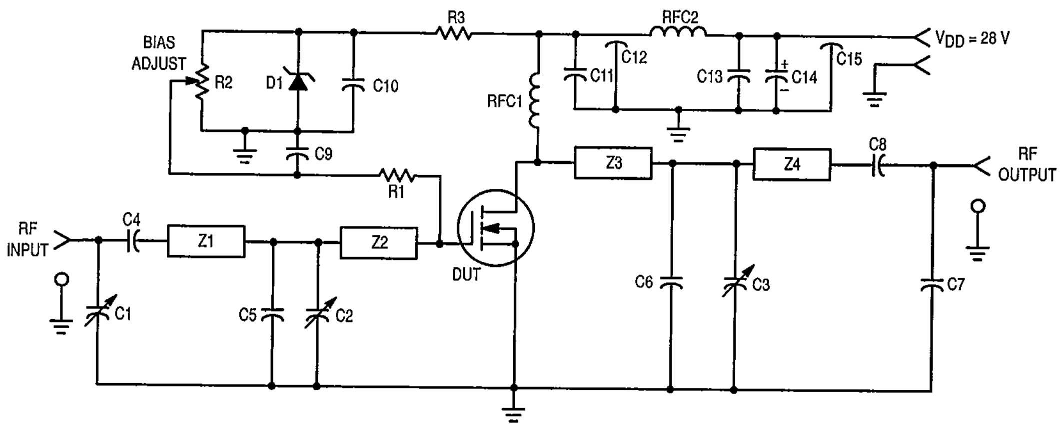

C1, C2, C3 — 1.0–20 pF Johanson or Equivalent
C4, C8 — 270 pF, 100 Mil Chip Cap
C5, C6 — 18 pF Mini-Unelco or Equivalent
C7 — 12 pF Mini-Unelco or Equivalent
C9 — 0.01 μF, 50 V Disc Ceramic
C10, C11, C13 — 0.1 μF, 50 V Disc Ceramic
C12, C15 — 680 pF Feedthru
C14 — 20 μF, 50 V
D1 — 1N5925A Motorola Zener
R1 — 10 kΩ, 1/4 W
R2 — 10 Turns 10 kΩ
R3 — 1.6 kΩ, 1/4 W
RFC1 — 10 Turns, 0.300″ ID #20 AWG Enamel Closewound
RFC2 — Ferroxcube VK-200 — 19/4B
Z1 — 1.350″ x 0.250″ Microstrip
Z2 — 0.600″ x 0.250″ Microstrip
Z3 — 0.710″ x 0.250″ Microstrip
Z4 — 1.300″ x 0.250″ Microstrip
Board — Glass Teflon, 62 Mils, ϵ_r = 2.56

Figure 1. 400 MHz Test Circuit

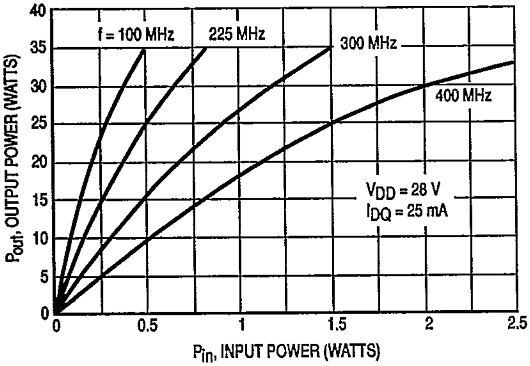

Figure 2. Output Power versus Input Power

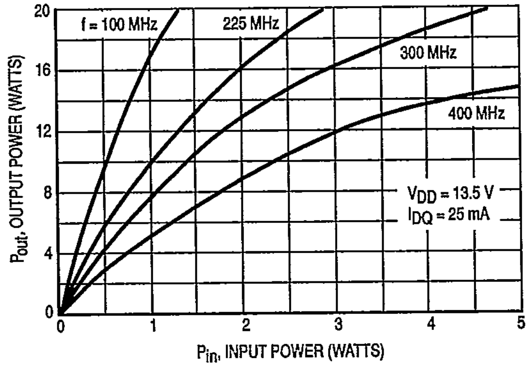

Figure 3. Output Power versus Input Power

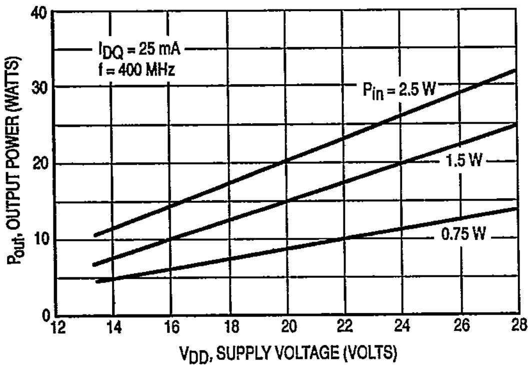

Figure 4. Output Power versus Supply Voltage

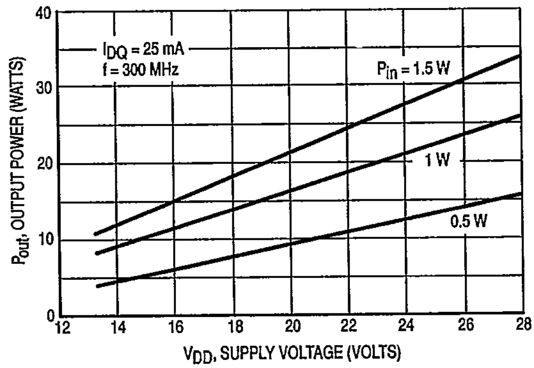

Figure 5. Output Power versus Supply Voltage

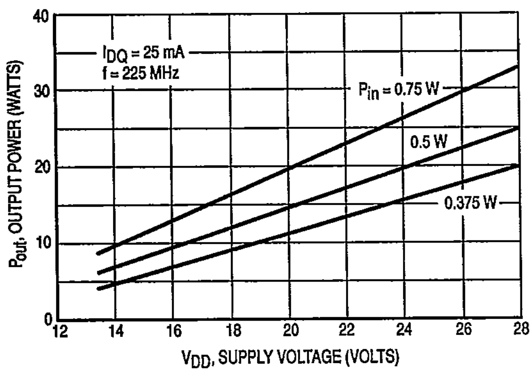

Figure 6. Output Power versus Supply Voltage

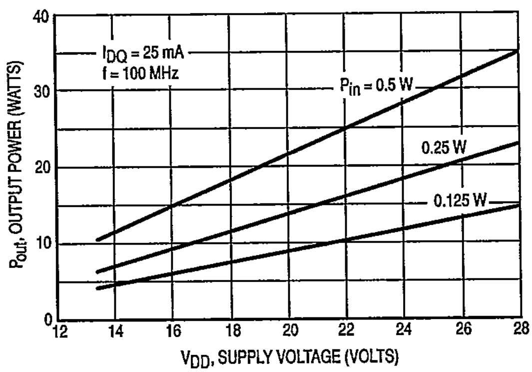

Figure 7. Output Power versus Supply Voltage

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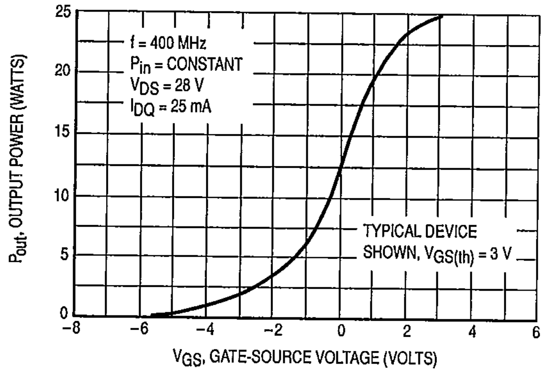

Figure 8. Output Power versus Gate Voltage

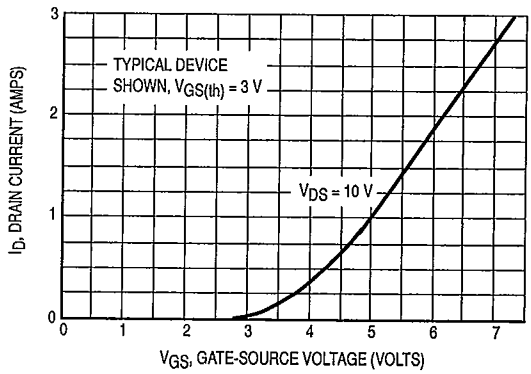

Figure 9. Drain Current versus Gate Voltage (Transfer Characteristics)

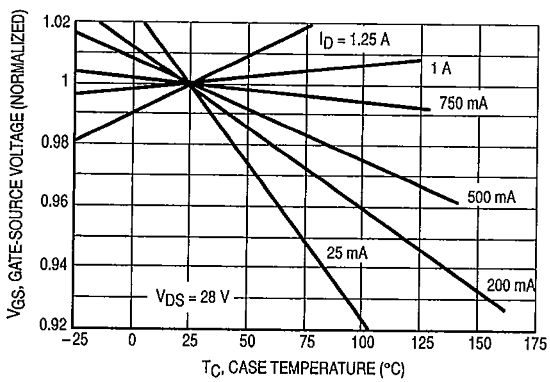

Figure 10. Gate-Source Voltage versus Case Temperature

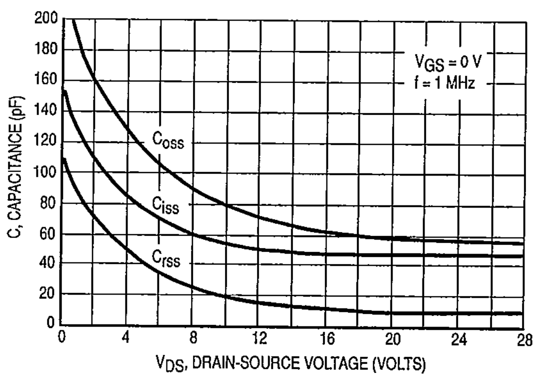

Figure 11. Capacitance versus Drain-Source Voltage

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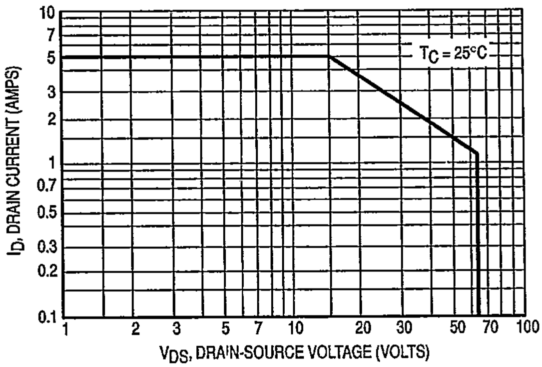
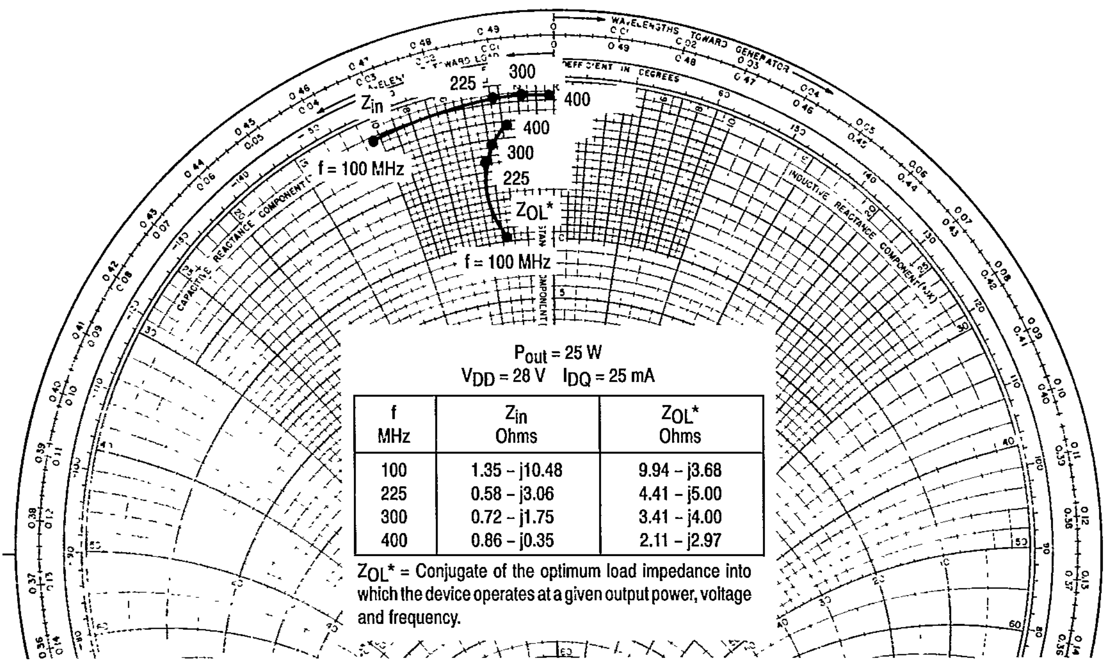


Figure 12. DC Safe Operating Area



P_{out} = 25 W
V_{DD} = 28 V I_{DQ} = 25 mA

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
100	1.35 – j10.48	9.94 – j3.68
225	0.58 – j3.06	4.41 – j5.00
300	0.72 – j1.75	3.41 – j4.00
400	0.86 – j0.35	2.11 – j2.97

Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

Figure 13. Input and Output Impedance

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
2.0	0.985	−30	56.97	166	0.010	63.9	0.611	−36
10	0.875	−105	34.12	125	0.032	30.6	0.736	−116
25	0.841	−145	16.17	104	0.038	9.2	0.798	−152
50	0.833	−162	8.201	92.7	0.038	1.6	0.800	−165
75	0.836	−167	5.496	86.8	0.037	−2.5	0.802	−168
100	0.838	−170	4.121	82.3	0.039	−3.0	0.804	−170
125	0.838	−171	3.255	78.6	0.039	−5.8	0.809	−170
150	0.840	−172	2.718	74.3	0.037	−8.5	0.815	−171
175	0.844	−173	2.326	70.8	0.037	−9.6	0.819	−171
200	0.849	−173	2.027	67.2	0.036	−10.4	0.824	−171
225	0.851	−173	1.782	64.0	0.036	−10.3	0.833	−171
250	0.857	−173	1.593	60.9	0.034	−11.7	0.839	−171
275	0.862	−173	1.438	58.9	0.035	−11.1	0.844	−171
300	0.866	−173	1.319	55.6	0.033	−12.1	0.846	−170
325	0.872	−173	1.209	52.3	0.032	−12.7	0.861	−170
350	0.875	−173	1.110	49.0	0.031	−13.4	0.873	−170
375	0.879	−173	1.030	46.7	0.031	−12.2	0.876	−170
400	0.882	−173	0.966	44.1	0.030	−14.6	0.883	−170
425	0.888	−173	0.904	41.3	0.029	−13.4	0.888	−170
450	0.891	−173	0.836	39.4	0.028	−11.7	0.895	−170
475	0.893	−173	0.792	37.1	0.027	−8.8	0.902	−170
500	0.901	−173	0.748	35.2	0.027	−6.1	0.911	−170
525	0.906	−173	0.715	32.4	0.025	−6.0	0.921	−170
550	0.911	−173	0.679	30.2	0.024	−6.0	0.928	−170
575	0.912	−173	0.637	28.7	0.024	−3.9	0.934	−170
600	0.913	−173	0.605	26.9	0.024	−1.0	0.939	−170
625	0.919	−174	0.579	25.3	0.024	1.0	0.947	−170
650	0.921	−174	0.566	23.0	0.025	10.1	0.961	−170
675	0.927	−174	0.540	22.6	0.025	12.1	0.963	−170
700	0.927	−174	0.510	19.9	0.025	16.5	0.966	−170
725	0.927	−173	0.485	19.5	0.025	23.1	0.967	−170
750	0.933	−174	0.481	17.4	0.026	25.3	0.967	−170
775	0.937	−174	0.453	17.2	0.028	28.0	0.976	−170
800	0.942	−174	0.448	16.8	0.030	33.8	0.976	−170

Table 1. Common Source Scattering Parameters 50 Ohm System
V_{DS} = 28 V, I_D = 0.5 A

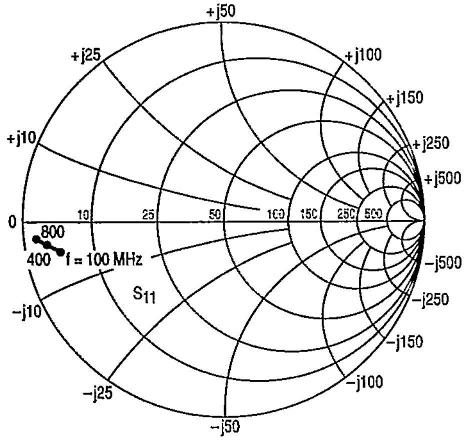


Figure 14. S_{11}, Input Reflection Coefficient versus Frequency
V_{DS} = 28 V, I_D = 0.5 A

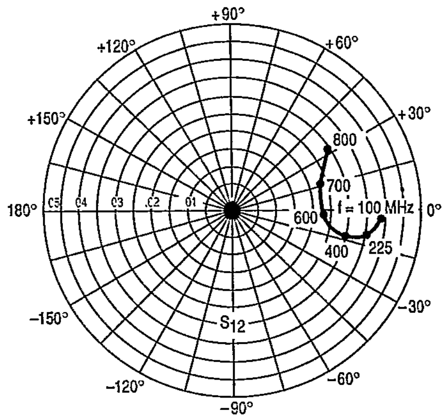


Figure 15. S_{12}, Reverse Transmission Coefficient versus Frequency
V_{DS} = 28 V, I_D = 0.5 A

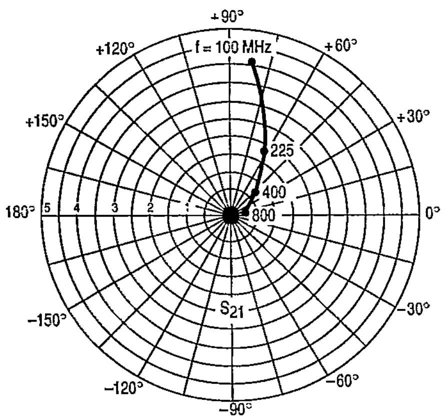


Figure 16. S_{21}, Forward Transmission Coefficient versus Frequency
V_{DS} = 28 V, I_D = 0.5 A

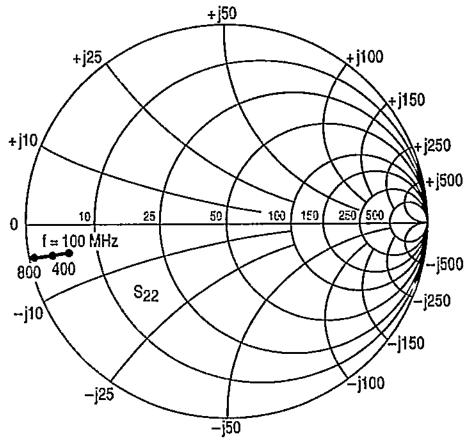


Figure 17. S_{22}, Output Reflection Coefficient versus Frequency
V_{DS} = 28 V, I_D = 0.5 A

DESIGN CONSIDERATIONS

The MRF163 is a RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for UHF power amplifier and oscillator applications. Motorola RF MOSFETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF163 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF163 was characterized at I_{DQ} = 25 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

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The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF163 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar UHF transistors are suitable for MRF163. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOSFETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF163, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Two port parameter stability analysis with the MRF163 s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A for a discussion of two port network theory and stability.

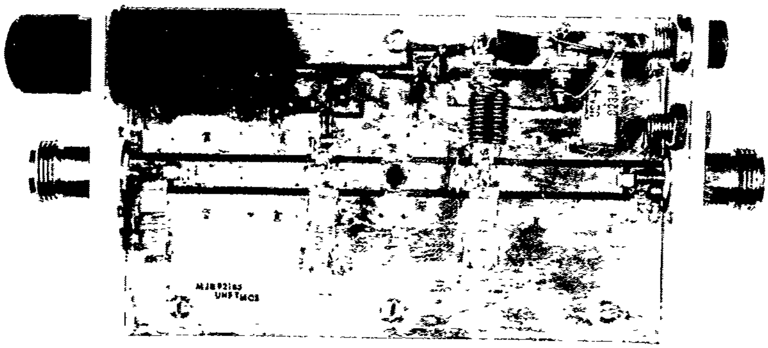

Figure 18. 400 MHz Test Circuit