1ED44171N01B

Single-channel low-side gate driver IC

Features

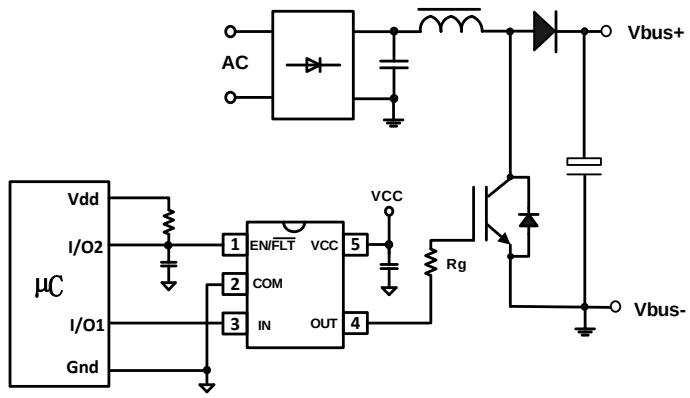
- CMOS Schmitt-triggered inputs
- Under voltage lockout
- Single pin for fault output and enable
- Programmable fault clear time
- 3.3 V, 5 V and 15 V input logic compatible
- 25 V VCC voltage supply support (max)
- Output in phase with input
- -10 Vdc negative input capability of “IN” pin
- 3 kV ESD HBM
- RoHS compliant

Potential applications

- PFC stages
- Home appliances
- Air conditioner
- Industrial applications
- General purpose low-side gate driver for single-ended topologies

Description

The 1ED44171N01B is a low-voltage, power devices (such as: IGBT, MOSFET) non-inverting gate driver. Proprietary latch-up immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output driver features a current buffer stage. The 1ED44171N01B provides an under-voltage lockout protection and has a FAULT status output (when activated, EN/$\overline{\text{FLT}}$ pin is internally pulled down). The EN/$\overline{\text{FLT}}$ needs to be externally pulled up to provide normal operation, pulling EN/$\overline{\text{FLT}}$ low disables the driver. The under-voltage lockout protection holds the output low until VCC supply voltage is within operating range.



(Refer to lead assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to our application notes and design tips for proper circuit board layout.

Figure 1 Typical application

Ordering information

Product type	Package	Standard pack		Orderable part number
		Form	Quantity	
1ED44171N01B	PG-SOT23-5-1	Tape and Reel	3000	1ED44171N01BXTSA1

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47/22 and J-STD-020.

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1 Block diagram

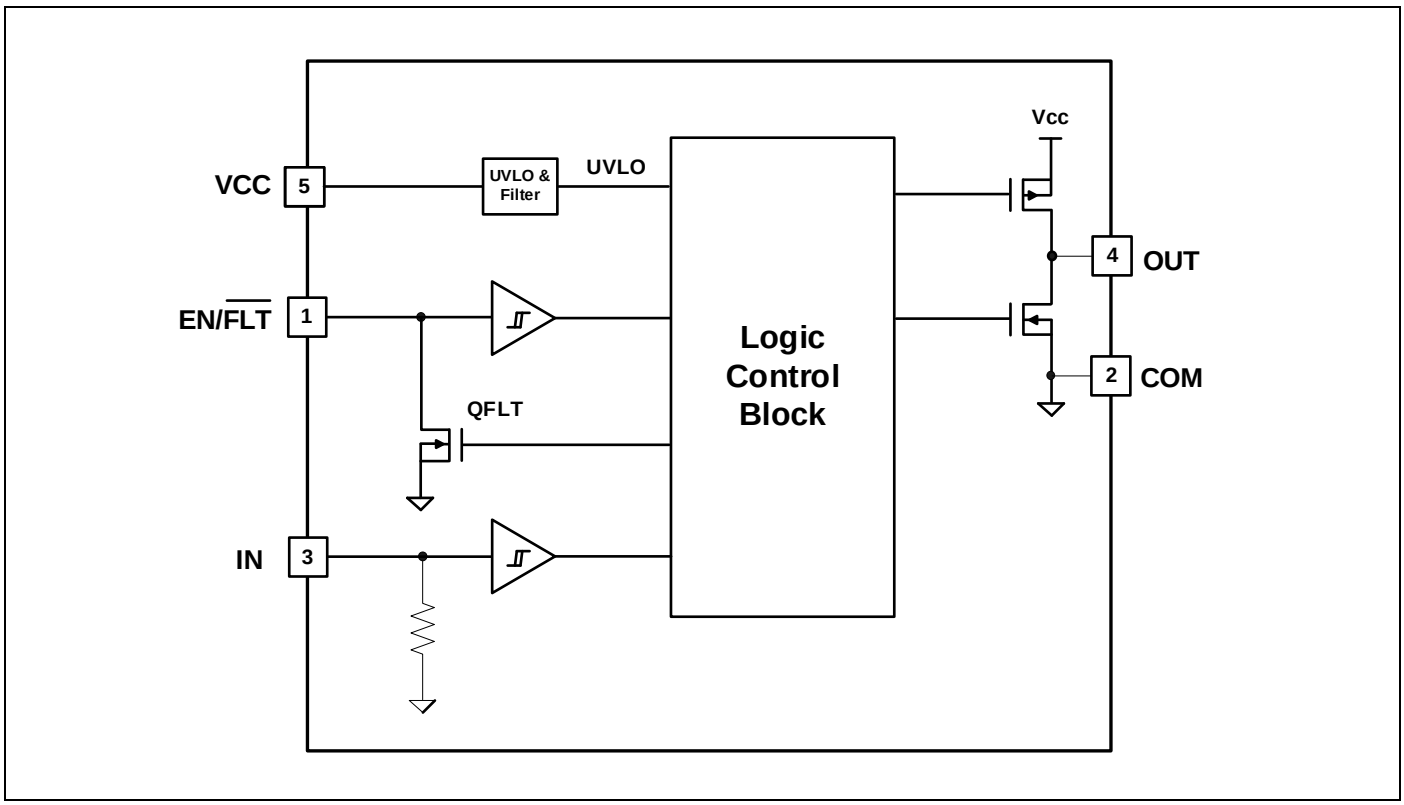


Figure 2 Block diagram

2 Pin configuration and functionality

2.1 Pin configuration

Table 1 Pin configuration

Pin no.	Name	Function
1	EN/$\overline{\text{FLT}}$	Enable, fault reporting and fault clear time program pin, three functions: 1. Logic input to enable I/O functionality. I/O logic functions when ENABLE is high. 2. Fault reporting function with undervoltage lockout, this pin has negative logic and an open-drain output. 3. Fault clear time program with external resistor and capacitor.
2	COM	Ground
3	IN	Logic input for gate driver output (OUT), in phase
4	OUT	Gate drive output
5	VCC	Supply Voltage

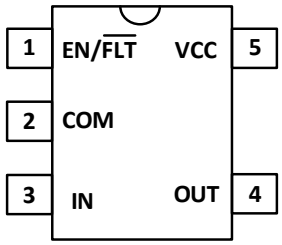


Figure 3 PG-SOT23-5-1 (top view)

2.2 Input/output logic truth table

Table 2 Input/output logic truth table

IN	UVLO[1)]	$EN/\overline{FLT}$ [2)]	OUT	Note
L	H	H	L	OUT = L
H	H	H	H	OUT = H
X	L	L	L	OUT = L and $EN/\overline{FLT}$= L (UVLO protection will disable input signal and internally pull down $EN/\overline{FLT}$ pin.)
X	H	L	L	OUT = L (Externally pull down $EN/\overline{FLT}$ pin will disable I/O logic until $EN/\overline{FLT}$ returns to high level.)

1) UVLO “L” state is under-voltage protection.

2) $EN/\overline{FLT}$ “H” state is $EN/\overline{FLT}$ pin externally pulling up and internally pull down MOSFET (QFLT) is off. (See Block Diagram.)

3 Qualification information

Qualification level		Industrial [1] Comments: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.
Moisture sensitivity level		MSL1 [2] 260°C (per JEDEC standard J-STD-020)
ESD	Charged device model	1.5 kV (per ANSI/ESDA/JEDEC standard JS-002)
	Human body model	3 kV (per ANSI/ESDA/JEDEC standard JS-001)
IC latch-up test		Class II, Level A (per JESD78)
RoHS compliant		Yes

1) Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.

2) Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

4 Electrical parameters

4.1 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. The device may not function or not be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Table 3 Absolute maximum ratings

Symbol	Definition		Min	Max	Units
VCC	Fixed supply voltage		– 0.3	25	V
V_O	Output voltage (OUT)		- 0.3	VCC + 0.3	
$V_{EN/\overline{FLT}}$	Voltage at enable and fault reporting pin ($EN/\overline{FLT}$)		– 0.3	VCC + 0.3	
V_{IN}	Logic input voltage (IN)		– 10	VCC + 0.3	
P_D	Package power dissipation @ $T_A \leq 25°C$	PG-SOT23-5	—	0.5	W
Rth_{JA}	Thermal resistance, junction to ambient		—	191	°C/W
T_J	Junction temperature		– 40	150	°C
T_S	Storage temperature		– 55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	260	

4.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table.

Table 4 Recommended operating conditions

Symbol	Definition	Min	Max	Units
VCC	Fixed supply voltage	12.7	20	V
V_O	Output voltage	COM	VCC	
$V_{EN/\overline{FLT}}$	Voltage at enable and fault reporting pin ($EN/\overline{FLT}$)	0	VCC	
V_{IN}	Logic input voltage (IN)	– 5	VCC	
T_A	Ambient temperature	– 40	125	°C

4.3 Static electrical characteristics

VCC = 15V, T_A = 25°C unless otherwise specified. The V_{INL}, V_{INH}, V_{ENL}, V_{ENH}, and I_{IN}, $I_{\overline{FLT}}$ parameters are referenced to COM and are applicable to input leads: IN and EN/$\overline{FLT}$. The V_O and I_O parameters are referenced to COM and are applicable to the output lead: OUT.

Table 5 Static electrical characteristics

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
VCC_{UV+}	VCC supply undervoltage positive going threshold	11.2	11.9	12.7	V	
VCC_{UV-}	VCC supply undervoltage negative going threshold	10.3	11	11.8		
VCC_{UVH}	VCC supply undervoltage lockout hysteresis	—	0.9	—		
V_{INL}	Logic “0” input voltage (OUT = LO)	0.8	1.0	1.2		
V_{INH}	Logic “1” input voltage (OUT = HI)	1.9	2.1	2.3		
V_{ENL}	Logic “0” disable voltage	0.8	1.0	1.2		
V_{ENH}	Logic “1” enable voltage	1.9	2.1	2.3		
V_{OH}	High level output voltage, VCC -V_{OUT}	—	0.02	0.1		I_O = 2 mA
V_{OL}	Low level output voltage, V_{OUT}	—	0.02	0.1		I_O = 2 mA
I_{IN+}	Logic “1” input bias current IN pin	35	50	70	µA	V_{IN} = 5 V
I_{IN-}	Logic “0” input bias current IN pin	-10	- 6	—		V_{IN} = 0 V
I_{QCC}	Quiescent VCC supply current	—	700	1200		V_{IN} = 0 V or 5 V
I_{O+}	Output sourcing short circuit pulsed current	2	2.6	—	A	V_O = 0 V, PW ≤ 2 µs
I_{O-}	Output sinking short circuit pulsed current	2	2.6	—		V_O = 15 V, PW ≤ 2 µs
$I_{\overline{FLT}}$	EN/$\overline{FLT}$ pull down sinking current	18	—	—	mA	$V_{EN/\overline{FLT}}$ = 0.4 V
V_{ACTSD}	Active shut down voltage	—	2.0	2.3	V	VCC = open, I_{OUT-}/I_{O-} = 0.1

4.4 Dynamic electrical characteristics

VCC = 15 V, T_A = 25°C, and C_L = 1000 pF unless otherwise specified.

Table 6 Dynamic electrical characteristics

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	50	75	ns	Figure 6 V_{IN} pulse = 5 V
t_{off}	Turn-off propagation delay	—	50	75		
t_r	Turn-on rise time	—	5	—		
t_f	Turn-off fall time	—	5	—		
t_{DISA}	Disable propagation delay	—	50	75		Figure 11 V_{EN} pulse = 5 V
t_{FLTC}	FAULT clear time	80	103	130	µs	Figure 8 VCC = 3.3 V R_{FLTC} = 1MΩ to Vdd, C_{FLTC} = 150pF to COM
tv_{CCUV}	VCC supply UVLO filter time *	—	2	—	µs	Figure 8

*Parameter verified by design, not tested in production.

5 Application information and additional details

Information regarding the following topics is included as subsections within this section of the datasheet.

- Low side gate driver
- Switching and timing relationships
- Input logic compatibility
- Undervoltage lockout protection
- Fault reporting and programmable fault clear timer
- Enable input

5.1 Low side gate driver

The 1ED44171N01B is designed to drive the gate of power devices (such as: IGBT, MOSFET). Figure 4 and Figure 5 illustrate several parameters associated with the gate driver functionality of the driver. The output current of the driver, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{OUT}.

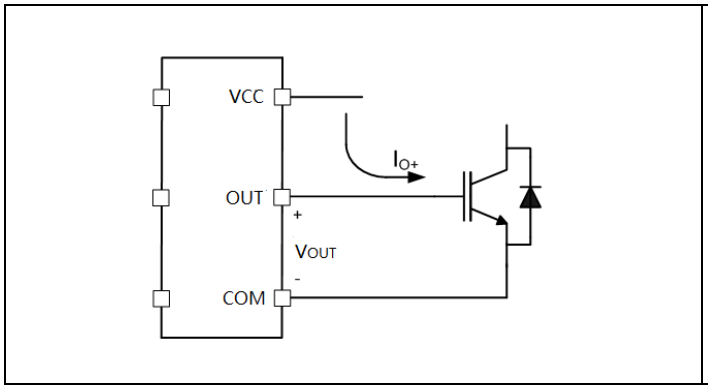


Figure 4 Gate output sourcing current

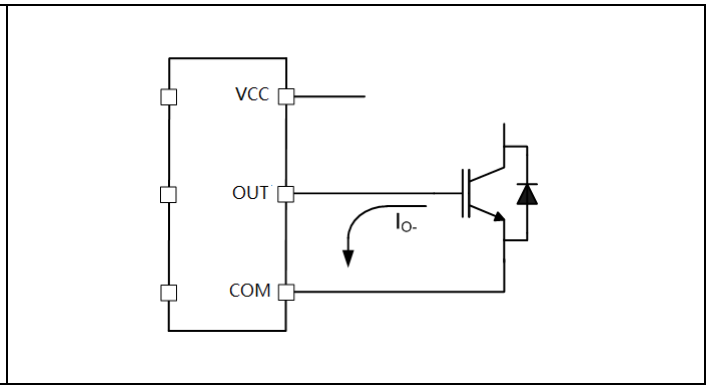


Figure 5 Gate output sinking current

5.2 Switching and timing relationships

The relationships between the input and output signals of the 1ED44171N01B are illustrated below Figure 6. From the figure, we can see the definitions of several timing parameters (i.e. t_{on}, t_{off}, t_r, and t_f) associated with this device.

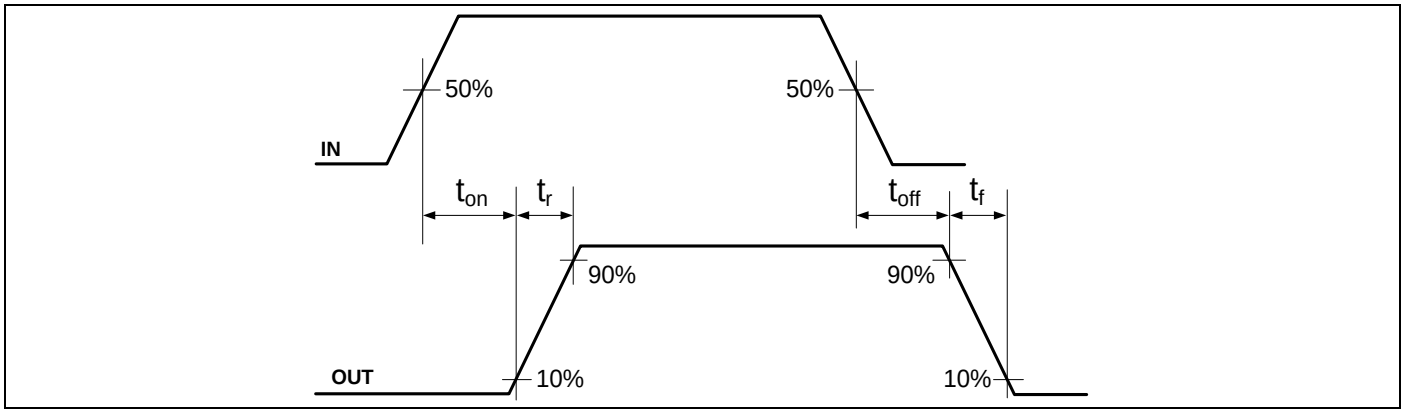


Figure 6 Switching time waveforms

5.3 Input logic compatibility

The input of this IC is compatible with standard CMOS and TTL outputs. The 1ED44171N01B has been designed to be compatible with 3.3 V, 5 V and 15 V logic-level signals. The input high threshold (V_{INH}) is typ. 2.1 V and low threshold (V_{INL}) is typ. 1 V. Input hysteresis offers enhanced noise immunity. The 1ED44171N01B includes an important feature: wherein, whenever the input pin is in a floating condition, the output is held in the low state. This is achieved using GND pull-down resistors on the input pin. Figure 7 illustrates an input signal to the 1ED44171N01B, its input threshold values, and the logic state of the IC as a result of the input signal.

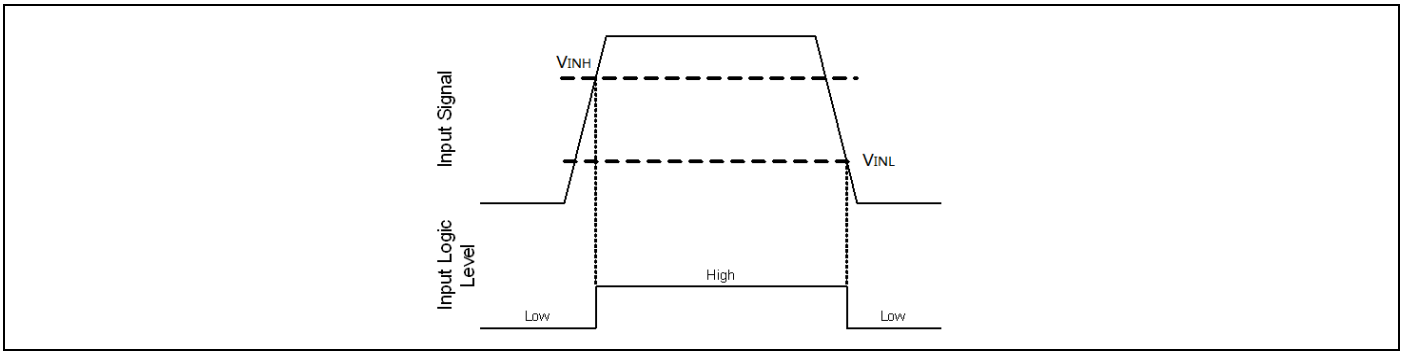


Figure 7 IN input thresholds

5.4 Undervoltage lockout (VCC)

The 1ED44171N01B has internal UVLO protection feature on the VCC pin supply circuit blocks. When VCC bias voltage keeps lower than the V_{CCUV-} threshold more than UVLO filter time (t_{VCCUV}), the VCC UVLO feature holds the output low, regardless of the status of the IN input.

At the same time, the internal MOSFET Q_{FLT} turns on and the EN/$\overline{\text{FLT}}$ pin is internally pulled down to COM. The EN/$\overline{\text{FLT}}$ output stays in the low state until the UVLO has been removed; once the UVLO is removed, the internal MOSFET Q_{FLT} turns off, and the voltage on the EN/$\overline{\text{FLT}}$ pin is charged up by external voltage Vdd.

And when VCC is higher than V_{CCUV+} and longer than fault clear time (t_{FLTC}), the OUT still keeps low until next input signal IN is high. (See Figure 8)

The filter time (t_{VCCUV}) of about 2 µs helps to suppress noise from the UVLO circuit, so that negative going voltage spikes at the supply pin will avoid parasitic UVLO events.

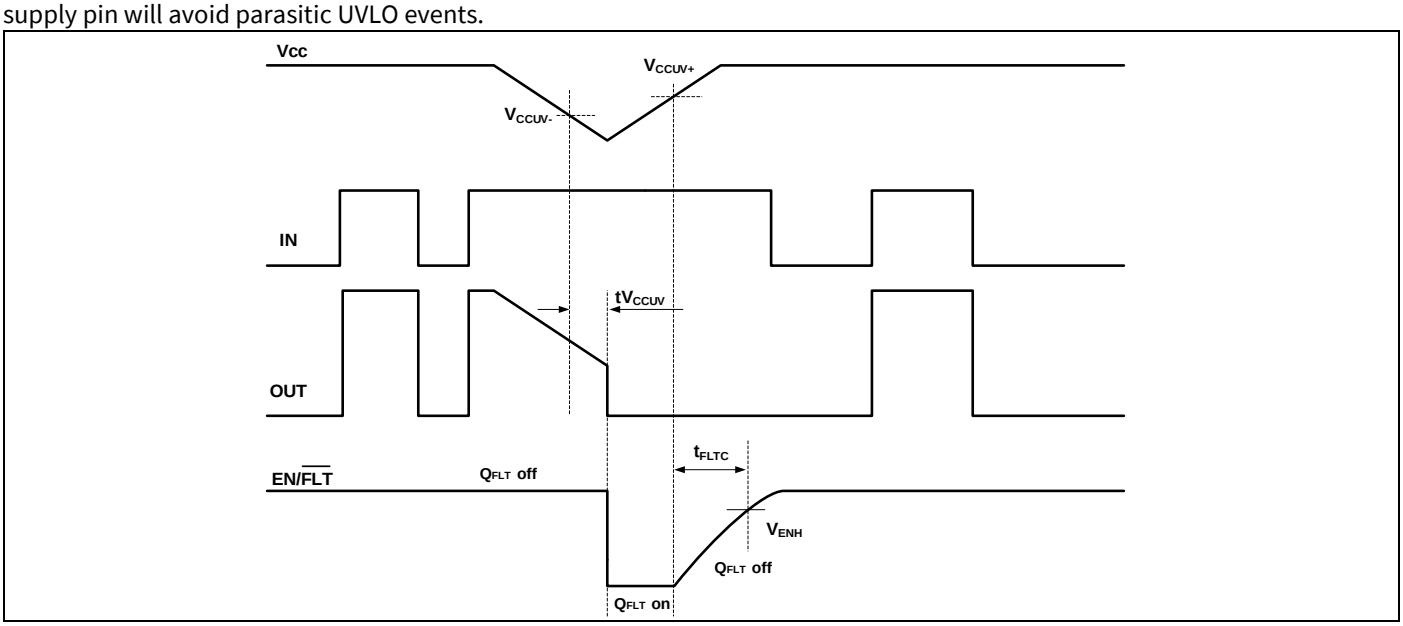


Figure 8 VCC under voltage protection waveform definitions

5.5 Fault reporting and programmable fault clear timer

The 1ED44171N01B provides an integrated fault reporting output and an adjustable fault clear timer at the under voltage condition of VCC. Once the under voltage of VCC occurs, the EN/$\overline{\text{FLT}}$ pin is internally pulled to COM. The EN/$\overline{\text{FLT}}$ output stays in the low state until the fault condition has been removed and the internal pull down NMOS Q_{FLT} turns off, the voltage on the EN/$\overline{\text{FLT}}$ pin is charged up with external pull-up voltage.
The length of the fault clear time period (t_{FLTC}) is determined by exponential charging characteristics of the capacitor where the time constant is set by R_{FLTC} and C_{FLTC}. Figure 9 shows that R_{FLTC} is connected between the external supply (Vdd) and the EN/$\overline{\text{FLT}}$ pin, while C_{FLTC} is placed between the EN/$\overline{\text{FLT}}$ and COM pins. EN/$\overline{\text{FLT}}$ is weakly pulled up to 3.3 V reference voltage with 2.15 M resistor internally. So the length of the fault clear time period can be determined by using the formula below (If Vdd = 3.3 V).

$$t_{FLTC} = -\left(\frac{R_{FLTC} \times 2.15M}{R_{FLTC} + 2.15M}\right) \times C_{FLTC} \times \ln\left(1 - \frac{V_{ENH}}{V_{dd}}\right)$$

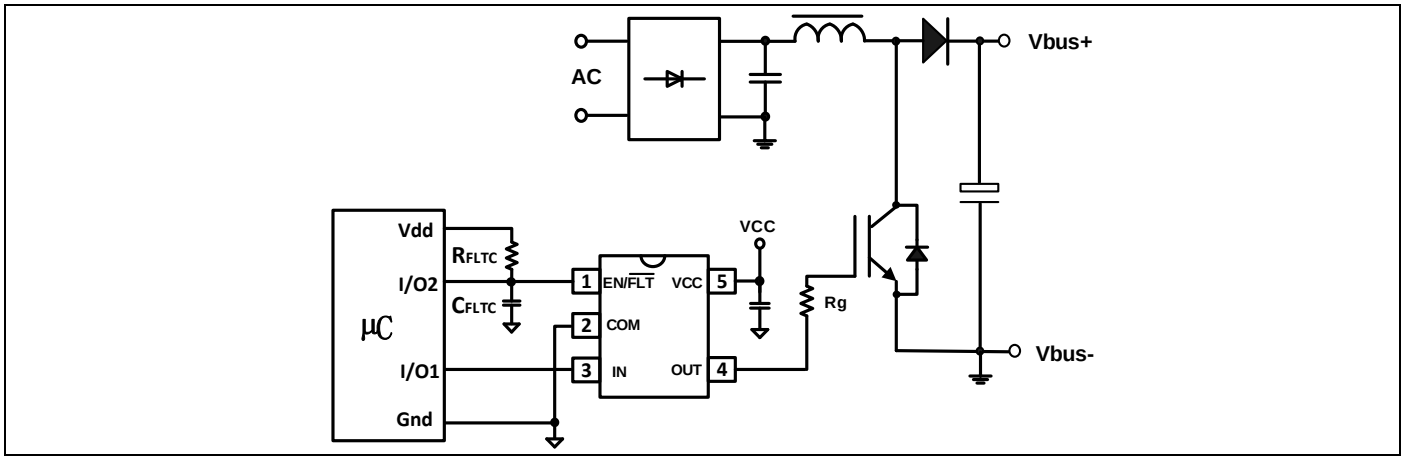


Figure 9 1ED44171N01B in Boost application

5.6 Enable input

1ED44171N01B provides an enable functionality that allows to shutdown or to enable the output. When EN/$\overline{\text{FLT}}$ is pulled up (the enable voltage is higher than V_{ENH}) the output is able to operate normally, pulling EN/$\overline{\text{FLT}}$ low (the enable voltage is lower than V_{ENL}) the output is disable. The relationships between the input, output and enable signals of the 1ED44171N01B are illustrated below in Figure 10~12. From these figures, we can see the definitions of several timing parameters and threshold voltages (i.e. t_{DISA}, V_{ENH} and V_{ENL}) associated with this device.

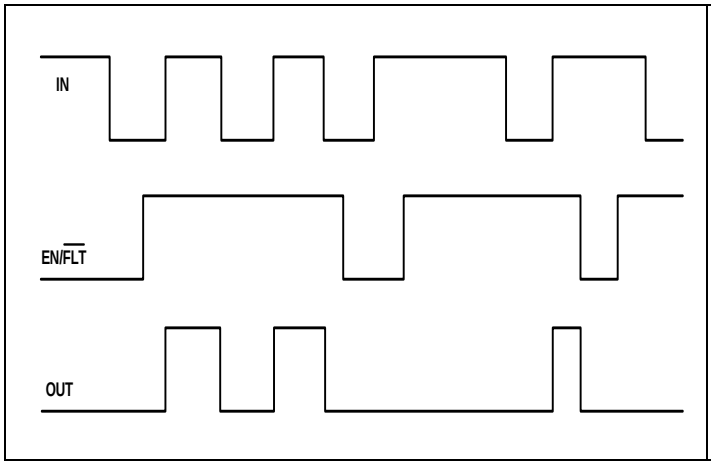


Figure 10 Input/output/enable pins timing diagram

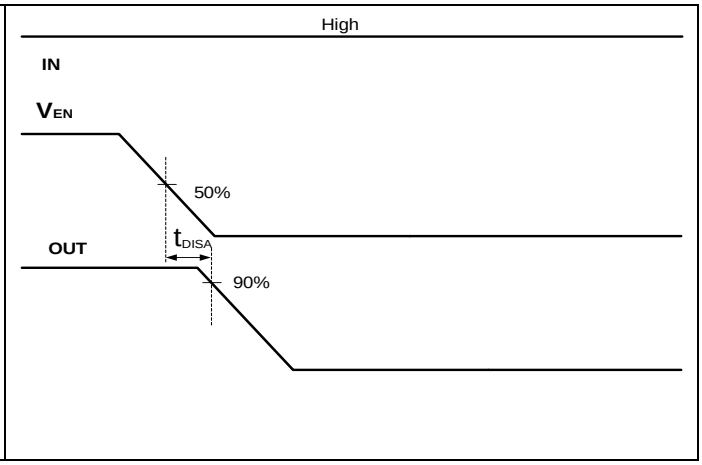


Figure 11 EN pin switching time waveform

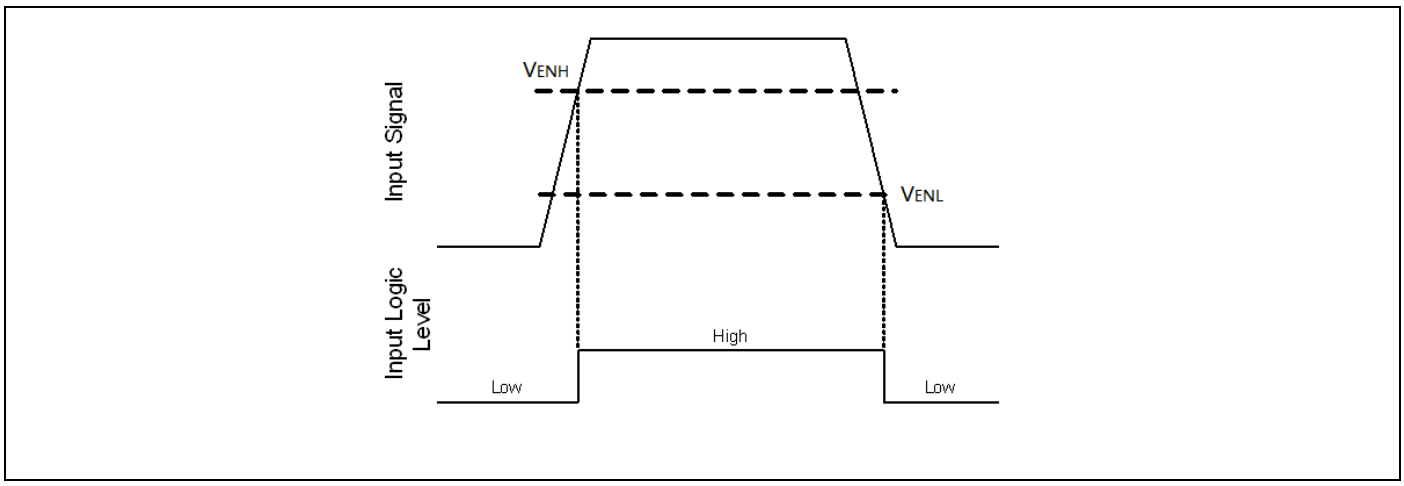
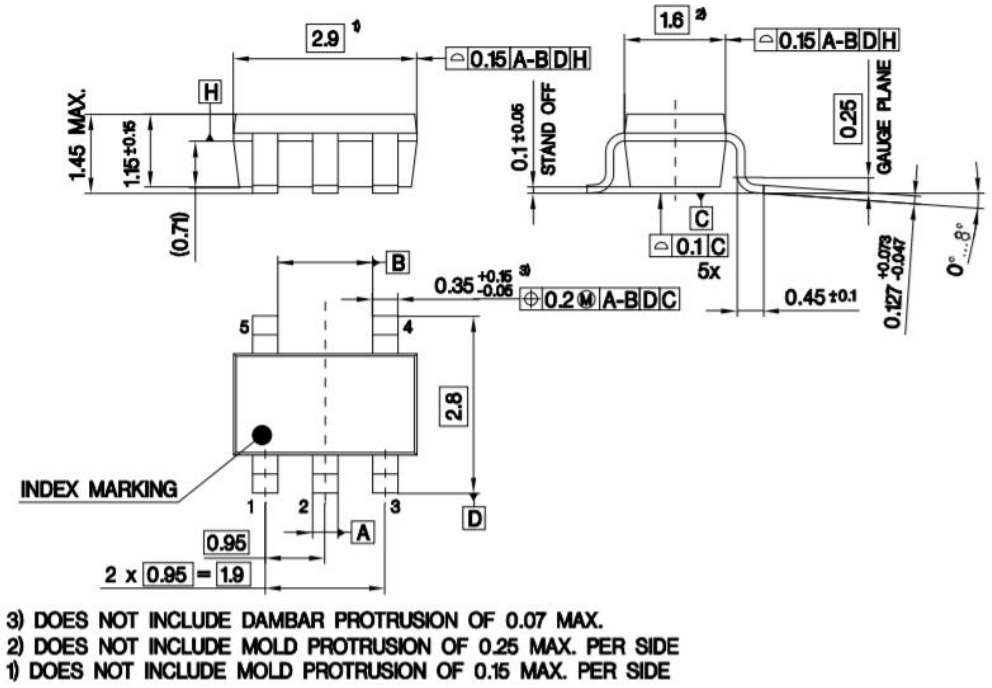
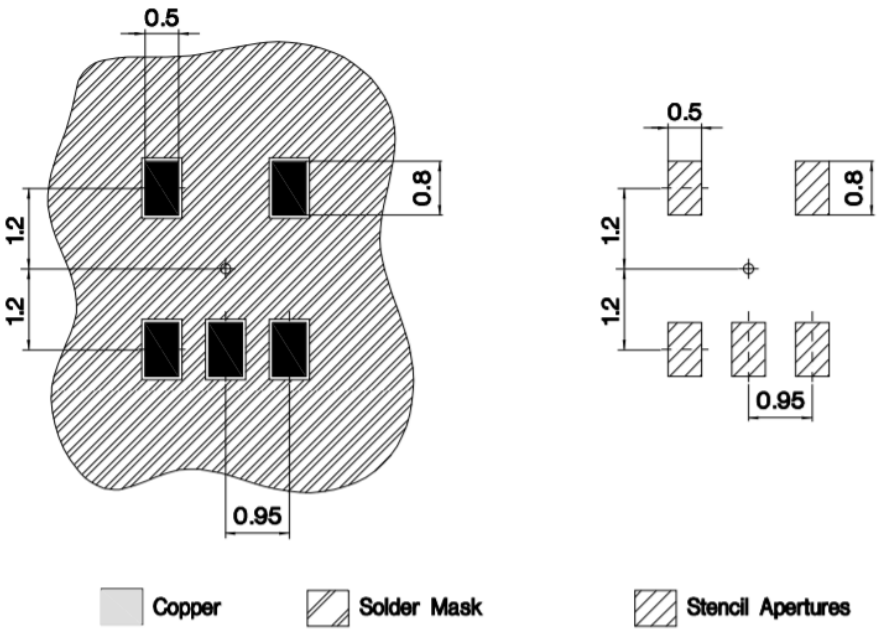


Figure 12 EN input thresholds

6 Package outline: PG-SOT23-5-1



Outline dimensions



Footprint dimensions

Figure 13 Package outline

7 Tape and reel details

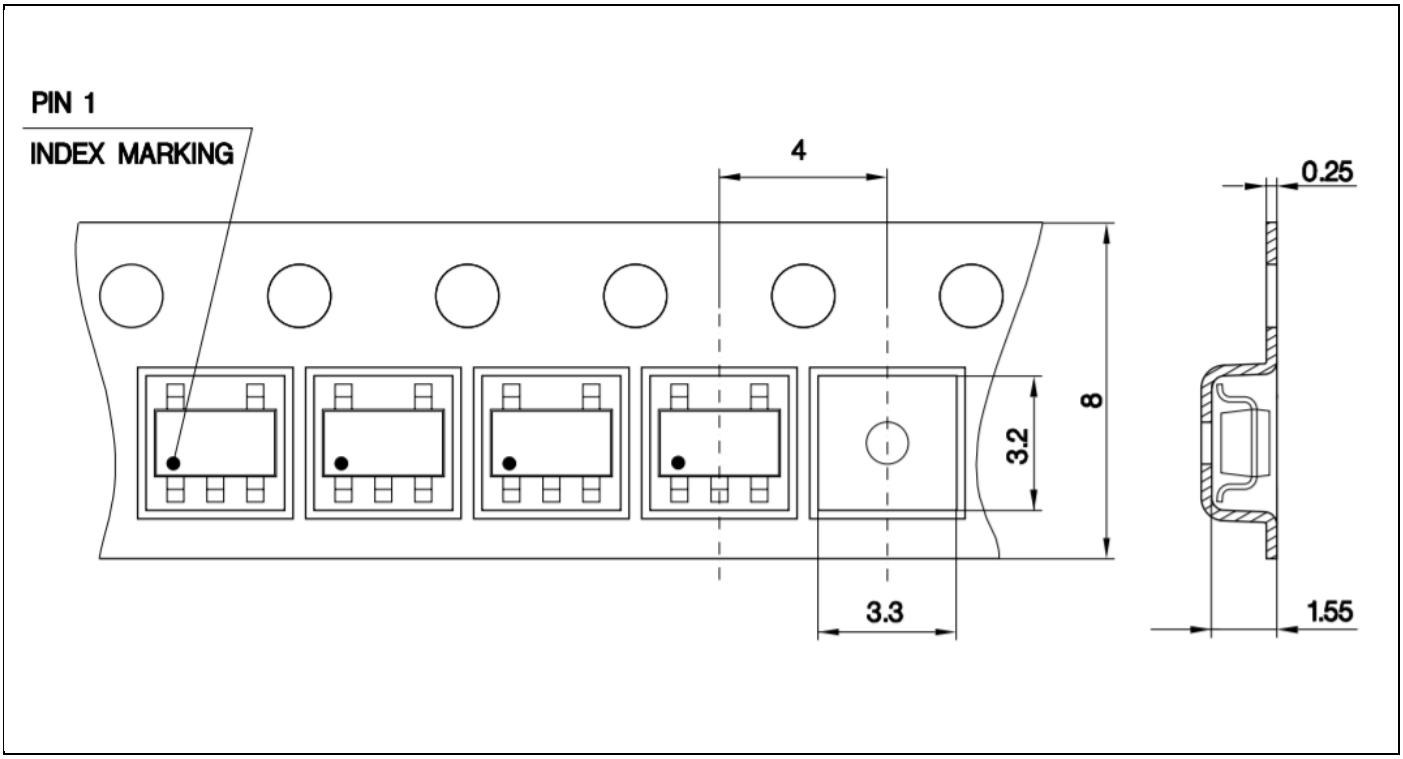
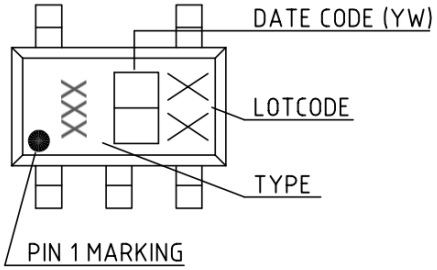


Figure 14 Tape and reel dimensions

Notes: For further details, please visit www.infineon.com/packages

8 Part marking information



TOP MARKING

Figure 15 Part marking information

9 Similar products

Channels	Typ. gate drive (Io+/Io-)	Part number	Max supply voltage	UVLO (on/off)	Typ. prop. delay (on/off)	Logic and features	Package options
	A		V	V	ns		
1	1.5 / 1.5	IRS44273L	25	10.2 / 9.2	50 / 50	Single non-inverting channel Dual OUT pins	SOT23-5L
	2.6/2.6	1ED44173	25	8.0/7.3	34 / 34	Single negative current sense OCP, fault out and ENABLE	SOT23-6-3
	2.6/2.6	1ED44175	25	11.9/11.4	50 / 50	Single negative current sense OCP, fault out and ENABLE	SOT23-6-3
	0.8/1.75	1ED44176	25	11.9/11.4	50 / 50	Single positive current sense OCP, fault out and ENABLE	PG-DSO-8
2	2.3 / 3.3	IRS4426S	25		50 / 50	Dual inverting channels	SOIC-8L
		IRS44262S	20	10.2 / 9.2	50 / 50	Dual inverting channels	SOIC-8L
		IRS4427S	25		50 / 50	Dual non-inverting channels	SOIC-8L
		IRS4428S	25		50 / 50	Single inverting channel Single non-inverting channel	SOIC-8L
	10/10	2ED24427	24	11.5/10	40 / 55	Dual non-inverting channels with ENABLE	Power Pad DSO-8

Revision history

Document version	Date of release	Description of changes
0.1	July 08, 2021	Target datasheet draft
1.0	Jan. 17, 2022	Datasheet
1.1	Feb. 02, 2022	Final Datasheet

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