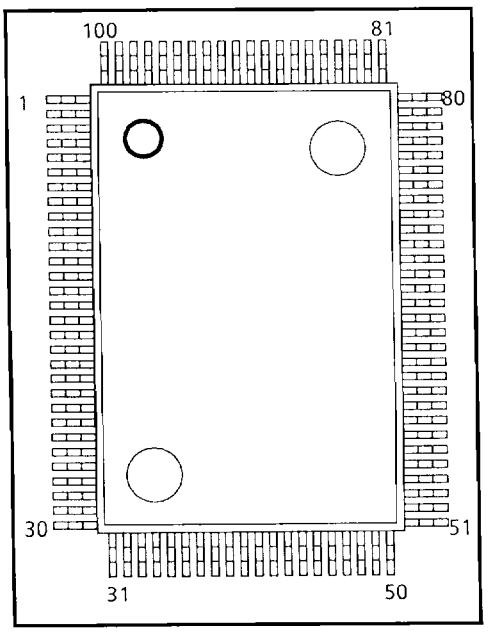
TC85041F

Bus Interface Adapter

1. GENERAL DESCRIPTION

The TC85041F is a bus interface adapter (BIA) for converting the system interface to that of 16 bit PIO type by means of connecting to the host bus side of the hard disk controller T7518 or TC8560F. This IC has the sector buffer (264 byte × 2) and built-in registers for receiving the command and the parameter to the hard disk controller. Various kinds of commands and parameters sent from the host for controlling the disk can be transferred to the hard disk controller of the main body. These structures are systematically equivalent to those of IBM AT, making the compatible disk controller available.

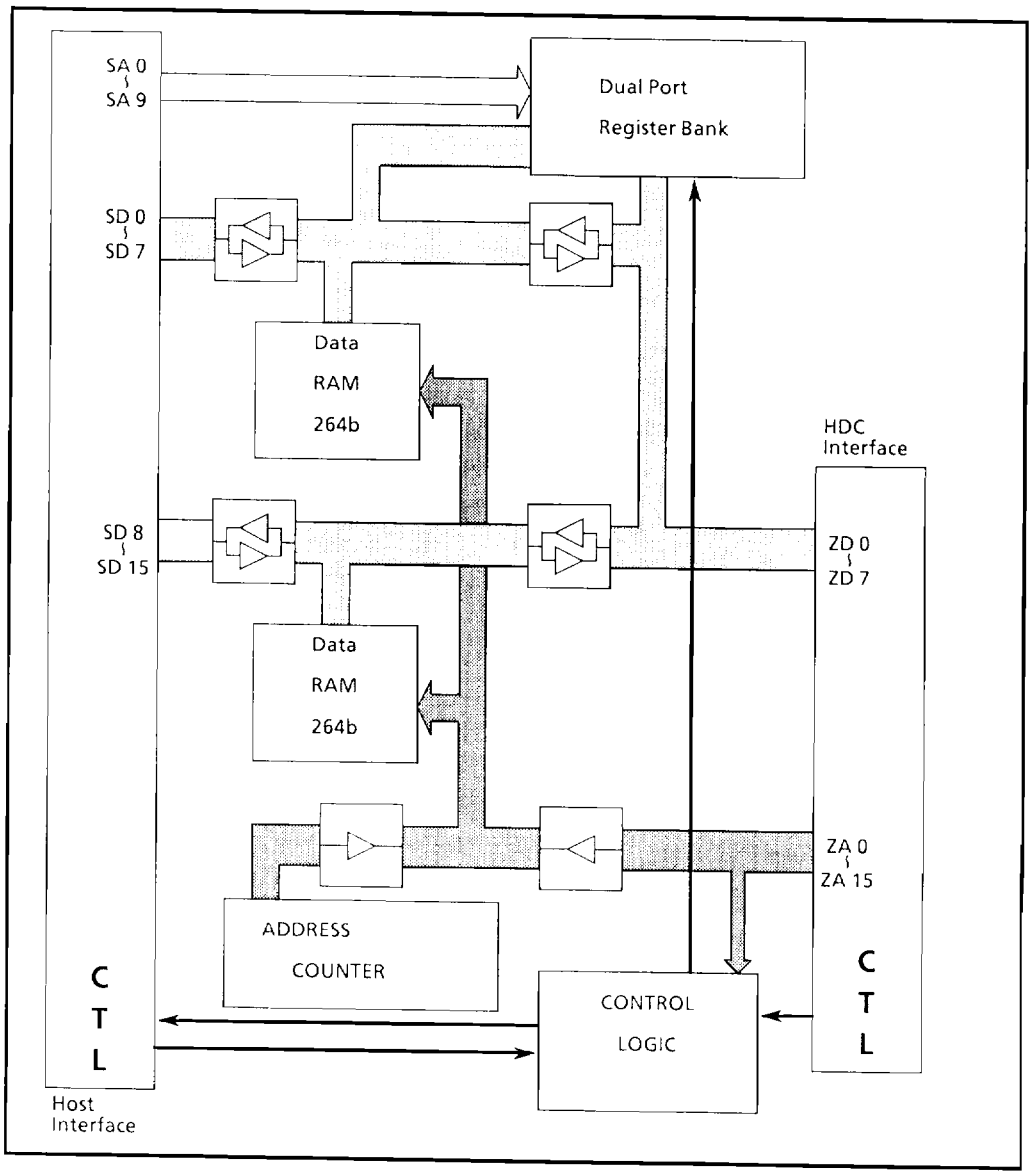


2. FEATURES

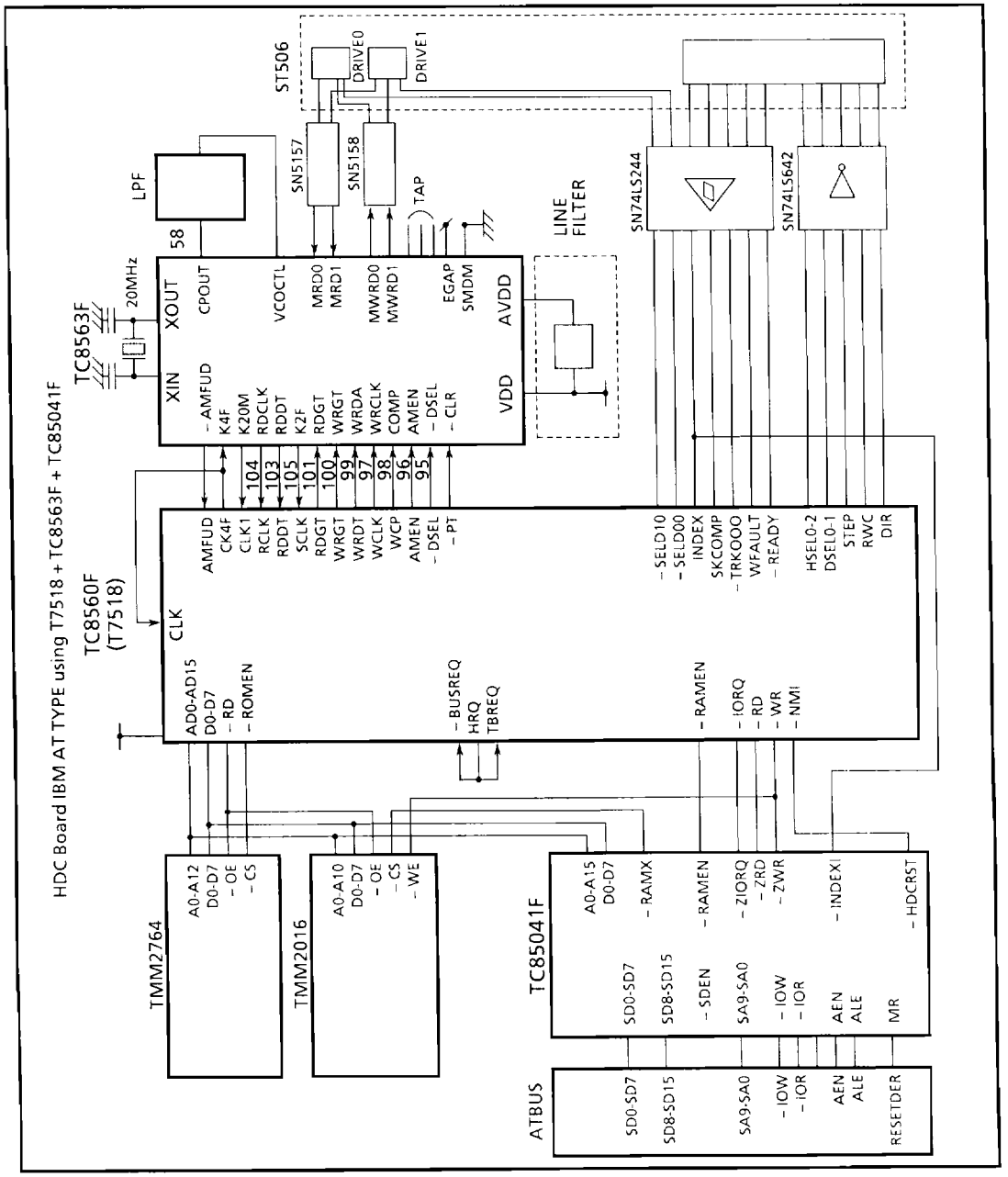
- Si-gate high speed CMOS technology
- +5V single power supply
- 100 pin flat package
- Built-in 264 bytes × 2 sector buffer RAM
- IBM, PC/AT compatible interface
- Direct connection of HDC (T7518 or TC8560F)
- Built-in command receiving register

3. APPLICATION SYSTEM

3.1 BIA BLOCK DIAGRAM



3.2 TYPICAL APPLIED SYSTEM CONFIGURATION



4. PIN DESCRIPTION

4.1 PIN CONFIGURATION

NO.	I/O	PIN NAME	NO.	I/O	PIN NAME	NO.	I/O	PIN NAME
1	I	SA4	36	I	ENID	71	I	ZA2
2	I	SA3	37	OD	– BUSY	72	I	ZA1
3	I	SA2	38	O	– WGT	73	I	ZA0
4	I	SA1	39	O	RGT	74	I	– RAMEN
5	I	SA0	40	G	GND	75	I	– ZIOREQ
6	G	GND	41	V	VDD	76	I	– ZWR
7	IO	SD15	42	I	WGTI	77	I	– ZRD
8	IO	SD14	43	I	– SVGT	78	O	– INT
9	IO	SD13	44	I	RGTI	79	O	– RAMX
10	IO	SD12	45	I	N/L	80	O	– RAMY
11	IO	SD11	46	I	DSEL0I	81	G	GND
12	IO	SD10	47	I	DSEL1I	82	G	GND
13	IO	SD9	48	O	– DSEL0	83	O	– HDCRST
14	IO	SD8	49	O	– DSEL1	84	I	MR
15	G	GND	50	G	GND	85	I	– MR
16	V	VDD	51	V	VDD	86	I	– IOR
17	IO	SD7	52	IO	ZD0	87	I	– IOW
18	IO	SD6	53	IO	ZD1	88	I	TEST
19	IO	SD5	54	IO	ZD2	89	I	– PRIM
20	IO	SD4	55	IO	ZD3	90	V	VDD
21	IO	SD3	56	IO	ZD4	91	G	GND
22	IO	SD2	57	IO	ZD5	92	I	ALE
23	IO	SD1	58	IO	ZD6	93	OD	– IOCS16
24	IO	SD0	59	IO	ZD7	94	OD	– IOCS16D
25	G	GND	60	I	ZA14	95	I	AEN
26	O	– SDEN	61	I	ZA13	96	I	SA9
27	O	– SD7EN	62	I	ZA9	97	I	SA8
28	V	VDD	63	I	ZA8	98	I	SA7
29	O	IRQ14	64	I	ZA7	99	I	SA6
30	03	IRQ14P	65	V	VDD	100	I	SA5
31	O	HDMAEN	66	G	GND			
32	O	– INDEX	67	I	ZA6			
33	I	– INDEXI	68	I	ZA5			
34	I	– FDCEN	69	I	ZA4			
35	I	– DACK2	70	I	ZA3			

4.2 PIN FUNCTIONS

note) I : input, O : output, 03 : three-state, OD : open drain

NO.	PIN NAME	I/O	FUNCTION
1	SA4	I	Address input. Asserted at "High".
2	SA3	I	Address input. Asserted at "Low".
3	SA2	I	Host address. Low order 3 bit input.
4	SA1	I	
5	SA0	G	
6	GND	IO	GND terminal.
7	SD15	IO	Host data bus high order bits.
8	SD14	IO	
9	SD13	IO	
10	SD12	IO	
11	SD11	IO	
12	SD10	IO	
13	SD9	IO	
14	SD8	IO	
15	GND	G	GND terminal.
16	VDD	V	+ 5V power supply terminal.
17	SD7	IO	Host data bus low order bits.
18	SD6	IO	
19	SD5	IO	
20	SD4	IO	
21	SD3	IO	
22	SD2	IO	
23	SD1	IO	
24	SD0	IO	
25	GND	G	GND terminal.
26	– SDEN	O	Enable output at external buffer application.
27	– SD7EN	O	Enable output for external buffer of "SD7". This is used at the application with FDC is out of bus buffer.
28	VDD	V	+ 5V power supply terminal.
29	IRQ14	O	Interrupt output to host. Valid only when BUSY = 0. Reset by the reading out of status register from host. "High" active totempole CMOS output.
30	IRQ14P	03	Three-state output of [IRQ14], enabled by "High" on the [HDMAEN].
31	HDMAEN	O	Interruption enable output to HDD.
32	– INDEX	O	Index signal output to HDC.
33	– INDEXI	I	Index signal input from drive.
34	– FDCEN	I	Input "Low" when TC85041F is used at the common bus buffer application with FDC.
35	– DACK2	I	Input DMA acknowledge signal for FDC.

NO.	PIN NAME	I/O	FUNCTION
36	ENID	I	Input ENID signal from FDC.
37	– BUSY	OD	Signal for indicating that HDC is under command execution. "Low" active open drain output.
38	– WGT	O	Write control signal. Inhibited during SVGT is "Low".
39	RGT	O	Signal for indicating the start of reading operation to VFO circuit. Inhibited during SVGT.
40	GND	G	GND terminal.
41	VDD	V	+ 5V power supply terminal.
42	WGTI	I	Write control signal from HDC.
43	– SVGT	I	Servo gate signal from drive.
44	RGTI	I	Read gate signal from HDC.
45	N/L	I	At "Low", control of [DSEL0] and [DSEL1] possible. Pulled up internally.
46	DSEL0I	I	Drive selection signal input.
47	DSEL1I	I	
48	– DSEL0	O	Drive selection signal output. Power-save control is possible.
49	– DSEL1	O	
50	GND	G	GND terminal.
51	VDD	V	+ 5V power supply terminal.
52	ZD0	IO	Connected to CPU Z80 data bus of HDC.
53	ZD1	IO	
54	ZD2	IO	
55	ZD3	IO	
56	ZD4	IO	
57	ZD5	IO	
58	ZD6	IO	
59	ZD7	IO	
60	ZA14	I	Connected to CPU Z80 address bus of HDC.
61	ZA13	I	
62	ZA9	I	
63	ZA8	I	
64	ZA7	I	
65	VDD	V	+ 5V power supply terminal.
66	GND	G	GND terminal.

NO.	PIN NAME	I/O	FUNCTION
67	ZA6	I	Connected to CPU Z80 address bus of HDC.
68	ZA5	I	
69	ZA4	I	
70	ZA3	I	
71	ZA2	I	
72	ZA1	I	
73	ZA0	I	
74	– RAMEN	I	RAM enable signal input from HDC.
75	– ZIOREQ	I	– IOREQ from Z80 in HDC is input. Pulled up internally.
76	– ZWR	I	– WR from Z80 in HDC is input. Pulled up internally.
77	– ZRD	O	– RD from Z80 in HDC is input. Pulled up internally.
78	INT	O	Interrupt request signal to HDC.
79	– RAMX	O	Chip select alternate signal to external SRAM. Allocation to A000H to BFFFH is executed.
80	– RAMY	O	Chip select alternate signal to external SRAM.
81 82	GND	G	Allocation to C000H to FFFFH is executed. GND terminal.
83	– HDCRST	O	Reset interrupt signal to HDC. Soft reset (SR bit) is output
84	MR	I	Master reset signal.
85	– HR	I	"Low" active hard reset signal.
86	– IOR	I	I/O read signal from host.
87	– IOW	I	I/O write signal from host.
88	TEST	I	Terminal for test. Pulled down internally.

NO.	PIN NAME	I/O	FUNCTION
89	– PRIM	I	Primaryn or secondary of address selects to HDD circuit is selected. Pulled down internally.
90	VDD	V	+ 5V power supply terminal.
91	GND	G	GND terminal.
92	ALE	I	Address latch input for setting reflective response to [IOCS16] terminal.
93	– IOCS16	OD	This terminal is "Low" active open drain output. I/O CS response signal. Becomes "Low" when ALE is "High" at the time of valid address inputting from host, and becomes to "High" for an instant with – IOR or – IOW fall, and returns to "Hi-z" soon.
94	– IOCS16D	OD	Low" active open drain output of [IOCS16] signal".
95	AEN	I	Receives AEN signal from system. At "Low", BIA becomes selectable.
96	SA9	I	Address input. Used for decoding.
97	SA8	I	Address input. Asserted at "High".
98	SA7	I	Address input. Used for decoding.
99	SA6	I	Address input. Asserted at "High".
100	SA5	I	

Low level Primary	High level Secondary	Register Name
hex 1F0	hex 170	Data Port
hex 1F1	hex 171	WPC/ERR
hex 1F2	hex 172	SCT
hex 1F3	hex 173	SN
hex 1F4	hex 174	CLL
hex 1F5	hex 175	CLH
hex 1F6	hex 176	SDH
hex 1F7	hex 177	CMD/ST
hex 3F6	hex 376	HDR
hex 3F7	hex 377	DIR

5. FUNCTIONAL SPECIFICATION

5.1 HOST INTERFACE

The host interface of the TC85041F makes the PIO port allocated on the 16 bit data bus available. Through the connection of the PC bus with the host interface terminals, eight I/O ports successively allocated on the I/O address of the host system are fabricated. By the input pin assignment, the primary or the secondary address can be selected.

I/O ADDRESS		READ	WRITE	BYTE/ WORD
PRIMARY	SECONDARY			
1F0H	170H	Data Port	←	word
1F1H	171H	Error Register	Write Pre-comp	byte
1F2H	172H	Sector Count	←	byte
1F3H	173H	Sector Number	←	byte
1F4H	174H	Cylinder Low order bit	←	byte
1F5H	175H	Cylinder High order bit	←	byte
1F6H	176H	Drive/Head	←	byte
1F7H	177H	Status Register	Command Register	byte
3F6H	376H	Alternate Status Register	Hard Disk Register	byte
3F7H	377H	Digital Input Register		byte

These register main bodies are prepared in the TC85041F as a scratch-pad register. Since the access from the HDC interface port of the TC85041F is also made possible, the function as the system is realized by the program control from the CPU of the HDC side.

(1) Data port

The data of the built-in sector buffer RAM can be read or written with 16 bit width by the system data port. The RAM address is controlled by the built-in counter. This counter is incremented by the trailing edge of the read or write strobe pulse effective.

The initialize of the counter is set by the port of the HDC side. The access to the port is inhibited in the period excepting the time during which the read or write command is executed by the HDC.

The access to this port is performed when the bit 3(data request) of the status register is "1" during the read or write command is executed.

(2) Error register

The error register is a read-only register. Its contents is the byte which is set from the HDC side. The information for the command which is executed just before is set.

In this data, only the data bit, which is set at the time other than that of the DIAGNOSTIC mode, is effective. The DIAGNOSTIC mode is applicable at the time just after the power-on and the

DIAGNOSTIC command is issued. The error register indication in the case of DIAGNOSTIC mode is different from that in the case of DIAGNOSTIC mode is different from that in the case of usual mode.

DIAGNOSTIC mode (Diag MODE)

01 No error
02 Controller error
03 Sector buffer error
04 ECC circuit error
05 Control processor error

Normal operation response

Bit 0 : Data address mark (DAM) not found. When the address mark of the disk can not be detected, "1" is set.

Bit 1 : Track zero error.
This bit is set when no track zero signal is received even after the outer seek of 1023 times or more. In this case, abnormality of the drive is suspected.

Bit 2 : Abnormal termination of command.
This bit indicates that the command is abnormally terminated due to the abnormality of the drive, so on. These errors are the write fault, the seek abnormality, the drive not-ready and the invalid command. In these cases, the status register and the error register should be checked for investigating the cause.

Bit 3 : Not used.

Bit 4 : ID not found.
This is the case where the objective ID (head, sector Number) can not be found on the designated cylinder. This bit is set after the retry of 16 revolutions when the retry is assigned by the command byte, or after the retry of two revolutions when the retry is not assigned.

Bit 5 : Not used.

Bit 6 : Data ECC error.
This bit indicates that a uncorrectable ECC error occurred during reading the target data.

Bit 7 : Bad sector detect.
This bit indicates that a bad-sector mark is detected during the target data search. No read or write of the data can be performed to this sector.

Write pre-compensation

The numerical value, obtained through dividing with 4 the cylinder number to be used for performing the write pre-compensation, is input. The program of the HDC side is prepared so that the reduction of write current or the process of write pre-compensation would be performed during the write process equal or inner than this cylinder.

[ ] Sector count register

The number of sectors to be used by the verify, read/write and format commands are set in this register.

The number of sectors of this register is decremented by the HDC at every sector processing. This setting is required to be made prior to the command execution.

Setting "0" at this register means the multi-sector processing of 256 sectors.

[ ] Sector number register

The number of the objective sector to be processed is input.

[ ] Low order and high order of cylinder number

Input the cylinder number of the objective data to be processed. The maximum value of the cylinder number is 1023.

DATA BIT	CYLINDER HIGH ORDER								CYLINDER LOW ORDER							
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
CYLINDER NO.							X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

[ ] Drive/Head register

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	0	1	DS	H3	H2	H1	H0

Bit 7 : "1" is set : 4byte ECC is selected.
Bit 6 : "0" is set ┐
Bit 5 : "1" is set ┘ 512byte sector is selected.
Bit 4 : Drive number is selected. By "0", drive #1 and by "1", drive #2 is selected.
Bit 3-0 : Head select data

[ ] Status register

The status register is a read-only register for the result status which is set by the HDC after the command execution.

This status register is necessary to be investigated by the host system according to the command termination interrupt [IREQ14].

The IREQ14 is reset by the status register read. When the busy bit (Bit 7) is "1", other bits and the contents at other registers have no meaning. The busy bit has the facility which set to "1" by the command writing the DREQ bit is also reset at this time. The other bits of status register should be prepared later.

Bit 7 : Busy [BUSY]

This bit indicates that the HDC is in the BUSY state. In this state, other bits of the status register and the contents of other registers are invalid. Therefore, the Bit 7 of the status register is required to be checked before all the register readings. The BUSY state is turned on at the time indicated below.

(1) Reset state (Absolved by the CCLR (Counter Clear) from HDC)
(2) When the command is written from the host. (Reset by the command reading from the HDC.)
(3) When the multi-sector transfer is completed. (CFULL state).
(4) When "1" is written to the Bit 7 [BUSY] of the status register by the HDC.

Bit 6 : Drive ready [READY]

When both this bit and the seek complete bit (Bit 4) are "1", the HDD is ready to use. In other conditions, the access to HDD is inhibited. The contents of the bit 6 of the status register written by theHDC appears.

Bit 5 : Write fault [WFAULT]

This bit indicates the occurrence of the illegal write to the disk. The contents of the bit 5 of the status register written by the HDC appears.

Bit 4 : Seek complete [SKCOMP]

This bit indicates that the seek operation of the read/write head is finished. The signal of the SKCOMP input appears.

Bit 3 : Data request [DREQ]

This bit indicates that the sector buffer requires the service of the host. This bit shows what is written to the Bit 3 of the status register by the HDC.

When the 256 word transfer is completed at the host transfer unaccompanied by the ECC, this bit is reset automatically. When the 256 word + 4 byte or + 7 byte transfer is completed at the host transfer accompanied by the ECC, this bit is reset automatically

Bit 2 : Corrected data [CORR]

This bit indicates that the ECC error is properly corrected by the ECC correcting operation. This kind of error will not terminate the multi-sector operation. The contents of the Bit 2 of the status register is written by the HDC appears.

Bit 1 : Index [INDEX]

The index pulse of the selected HDD can be read. The inverted signal of the – INDEXI input appears.

Bit 0 : Error [ERROR]

This bit indicates that the command just executed has made an error because of the certain cause. When the next command is written, this bit is reset. The contents of Bit 0 of the status register is written by the HDC appears. The status of drive side selected by DS bit in Drive/Head register appears on the three bits of READY, WFAULT and SKCOMP. When DS bit is "0", the contents of status register #1 written by HDC appears on these bits. When DS bit is "1", the contents of status register #2 appears.

[ ] Alternate status register

The contents of this register is the same as the status register for the task file. The difference of this register from the status register is the function in which even when the host begins to read this register, the interrupt acknowledge is not allowed to function and the interrupt status is not reset. The definition of the bit is the same as the status register.

[ ] Command register

The command register can receive eight kinds of commands with the control program of the HDC side. The command is activated by means of writing the command to the command register after preparing the value to each register during the not-busy state.
The Bit 7 of the status bit (BUSY) is set by the command register write, and at the same time, the interrupt signal is generated against the HDC ([−INT] terminal). The standard HDC control program makes the following commands valid.

COMMAND	D7	D6	D5	D4	D3	D2	D1	D0
Recal	0	0	0	1	S3	S2	S1	S0
Seek	0	1	1	1	S3	S2	S1	S0
Read	0	0	1	0	0	0	0	RTY
Write	0	0	1	1	0	0	0	RTY
Read Long	0	0	1	0	0	0	1	RTY
Write Long	0	0	1	1	0	0	1	RTY
Verify	0	1	0	0	0	0	0	RTY
Format	0	1	0	1	0	0	0	0
Diag	1	0	0	1	0	0	0	0
Specify	1	0	0	1	0	0	0	1

note) The polynomials of CRC and ECC to be used for the case, in which the TC8560F is used as the HDC, are shown below.

ID CRC $= (X^{16} + X^{15} + X^2 + 1)$

DATA ECC $= (X^{21} + 1)(X^{11} + X^2 + 1)$

- Hard disk register

  This is a write-only register.

Bit 0	: Reserved	
Bit 1	: HINTDIS	This bit resets the IRQ14 output into the Hi-Z status through setting this bit to "1". The reversed signal of this bit is output to the HDMAEN terminal.
Bit 2	: SR	This is a bit for resetting the HDC. When this bit is set at "1", "Low" is output to the −HDCRST terminal.
Bit 3	: HS3	"1" is set when the drive has eight or more heads The contents appear to the Bit 0 of the control input register (F8 Read) of the HDC side.
Bit 4-7	: Reserved	

- Digital input register

  This is a read-only register to know the present drive status.

Bit 0 : −DSEL0	Drive No. (Chosen by Drive/Head register)	"0" appears when DS bit is "0"
Bit 1 : −DSEL1		"0" appears when DS bit is "1"
Bit 2 : −HSEL0	Head Select	The inverted contents of Bit0-3 of the Drive/Head register appears.
Bit 3 : −HSEL1		
Bit 4 : −HSEL2		
Bit 5 : −HSEL3		
Bit 6 : −WGT		The input of WGT appears.
Bit 7 : Diskette Changed		Hi-Z state is maintained on the data bus SD7. This is a bit for outputting the Dskette Change bit of the FDC to the host.

5.2 HDC INTERFACE

The HDC interface of the TC85041F provides the register and the buffer memory, which are allocated to the I/O and the memory, for Z80 which is the built-in CPU of HDC.

REGISTER NAME	ADDRESS
Buffer RAM	8000H to 820FH (- RAMEN = 0) (- ZIOREQ = 1)
Scratch-pad register	F1H to FFH For address allocation, refer to following paragraph.
Control I/O register	F8H
Head select	F0H Write only
Drive register	28H

[ ] Scratch-pad register address

REGISTER NAME	HOST ACCESS	HDC ACCESS ADDRESS	
Error register	Read only	Write only	F9H
Write pre-comp.	Write only	Read only	F1H
Sector count	R/W	R/W (*1)	F2H/FAH
Sector Number	R/W	R/W (*1)	F3H/FBH
Cylinder low order	R/W	R/W (*1)	F4H/FCH
Cylinder high order	R/W	R/W (*1)	F5H/FDH
Drive/Head	R/W	R/W (*1)	F6H/FEH
Status register #1	Read only	Write only (*3)	FFH
Status register #2	Read only	Write only (*3)	EFH
Command register	Write only	Read only (*2)	F7H

(*1) Since this is of the dual-port structure, the access should be carried out with the Bit 7 of the status register set at "1".

(*2) Write to the command port from the host asserts the INT.

(*3) BUSY (Bit 7), DREQ (Bit 3), CORR (Bit 2) and ERROR (Bit 0) are common between the status register #1 and status register #2. INDEX (Bit 1) is reserved. The three bits of READY, WFAULT and SKCOMP are separated to drive #1 and drive #2.

(1) Buffer RAM

The buffer RAM is fabricated as the RAM of bank-switching type accessible from both the host bus and the HDC CPU. The contents are read out to the host bus as a word from the 0 address by the PIO operation of the built-in address counter.

For the HDC CPU, the byte addresses beginning from 8000H correspond to the HOST addresses. The correspondency of the address is as shown below.

HOST ADDRESS		HDC ADDRESS
DECIMAL	HEXADECIMAL	HEXADECIMAL
0	000H Low order 8bit	8000H
0	000H High order 8bit	8001H
1	001H Low order 8bit	8002H
1	001H High order 8bit	8003H
	.	
265	100H Low order 8bit	8200H
265	100H High order 8bit	8201H
	.	
261	105H Low order 8bit	820AH
261	105H High order 8bit	820BH
262	106H Low order 8bit	820CH
262	106H High order 8bit	820DH
263	107H Low order 8bit	820EH
263	107H High order 8bit	820FH

(2) Control output register (Write F8H)

The control output register is available for controlling the operation of the TC85041F.

Bit 0 : HINTS When this bit is set at "1", "High" is output to the IRQ14 at BUSY = 0.

Bit 1 : SEL The buffer RAM is set at the host side.

Bit 2 : CCLR The address counter for the RAM access from the host is turned into clear state (Reset).

Bit 3 : HINTR The IRQ14 is reset.

Bit 4 : LONG — The bit is set at "1" at transferring the data with the ECC bytes. When this bit is "0", DREQ bit is reset at C-FUL (Counter Full).

Bit 5 : MULTI — This bit is set at "1" at executing the multi-sector Read/Write command. When this bit is set at "1" and LONG is "0", BUSY bit is reset at C-FUL (Counter Full) state.

Bit 6 : ECC7S — Selected ECC is 7 byte at "1" and ECC is 4 byte at "0".

Bit 7 : Reserved

MULT1	LONG	ECC7S	CONTROL OF DREQ and BUSY
0	0	×	DREQ is reset at C-FUL. BUSY is not set.
0	1	0	DREQ is reset at LC-FUL. BUSY is not set.
0	1	1	DREQ is reset at L7C-FUL. BUSY is not set.
1	0	×	DREQ is reset at C-FUL. BUSY is set.
1	1	0	DREQ is reset at LC-FUL. BUSY is set.
1	1	1	DREQ is reset at L7C-FUL. BUSY is set.

- Control input register (Read F8H)

This is a control input register for investigating the status of TC85041F.

Bit 0 : HS3/RWC — This bit indicates that the heads of eight or more are provided. When this bit is set at "1", the HS3 (Bit 3) of the drive/head register (Bit 3) becomes valid.

Bit 1 : C-FUL — This bit becomes "1" when the address counter counts up to the 512th byte.

Bit 2 : LC-FUL — This bit becomes "1" when the address counter counts up to the (512+4)th byte.

Bit 3 : COM — This bit is set at "1" when the command is written from the host and when the HDC reads the command this bit is reset at "0".

Bit 4 : L7C-FUL — This bit becomes "1" when the address counter counts up to the (512+7)th byte.

Bit 5-7 : These bits are always "0".

- Drive register write (Write 28H)

Bit 7 : SIDX — This bit is the SIDX (sector index) bit for controlling the −INDEX is output.
When SIDX = 0, the contents of −INDEXI is output to the −INDEX.
When SIDX = 1, the contents of −SVGT is output to the −INDEX.
This bit should be used for special HDD.

Bit 6 : RXSR — This bit is to write to the received bit of the software reset signal from Host.

Bit 5-0 : Reserved

[ ] Drive register read (Read 28H)

Bit 7 : SYDX — This bit is SYIDX bit for checking the change of the −INDEXI input. This bit is inverted at every trailing edge of the −INDEXI input. When the pulse width of the −INDEXI input is small or when the SIDX bit is "1" and the contents of −INDEXI is not transferred to the HDC, the status of the −INDEX can be observed by this SYIDX bit.

Bit 6 : RXSR — This is the received bit of the software reset signal from Host.

Bit 5-0 : These bits are always "0".

5.3 DRIVE INTERFACE

The TC85041F has the interface signal terminals to the hard disk drive.

(1) The contents of the −INDEXI input is developed to the −INDEX output.
However, when the SIDX bit of the drive register (W28) on the HDC side is "1", the contents of −SVGT input is output.

(2) −WGT, RGT
When the −SVGT input is "High", the inversion signal of the WGTI is output to the −WGT, and the RGTI contents to the RGT.
However, when the −SVGT input is "Low", the −WGT becomes "High" and the RGT, "Low".

(3) −DSEL0, −DSEL1
When the N/L input is "High" or OPEN, the inversion signal of the DSEL1I is respectively output to the DSEL0 and the DSEL1.
This generally becomes "High" when the N/L input is "Low". Only at the time of reading of the status register or the digital input register from the host, and the time of the BUSY state, the inversion signal of DSEL0I or DSEL1I is output. Through this process, power saving of drive is made possible.

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply Voltage	−0.5 ~ +7.0	V
V_{IN}	Input Voltage	−0.5 ~VCC +0.5	V
Topr	Operation Temperature	−40 ~ +85	°C
Tstg	Storage Temperature	−65 ~ +125	°C

6.2 DC CHARACTERISTICS

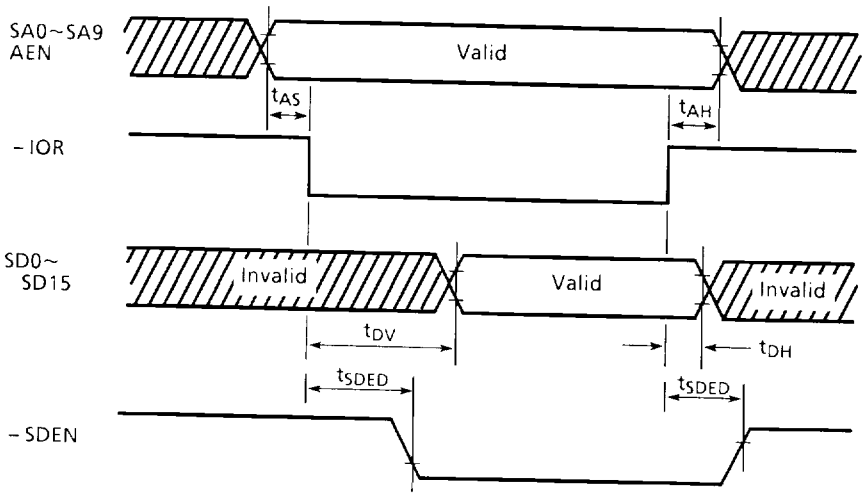
Ta = −40 ~ +85°C, VCC = 5V + 10%

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_{IH1}	High Level Input Voltage	*1	2.2	VCC + 0.5	V
V_{IL1}	Low Level Input Voltage	*1	−0.5	0.6	V
V_{IH2}	High Level Input Voltage	−IOR, −IOW, AEN, SA0~9	3.7	VCC + 0.5	V
V_{IL2}	Low Level Input Voltage	−IOR, −IOW, AEN, SA0~9	−0.5	1.2	V
V_{OH}	High Level Output Voltage	IOH = −3mA	VCC − 0.4	−	V
V_{OL}	Low Level Output Voltage	IOL = 6mA	−	0.4	V
I_{IH}	High Level Input Current	Except TEST, PRIME terminal	−10	10	μA
I_{IL}	Low Level Output Current	Except N/L, -ZRD, -ZWR, -ZIOREQ terminal	−10	10	μA

*1 : Except −IOR, −IOW, AEN, SA0~9 terminal.

.3 AC CHARACTERISTICS

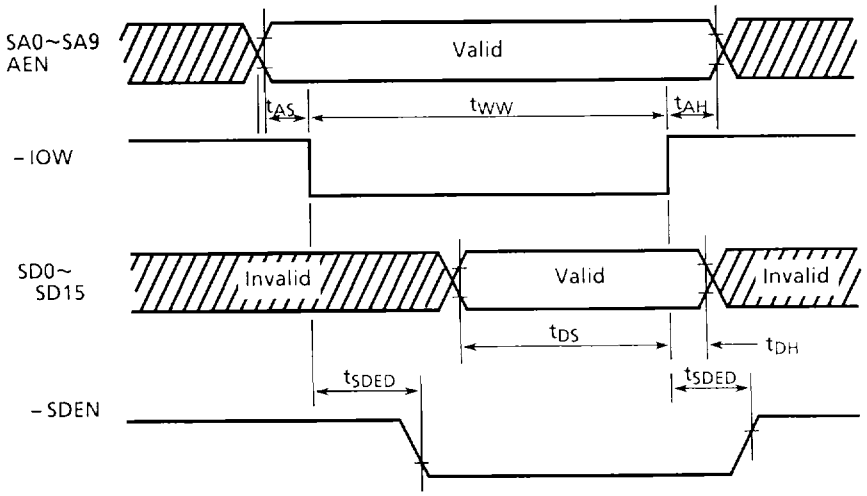
Host I/O Read Timing



Ta = −40 ~ +85°C, VCC = 5V + 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{AS}	Address Setup Time	20		ns
t_{AH}	Address Hold Time	20		ns
t_{DV}	Data Delay Time		80	ns
t_{DH}	Data Hold Time	10		ns
t_{SDED}	− SDEN Delay Time		60	ns

Host I/O Write Timing

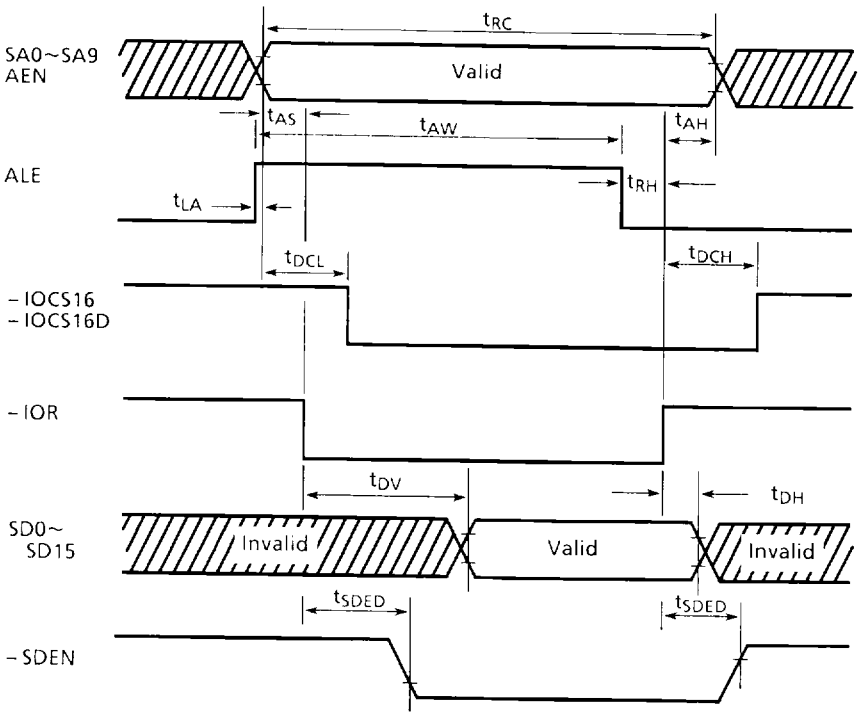


Ta = −40 ~ +85°C, VCC = 5V + 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{AS}	Address Setup Time	20		ns
t_{AH}	Address Hold Time	20		ns
t_{WW}	Write Pulse Width	100		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	40		ns
t_{SDED}			60	ns

5

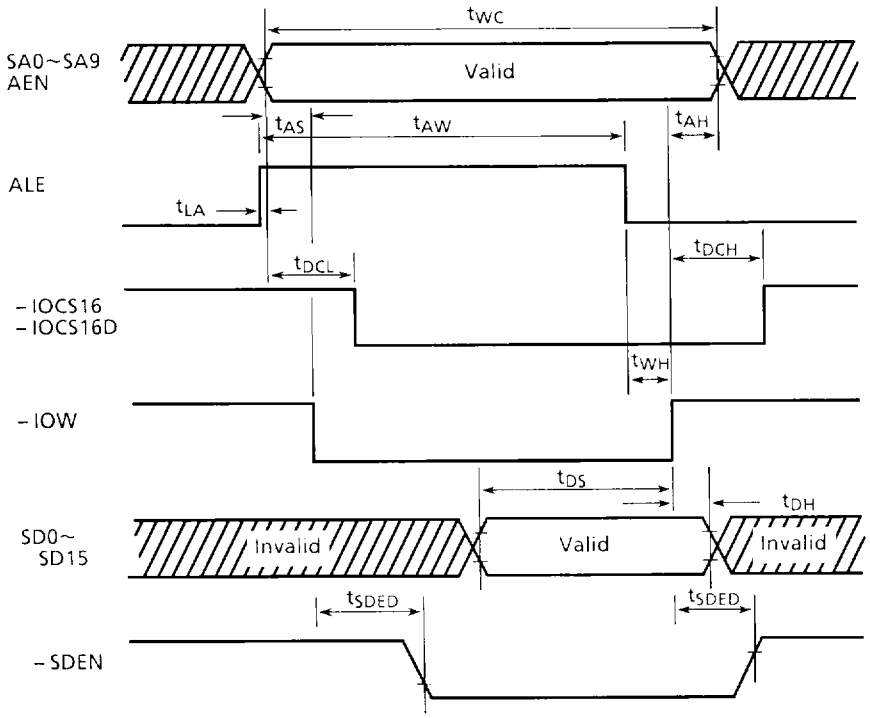
Host Sector Data Read Timing



Ta = −40 ~ +85°C, VCC = 5V + 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	120		ns
t_{AS}	Address Setup Time	20		ns
t_{AH}	Address Hold Time	20		ns
t_{AW}	ALE Pulse Width	30		ns
t_{LA}	ALE prior to address valid	0		ns
t_{RH}	Hold time after −IOR	30		ns
t_{DCL}	−IOCS16 "Low" Delay Time		60	ns
t_{DCH}	−IOCS16 "High" Delay Time		60	ns
t_{DV}	Data Delay Time		80	ns
t_{DH}	Data Hold Time	10		ns
t_{SDED}	−SDEN Delay Time		60	ns

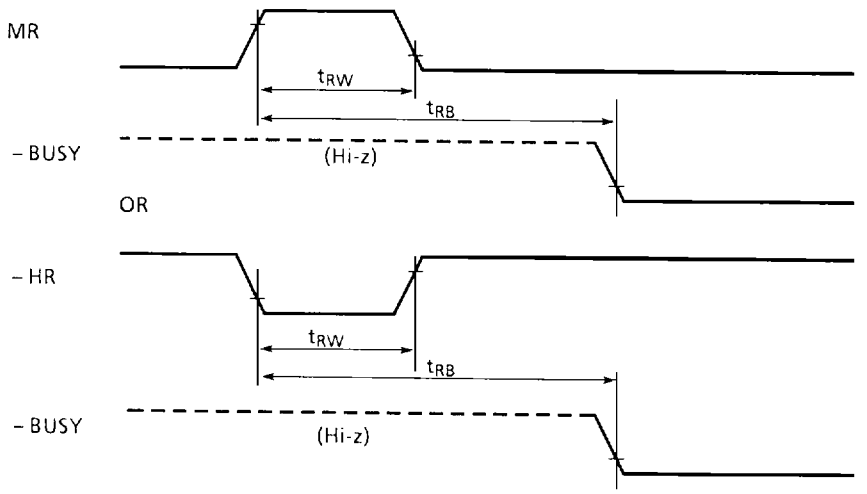
Host Sector Data Write Timing



Ta = −40 ~ +85°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	140		ns
t_{AS}	Address Setup Time	20		ns
t_{AH}	Address Hold Time	20		ns
t_{AW}	ALE Pulse Width	30		ns
t_{LA}	ALE prior to address valid	0		ns
t_{WH}	Hold time after -IOW	30		ns
t_{DCL}	-IOCS16 "Low" Delay Time		60	ns
t_{DCH}	-IOCS16 "High" Delay Time		60	ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	40		ns
t_{WW}	-IOW Pulse Width	100		ns
t_{SDED}	-SDEN Delay Time		60	ns

Reset Timing

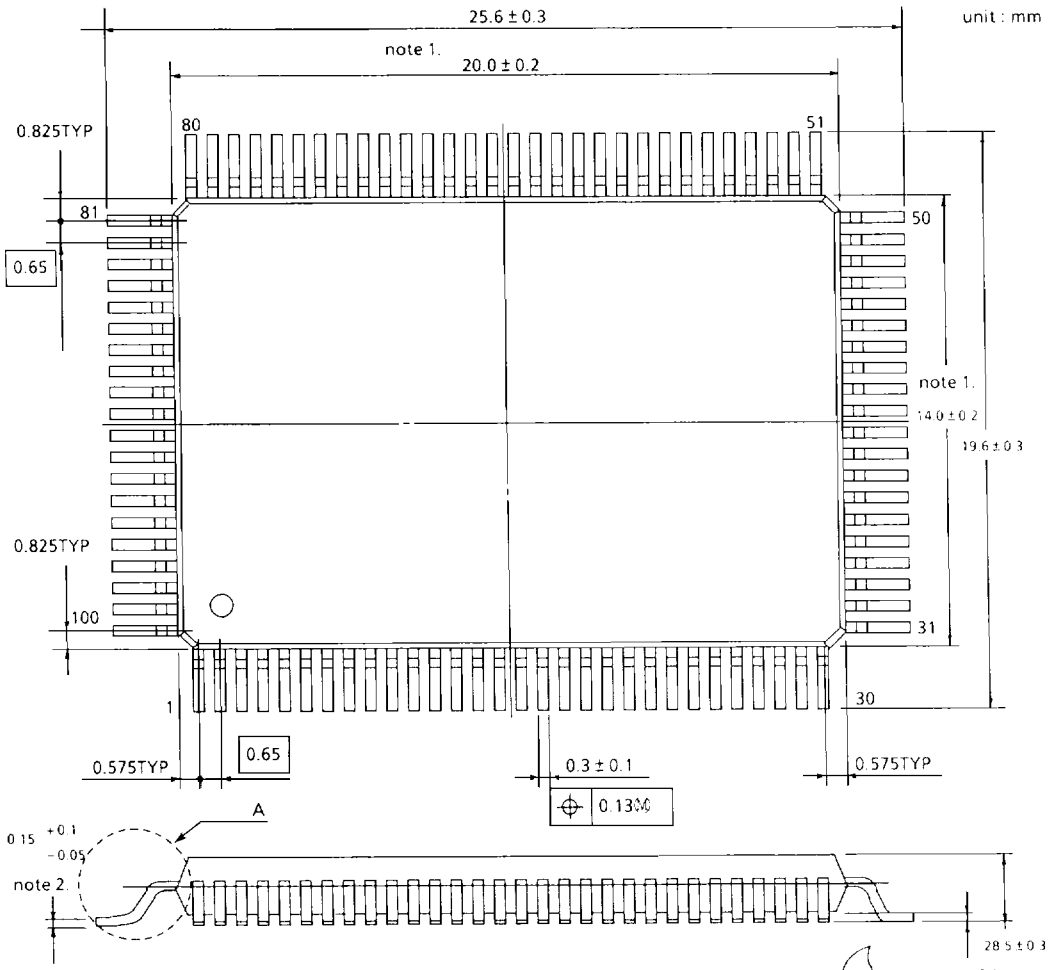


Ta = – 40 ~ + 85°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RW}	Reset Pulse Width	50		ns
t_{RB}	Reset → BUSY Delay Time		80	ns

7. PACKAGE DIMENSION

100 PIN mini FP (Flat Package)



note 1 : Out line dimension of the mold excludes of the remainder of the mold fragment and the tie-bar-cut. However, the remainder of the mold fragment and the tie-bar-cut are 0.15mm Max in each side.

note 2: Apply to the flat part of the lead.