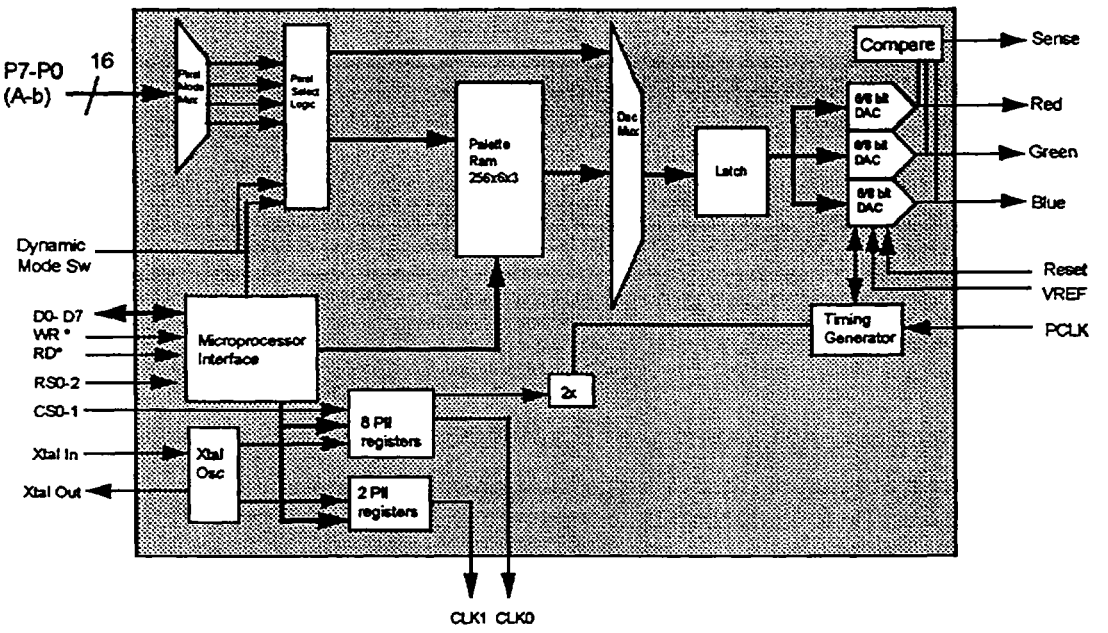
Integrated Circuit Systems, Inc.

Advance Information

16 bit integrated Clock, Palette Ram and DACs



Features:

- Triple 8 bit video DAC, dual clock generators, 256x6x3 palette, 16 bit pixel port
- Dynamic mode switch allows switching of color depth on a pixel by pixel basis. Ideal for multimedia video in a window applications
- Supports 8 bit pseudo, 15 bit, 16 bit hi-color and 24 bit true color (packed and sparse) modes
- On-chip loop filters reduce external components
- Eight programmable pixel clock frequency locations.
- Two programmable memory clock frequency locations
- DAC power down during blanking.
- Internal voltage reference
- Anti-sparkle circuitry
- Standard CPU interface, single external crystal (typically 14.318 MHz)
- Very low clock jitter

Color Modes:

8 bit interface

Mode number	CM3	CM2	CM1	CM0	COLOR MODE	CLOCK CYCLES/ PIXEL BITS
0	0	0	0	0	8 bit pseudo color with palette	1
1	0	0	0	1	15 bit direct color with bypass	2
3	0	0	1	0	24 bit true color with bypass	3
2	0	0	1	1	16 bit direct color with bypass	2
1	0	1	0	0	15 bit direct color with bypass	2
1	0	1	0	1	15 bit direct color with bypass	2
2	0	1	1	0	16 bit direct color with bypass	2
3	0	1	1	1	24 bit true color with bypass	3

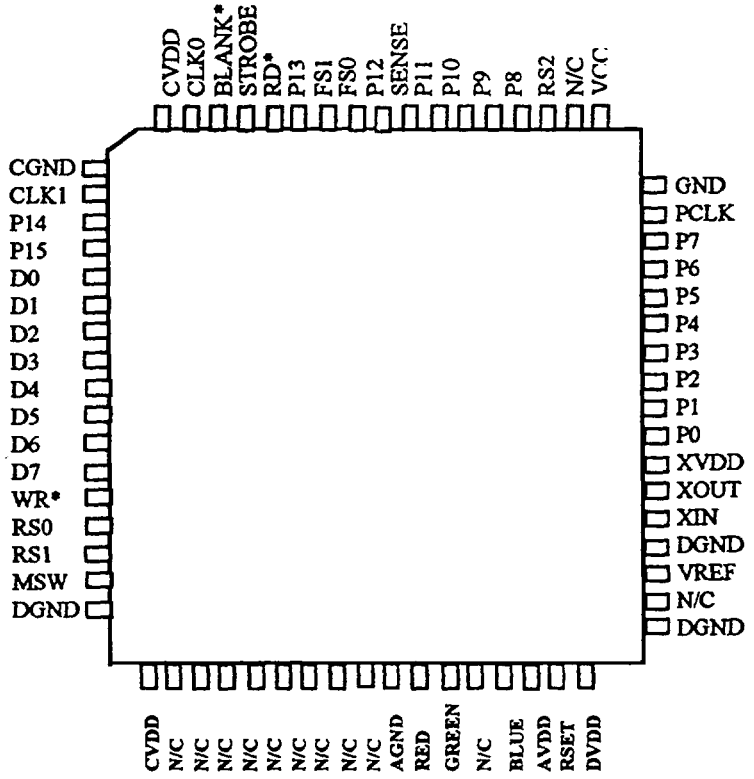
16 bit interface

Mode number	CM 3	CM 2	CM 1	CM 0	COLOR MODE	CLOCK CYCLES/ PIXEL BITS
4	1	0	0	0	Muxed 16 bit pseudo color with palette	1/2
5	1	0	0	1	15 bit direct color with bypass	1
6	1	0	1	0	16 bit direct color with bypass	1
7	1	0	1	1	24 bit true color with bypass	2
8	1	1	0	1	24 bit packed true color with bypass	3/2

Mode Select Operation:

The mode select pin MSW will toggle the chip between the primary mode and the secondary mode when "mode Enable Bit, " bit 2 of the Control Register is set. MSW will switch between two modes- 8 bit pseudo color (mode 0) and 16 bit pixel interface 16 bit direct color bypass mode (mode 6). If mode 0 is selected MSW = 0 will select the primary mode 0 and MSW =1 will select the secondary mode as mode 6 and MSW =1 will select the secondary mode as mode 0. By connecting the MSW pin to Vss the primary color mode is always selected.

Pin Configuration:



Pin Description (68 pin PLCC)

Symbol	Pin #	Type	Description
D7 - D0	14 - 21	I/O	Systems data bus I/O. These bi-directional Data I/O lines are used by the host microprocessor to write (using active low WR*) information into, and read (using active low RD*) information from the six internal registers (Pixel Address, Color Value, Pixel Mask, PLL Address, PLL Parameter, and Command). During the write cycle, the rising edge of WR* latches the data into the selected register (set by the status of the three RS pins). The rising edge of RD* determines the end of the read cycle. When RD* is a logical high, the Data I/O lines no longer contain information from the selected register and will go into a tri-state mode.
RD*	5	Input	RAM/PLL Read Enable, active low. This is the READ bus control signal. When active, any information present on the internal data bus is available on the Data I/O lines, D0-D7.
WR*	22	Input	RAM/PLL Write Enable, active low. This signal controls the timing of the write operation on the microprocessor interface inputs, D0-D7.
RS2 RS1 RS0	63 24 23	Input Input Input	Register Address Select 0. These inputs control the selection of one of the six internal registers. They are sampled on the falling edge of the active enable signal (RD* or WR*).
CVDD	27	-	Crystal oscillator and CLK0 power supply connect to AVDD.
XIN	48	Input	Crystal input. A 14.318 MHz crystal should be connected to this pin.
XOUT	49	Output	Crystal output. A 14.318 MHz crystal should be connected to this pin.
XVDD	50	-	Crystal oscillator power supply. Connect to AVDD.
MSW	25	Input	Mode switch. digital control for selecting primary and secondary pixel color modes. Low selects primary mode. connect to ground if not used.
CGND	26	-	VSS for CLK0. Connect to ground.
CLK1	11	Output	Memory clock output. Used to time the video memory.
CGND	10	-	VSS for CLK1. Connect to ground.
CLK0	8	Output	Video clock output. Provides a CMOS level pixel or dot clock frequency to the graphics controller. The output frequency is determined by the values of the PLL registers.
CVDD	9	-	CLK1 Power Supply. Connect to AVDD.
CS0	2	Input	Clock select 0. The status of CS0-1 determine which frequency is selected on the CLK0 (video) output.
CS1	3	Input	Clock select 1. The status of CS0-1 determine which frequency is selected on the CLK0 (video) output.
DGND	47	-	Vss for XTAL oscillator.
VREF	46	I/O	Internal Reference Voltage. Normally connects to a 0.1µ cap to ground. To use an external Vref, connect a 1.235V reference to this pin.

Pin Description (continued)

Symbol	Pin #	Type	Description
RSET	42	Input	Resistor Set. This pin is used to set the current level in the analog outputs. It is usually connected through a 140Ω, 1% resistor to ground.
SENSE*	68	Output	Monitor Sense, active low. This pin is low when any of the red, green, or blue outputs have exceeded 335mV. The chip has on-board comparators and an internal 335mV voltage reference. This is used to detect monitor type.
AVDD	41	-	DAC power supply. Connect to AVDD.
BLUE GREEN RED	40 38 37	Output Output Output	Color Signals. These three signals are the DACs' analog outputs. Each DAC is composed of several current sources. The outputs of each of the sources are added together according to the applied binary value. These outputs are typically used to drive a CRT monitor.
P0 - P15	51-58, 64067, 1-4, 12, 13	Input	Pixel Address Lines. This byte-wide information is latched by the rising edge of PCLK when using the Color Palette, and is masked by the Pixel Mask register. These values are used to specify the RAM word address in the default mode (accessing RAM). In the Hi-Color XGA, and True Color modes, they represent color data for the DACs. These inputs should be grounded if they are not used.
AGND	36	-	DAC Ground. Connect to ground.
DVDD	43	-	Digital power supply.
PCLK	59	Input	Pixel Clock. The rising edge of PCLK controls the latching of the Pixel Address and BLANK* inputs. This clock also controls the progress of these values through the three-stage pipeline of the Color Palette RAM, DAC, and outputs.
STROBE	6	Input	Latches the input clock select signals CS0-CS1.
BLANK*	7	Input	Composite BLANK* Signal, active low. When BLANK* is asserted, the outputs of the DACs are zero and the screen becomes black. The DACs are automatically powered down to save current during blanking. The color palette may still be updated through D0-D7 during blanking.
DGND	44	-	Digital Ground. Connect to ground.

Internal Registers

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
				There is a single Pixel Address register within the GENDAC. This register can be accessed through either register address 0,0,0 or register address 0,1,1. A read from address 0,0,0 is identical to a read from address 0,1,1. Writing a value to address 0,0,0 performs the following operations: a) Specifies an address within the color palette RAM. b) Initializes the Color Value register. Writing a value to address 0,1,1 performs the following operations: a) Specifies an address within the color palette RAM. b) Loads the Color Value register with the contents of the location in the addressed RAM palette and then increments the Pixel Address register.
0	0	0	Pixel Address WRITE	Writing to this 8-bit register is performed prior to writing one or more color values to the color palette RAM.
0	1	1	Pixel Address READ	Writing to this 8-bit register is performed prior to reading one or more color values from the color palette RAM.
0	0	1	Color Value	The 18-bit Color Value register acts as a buffer between the microprocessor interface and the color palette. Using a three bytes transfer sequence allows a value to be read from or written to this register. When a byte is read, the color value is contained in the least significant 6 bits, D0-D5 (the most significant 2 bits are set to zero). When writing a byte, the same 6 bits are used. When reading or writing, data is transferred in the same order - the red byte first, then green, then blue. Each transfer between the Color Value register and the color palette replaces the normal pixel mapping operations of the GENDAC for a single pixel. After writing three definitions to this register, its contents are written tot he location in the color palette RAM specified by the Pixel Address register, and the Pixel Address register increments. After reading three definitions from this register, the contents of the location in the color palette RAM specified by the Pixel Address registers are copied into the Color Value register, and the Pixel Address register increments.

Internal Registers (continued)

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
0	1	0	Pixel Mask	The 8-bid Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P0-P7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, while a zero sets that bit to zero. The Pixel Mask register does not affect the Pixel Address generated by the microprocessor interface when the palette RAM is being accessed. The I.D. register will be read on the forth consecutive read of the mask register. I.D. for this part is 10110001.

Functional Description

This section describes the register address and bit definition for RAMDAC and the Frequency Synthesizer sections.

Color Palette

Command Register

(RS0-RS2 = 011)

(RS0-RS1 = 01 with hidden flag)

By setting bits in the command register the ICS5340 can be programmed for different color modes and can be powered down for low power operations.

7	6	5	4	3	2	1	0
Color Mode							Snooze
2	1	0	3	=0	ME	=0	

Table 3 - Command Registers

Bit 7-4 **Color Mode Select**

These three bits select the Color Mode of RAMDAC operation as shown in the ICS5340 data sheet (default is 0 at power up);

Bit 3,1 **(Reserved)**

Bit 2 **Mode enable ME**

When this bit is set to 0 (default is 0), mode switch is disabled. If this bit is set to 1, the MSW pin will be enabled.

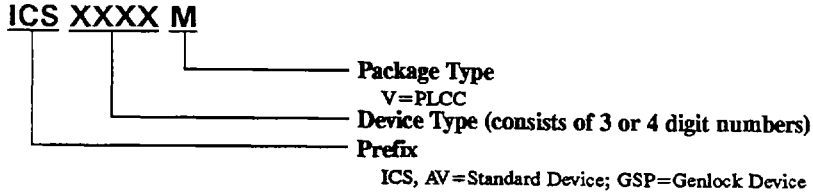
Bit 0 **Power Down Mode of RAMDAC**

When this bit is set to 0 (default is 0), the device operates normally. If this bit is set to 1, the power and clock to the Color Palette RAM and DACs are turned off. The data in the Color Palette RAM are still preserved. The CPU can access without loss of data by internal automatic clock start/stop control. The DAC outputs become the same as BLANK* (sync) level output during power down mode. This bit does not effect the PLL clock synthesizer function.

Ordering Information

ICS5342V

Example:



Integrated Circuit Systems, Inc.

ICS Sales Offices

Eastern & Central Area

Headquarters
Integrated Circuit Systems, Inc.
2435 Boulevard of the Generals, P.O. Box 968
Valley Forge, PA 19482-0968
Phone: (610) 630-5300
Fax: (610) 630-5399
Toll-Free: 1-800-220-3366

Western Area

Integrated Circuit Systems, Inc.
1271 Parkmoor Avenue
San Jose, CA 95126
Phone: (408) 297-1201
Fax: (408) 925-9460

Domestic — ICS Sales Representatives

Alabama
Elcom
Suite 145K
4960 Corporate Drive
Huntsville, Al 35805
Phone: (205) 830-4001
Fax: (205) 830-4058

Arizona
Toward Engineering Associates
Suite 2
4520 E. Indian School Rd.
Phoenix, AZ 85018
Phone: (602) 955-3193
Fax: (602) 955-3224

Arkansas
Impaq Sales
Ste. 140, 100 Decker Court
Irving, TX 75062
Phone: (214) 650-0000
Fax: (214) 650-1953

California
(Northern)
Nexus Manufacturers' Rep, Inc.
555 Mathilda Avenue
Sunnyvale, CA 94086
Phone: (408) 720-4787
Fax: (408) 720-4453

(Southern)
TNT & Associates, Inc.
Suite 19
22865 Lake Forest Drive
Lake Forest, CA 92630
Phone: (714) 830-6096
Fax: (714) 830-0154

Colorado
Waugaman Associates, Inc.
4800 Van Gordon Street
Wheat Ridge, CO 80033
Phone: (303) 423-1020
Fax: (303) 467-3095

Connecticut
Delta Conn Technical Sales
Ste. 206, One Prestige Dr.
Meriden, CT 06450
Phone: (203) 634-8558
Fax: (203) 238-1240

District of Columbia
S-J Chesapeake
Ste. 307, 900 S. Washington St.
Falls Church, VA 22046
Phone: (703) 533-2233
Fax: (703) 533-2236

Florida
Semtronic Associates
657 Maitland Avenue
Altamonte Springs, FL 32701
Phone: (407) 831-8233
Fax: (407) 831-2844

Florida *(continued)*
(Western)
1467 S. Missouri Avenue
Clearwater, FL 34616
Phone: (813) 461-4675
Fax: (813) 442-2234

(Southern)
3471 N.W. 55th Street
Ft. Lauderdale, Fl 33309
Phone: (305) 731-2484
Fax: (305) 731-1019

Georgia
Elcom
3060C Business Park Dr.
Norcross, GA 30071
Phone: (404) 447-8200
Fax: (404) 447-8340

Idaho
Waugaman Associates, Inc.
876 E. Vine Street
Salt Lake City, UT 84107
Phone: (801) 261-0802
Fax: (801) 261-0830

Illinois
KMA Sales
1040 S. Arlington Heights Rd.
Arlington Heights, IL 60005
Phone: (708) 398-5300
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Indiana
Phoenix Marketing Group, Inc.
11625 Sea Star Way
Fishers, IN 46038
Phone: (317) 577-4112
Fax: (317) 576-1155

Kansas
Impaq Sales
1434 East Sheridan
Olathe, KS 66062
Phone: (913) 780-6565
Fax: (913) 780-1484

Kentucky
Phoenix Marketing Group, Inc.
11625 Sea Star Way
Fishers, IN 46038
Phone: (317) 577-4112
Fax: (317) 576-1155

Louisiana
Impaq Sales
Ste. 140, 100 Decker Court
Irving, TX 75062
Phone: (214) 650-0000
Fax: (214) 650-1953

Maryland
S-J Chesapeake
Ste. 307, 900 S. Washington St.
Falls Church, VA 22046
Phone: (703) 533-2233
Fax: (703) 533-2236

Massachusetts
The Nashoba Group
One Technology Park Dr.
Westford, MA 01886
Phone: (508) 692-7503
Fax: (508) 692-5081

Michigan
C.B. Jensen & Associates
Ste. 201, 2145 Crooks Rd.
Troy, MI 48084-5318
Phone: (810) 643-0506
Fax: (810) 643-4735

Minnesota
Reptek
3433 Broadway St., N.E.
Minneapolis, MN 55413
Phone: (612) 331-1212
Fax: (612) 331-8783

Mississippi
Elcom
Suite 145K
4960 Corporate Drive
Huntsville, AL 35805
Phone: (205) 830-4001
Fax: (205) 830-4058

Missouri
Impaq Sales
1434 East Sheridan
Olathe, KS 66062
Phone: (913) 780-6565
Fax: (913) 780-1540

Montana
Waugaman Associates
4800 Van Gordon Street
Wheat Ridge, CO 80033
Phone: (303) 423-1020
Fax: (303) 467-3095

Nebraska
Impaq Sales
1434 East Sheridan
Olathe, KS 66062
Phone: (913) 780-6565
Fax: (913) 780-1540

New York
Astrorep, Inc.
103 Cooper Street
Babylon, NY 11702
Phone: (516) 422-2500
Fax: (516) 422-2504

(Upstate)
FSI Systems, Inc.
833 Phillips Road
Victor, NY 14564-9789
Phone: (716) 924-7510
Fax: (716) 924-0275

New Jersey
(Northern)
Astrorep, Inc.
103 Cooper Street
Babylon, NY 11702
Phone: (516) 422-2500
Fax: (516) 422-2504

(Southern)
Omega Electronic Sales, Inc.
Suite 101
Four Neshaminy Interplex
Trevose, PA 19053
Phone: (215) 244-4000
Fax: (215) 244-4104

New Hampshire
The Nashoba Group
One Technology Park Dr.
Westford, MA 01886
Phone: (508) 692-7503
Fax: (508) 692-5081

New Mexico
Toward Engineering Associates
Suite 2
4520 E. Indian School Rd.
Phoenix, AZ 85018
Phone: (602) 955-3193
Fax: (602) 955-3224

North Carolina
Elcom
3060C Business Park Dr.
Norcross, GA 30071
Phone: (404) 447-8200
Fax: (404) 447-8340

Ohio
Technology Marketing Corp.
Suite 11A
9200 Montgomery Road
Cincinnati, OH 45242
Phone: (513) 984-6720
Fax: (513) 984-6874

Technology Marketing Corp.
One Independence Place
4807 Rockside Rd., Ste.360
Independence, OH 44131
Phone: (216) 520-0150
Fax: (216) 520-0190

Oklahoma
Impaq Sales
Ste. 140, 100 Decker Court
Irving, TX 75062
Phone: (214) 650-0000
Fax: (214) 650-1953

Oregon
Advance Technical
Marketing, Inc.
Suite 155
4900 S.W. Griffith Drive
Beaverton, OR 97005
Phone: (503) 643-8307
Fax: (503) 643-4364

Pennsylvania
(Eastern)
Omega Electronic Sales, Inc.
Suite 101
Four Neshaminy Interplex
Trevose, PA 19053
Phone: (215) 244-4000
Fax: (215) 244-4104

(Western)
Technology Marketing Corp.
7017 Pearl Road
Middleburg Heights, OH 44130
Phone: (216) 885-5544
Fax: (216) 885-5011

Rhode Island
The Nashoba Group
One Technology Park Dr.
Westford, MA 01886
Phone: (508) 692-7503
Fax: (508) 692-5081

South Carolina
Elcom
3060C Business Park Dr.
Norcross, GA 30071
Phone: (404) 447-8200
Fax: (404) 447-8340

Tennessee
Elcom
Suite 145K
4960 Corporate Drive
Huntsville, AL 35805
Phone: (205) 830-4001
Fax: (205) 830-4058

Texas
Impaq Sales
Ste. 140, 100 Decker Court
Irving, TX 75062
Phone: (214) 650-0000
Fax: (214) 650-1953

Impaq Sales
Suite 308
13706 North Highway 183
Austin, TX 78750
Phone: (512) 335-9666
Fax: (512) 335-3858

Impaq Sales
Suite 530
507 North Belt East
Houston, TX 77060
Phone: (713) 820-0288
Fax: (713) 820-4860

Utah
Waugaman Associates, Inc.
876 E. Vine Street
Salt Lake City, UT 84107
Phone: (801) 261-0802
Fax: (801) 261-0830

Vermont
The Nashoba Group
One Technology Park Dr.
Westford, MA 01886
Phone: (508) 692-7503
Fax: (508) 692-5081

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S-J Chesapeake
Suite 307
900 S. Washington Street
Falls Church, VA 22046
Phone: (703) 533-2233
Fax: (703) 533-2236

Washington
Advance Technical
Marketing, Inc.
8521 154th Avenue N.E.
Redmond, WA 98052
Phone: (206) 869-7636
Fax: (206) 869-9841

Wisconsin
KMA Sales
Suite 202
2433 North Mayfair Road
Milwaukee, WI 53226-1406
Phone: (414) 259-1771
Fax: (414) 259-0246

Wyoming
Waugaman Associates, Inc.
4800 Van Gordon Street
Wheat Ridge, CO 80033
Phone: (303) 423-1020
Fax: (303) 467-3095

Integrated Circuit Systems, Inc.

ICS Sales Offices

Eastern & Central Area

Headquarters
Integrated Circuit Systems, Inc.
2435 Boulevard of the Generals, P.O. Box 968
Valley Forge, PA 19482-0968
Phone: (610) 630-5300
Fax: (610) 630-5399
Toll-Free: 1-800-220-3366

Western Area

Integrated Circuit Systems, Inc.
1271 Parkmoor Avenue
San Jose, CA 95126
Phone: (408) 297-1201
Fax: (408) 925-9460

International ICS Sales Representatives

Australia
(Please call ICS Headquarters for the rep in this area.)

Belgium
ACAL Auriema
Lozenberg 4
B-1932 Zaventem
Phone: (32) 2 720 59 83
Fax: (32) 2 725 10 14

Canada
(Alberta and British Columbia only)
Advance Technical Marketing, Inc.
8521 154th Avenue N.E.
Redmond, WA 98052
Phone: (206) 869-7636
Fax: (206) 869-9841

(Eastern)
Dynasty Components
#110-1140 Morrison Dr.
Ottawa, Ontario K2H 8S9
Phone: (613) 596-9800
Fax: (613) 596-9886

Denmark
NC NordComp Denmark AS
Titangade 15
2200 Copenhagen N
Phone: (45) 38 88 65 88
Fax: (45) 38 88 65 11

Finland
IE Oy AB
Turkhaudantie 1
SF-00700 Helsinki
Phone: (358) 0-351 3133
Fax: (358) 0-351 3134

France
Tekelec Airtronic
5, Rue Carle Vernet
92315 Sevres Cedex
Phone: (33) 1 46 23 24 25
Fax: (33) 1 45 07 21 91

Germany
Scantec GmbH
Behringstrasse 10
D-82152 Planegg
Phone: (49) 89 8 99 14 30
Fax: (49) 89 8 57 65 74

Scantec GmbH
Tannenbergstrasse 103
73230 Kirchheim/Teck
Phone: (49) 70 2 18 30 94
Fax: (49) 70 2 18 25 68

Germany *(continued)*
Topas Electronic GmbH
Striehlstrasse 18
30159 Hannover
Phone: (49) 51 1 13 12 17
Fax: (49) 51 1 13 12 16

Topas Electronic GmbH
Max-Weber Strasse 16
25451 Quickborn
Phone: (49) 41 06 73097
Fax: (49) 41 06 73378

Hong Kong
RTI Industries Co., Ltd.
Room 402
Nan Fung Commercial Centre
No. 19, Lam Lok Street
Kowloon Bay, Kowloon,
Hong Kong
Phone: (852) 795-7421
Fax: (852) 795-7839

Electrocon Products Ltd.
8/F, Blk. B,
Prosperity Centre
77 Container Port Road
Kwai Chung, N.T.,
Hong Kong
Phone: (852) 481-6022
Fax: (852) 481-5804

Israel
ELDIS Technologies Ltd.
4 Hess Street
Herzlia 46486
Phone: (972) 9 562666
Fax: (972) 9 562642

Italy
Sitel S.P.A.
Via Po, 37
20031 Cesano Maderno
Milan
Phone: (39) 362 524941
Fax: (39) 362 501516

Comprel S.P.A.
Via Po, 37
20031 Cesano Maderno
Milan
Phone: (39) 362 553 991
Fax: (39) 362 553 967
(Distribution Office)

Japan
Micro Summit K.K.
Premier Ki Building, 4F
1, Kanda Mikura-cho
Chiyoda-ku, Tokyo 101
Phone: (81) 3 3258-5531
Fax: (81) 3 3258-0433

Nichimen Elect.Comp. Corp.
Yokobori Kurisu Bldg. 2F,
8-5, Koraibashi 4-Chome,
Chuo-ku, Osaka 541
Phone: (81) 6 226-0015
Fax: (81) 6 226-0016

Rymex
Suite 201
1333 Lawrence Expressway
Santa Clara, CA 95051
Phone: (408) 296-6626
Fax: (408) 296-2063

Korea
Acetronix
Parklim Bldg., #402
Seobingko-Dong 95
Yongsan-Ku, Seoul
Phone: (82) 2 796-4561
Fax: (82) 2 796-4563

Netherlands
ACAL Auriema
Beatrix de Rijkweg 8
5657 EG Eindhoven
Phone: (31) 40 502 602
Fax: (31) 40 510 255

New Zealand
(Please call ICS Headquarters for the rep in this area.)

Norway
NC NordComp Norway AS
Vestvollveien 6
2020 Skedsmokorset
Phone: (47) 63 87 93 30
Fax: (47) 63 87 90 00

Puerto Rico
Semtronic Associates
Suite 816
Mercantil Plaza Building
Hato Rey, Puerto Rico 00918
Phone: (809) 766-0700
Fax: (809) 763-8071

Singapore
Scan Technology Pte. Ltd.
50 Kallang Bahru
#04-01/03
Kallang Industrial Estate
Singapore 1233
Phone: (65) 294-2112
Fax: (65) 296-1685

Scan Components (M)SDN BHD
761-B Jalan Sultan Azlan Shah
Sungai Nibong, 11900 Penang
Malaysia
Phone: (60) 4-835136
Fax: (60) 4-836320

Sweden
IE Komponenter AB
Ulvsundavagen 106
S-16111 Bromma
Phone: (468) 80 46 85
Fax: (468) 26 22 86

Taiwan
Maxtek Technology Co. Ltd.
3F, No. 197
Section 4, Nanking E. Road
Taipei, Taiwan ROC
Phone: (886) 2 713-0209
Fax: (886) 2 712-6780

Princeton Technology Corp.
2F, No. 233-1
Bao Chiao Road
Hsin Tien, Taipei Hsien
Taiwan, ROC
Phone: (886) 2 917-8856
Fax: (886) 2 917-3836

United Kingdom
Amega Technology
Loddon Business Centre
Roentgen Road,
Daneshill East,
Basingstoke,
Hants, RG24 ONG
Phone: (44) 256 330 301
Fax: (44) 256 330 302

ICS Distribution/USA

Nu Horizons Electronics Corp.

New York
Nu Horizons
6000 New Horizons Blvd.
Amityville, NY 11701
Phone: (516) 226-6000
Fax: (516) 226-6140

333 Metro Park
Rochester, NY 14623
Phone: (716) 292-0777
Fax: (716) 292-0750

Alabama
Nu Horizons
Suite 11
4801 University Square
Huntsville, AL 35816
Phone: (205) 722-9330
Fax: (205) 722-9348

California
Nu Horizons
2070 Ringwood Avenue
San Jose, CA 95131
Phone: (408) 434-0800
Fax: (408) 434-0935

Florida
(North)
Nu Horizons
Suite 270
600 S. North Lake Blvd.
Altamonte Springs, FL 32701
Phone: (407) 831-8008
Fax: (407) 831-8862

Nu Horizons
3421 N.W. 55th Street
Ft. Lauderdale, FL 33309
Phone: (305) 735-2555
Fax: (305) 735-2880

Georgia
Nu Horizons
Suite 370
5555 Oakbrook Parkway
Norcross, GA 30093
Phone: (404) 416-8666
Fax: (404) 416-9060

Maryland
Nu Horizons
Suite 160
8965 Guilford Road
Columbia, MD 21046
Phone: (410) 995-6330
Fax: (410) 995-6332

Massachusetts
Nu Horizons
19 Corporate Place, Bldg. 1
107 Audubon Road
Wakefield, MA 01880
Phone: (617) 246-4442
Fax: (617) 246-4462

Minnesota
Nu Horizons
6955 Washington Ave., South
Edina, MN 55439
Phone: (612) 942-9030
Fax: (612) 942-9144

New Jersey
Nu Horizons
39 U.S. Route 46
Pine Brook, NJ 07058
Phone: (201) 882-8300
Fax: (201) 882-8398

Ohio
Nu Horizons
Suite A-15
6200 SOM Center Road
Solon, OH 44139
Phone: (216) 349-2008
Fax: (216) 349-2080

Pennsylvania
Nu Horizons
Suite 200
18000 Horizon Way
Mt. Laurel, NJ 08054
Phone: (215) 557-6450 (PA)
Phone: (609) 231-0900 (NJ)
Fax: (609) 231-9510

Texas
Nu Horizons
2081 Hutton Dr., Suite 119
Carrollton, TX 75006
Phone: (214) 488-2255
Fax: (214) 488-2265

** Country & city codes listed apply to U.S. residents only. International calls placed outside of the U.S. should check with local telephone service for correct codes.