WaveFront™ Sounds (4M bit CMOS Mask ROM)

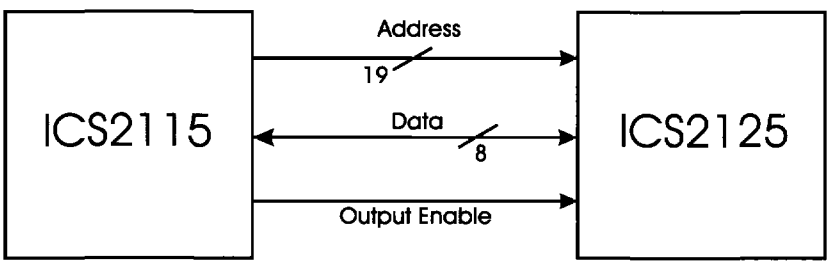
General Description

WaveFront Sounds are masked ROMs that serve as the wavetable for the ICS2115 WaveFront Synthesizer. Three different sounds sets are available: 4 MB (ICS2124-001 and ICS2124-002), 2 MB (ICS2122) and 512 KB (ICS2125). Each sound set contains the musical data needed to synthesize instruments from the General MIDI specification. The 512 KB sound set consists of one 512 KB ROM.

Features

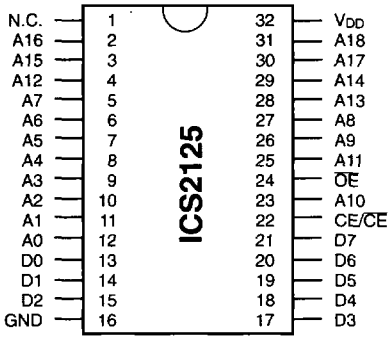
- Full featured set of General MIDI sounds.
- Available in three sizes, 4 MB, 2 MB, and 512 KB to provide the optimal balance between price and performance for many applications.
- Uses 512K Word X 8 bit ROM in a 32-pin SOP package.

Block Diagram



512K Patch Set

Pin Configuration



32-Pin SOP
K-8

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2-12, 23, 25-31	A0 through A18	I	Address Inputs
13-15, 17-21	D0 through D7	O	Data Outputs
24	$\overline{OE}$	I	Output Enable Input
22	$\overline{CE}$	I	Chip Enable Input
32	V_{DD}	P	Power Supply
16	GND	P	Ground
1	N.C.	-	No Connection

Absolute Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5-7.0	V
V_{IN}	Input Voltage	-0.5-V_{DD}	V
V_{OUT}	Output Voltage	0 - V_{DD}	V
P_D	Power Dissipation	1.0/0.6	W
T_{STG}	Storage Temperature	-55 to 150	° C
T_{OPR}	Operating Temperature	0 - 70	° C
T_{SOLDER}	Soldering Temperature - Time	260 - 10	° C - sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

AC Characteristics

T_A = 0~70°C, V_{DD}=5±10%

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Cycle Time	t_{CYC}	150	-	-	ns
Address Access Time	t_{ACC}	-	-	150	ns
Chip Enable Access Time	t_{CE}	-	-	150	ns
Output Enable Access Time	t_{OE}	-	-	70	ns
Output Disable Time from $\overline{CE}$	t_{CED}	-	-	40	ns
Output Disable Time from $\overline{OE}$	t_{OED}	-	-	40	ns
Output Hold Time	t_{OH}	5	-	-	ns

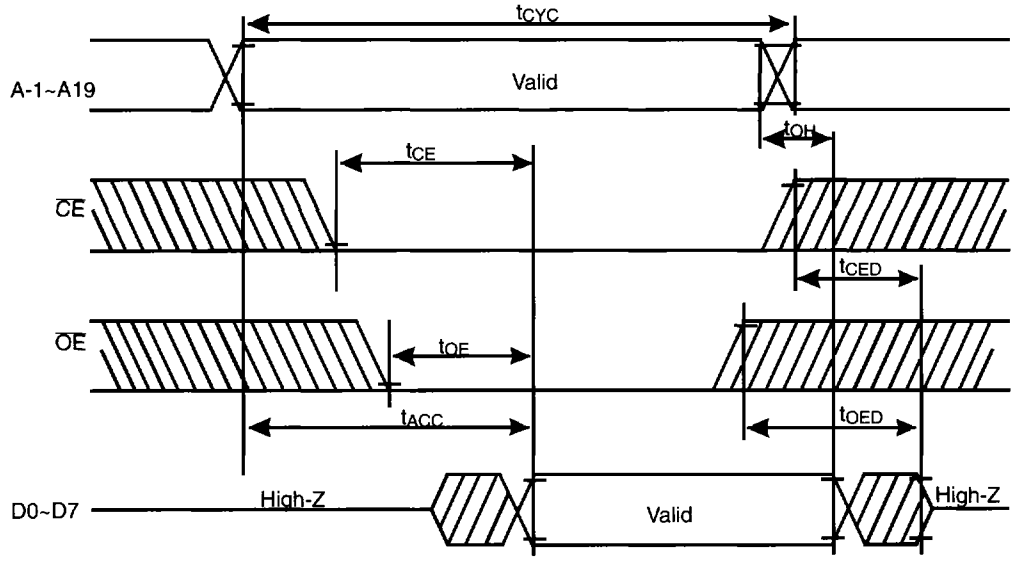
AC Test Conditions

Output Load: 100pf + 1TTL
Input Levels: 0.6V, 2.4V
Timing Measurement Reference Levels/Input: 0.8V, 2.2V
Timing Measurement Reference Levels/Output: 0.8V, 2.0V
Input Rise and Fall Time: 5ns

G

Timing Diagram

BYTE-WIDE READ MODE



Note: $\overline{BYTE}=V_{IL}$

Ordering Information

ICS2125M

Example:

ICS XXXX M

Package Type
M=SOP

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device