PCM FRAME ALIGNER

FEATURES

- Frame Alignment Recovery and loss in accordance with CCITT recommendations G.732 and G.737
- Jitter and phase-wander immunity exceed the requirements of CCITT recommendation G.823.
- Internal 1½ frame elastic buffer.
- Detection of incoming Alarm-Indication-Signal (AIS), and Distant Alarm
- Indication of Slip, loss of frame synchronisation, and loss of route clock conditions.
- ISO-CMOS technology, TTL Compatible.
- Pin-for-Pin replacement for Siemens PEB 2030 and SM 300
- Microprocessor Interface

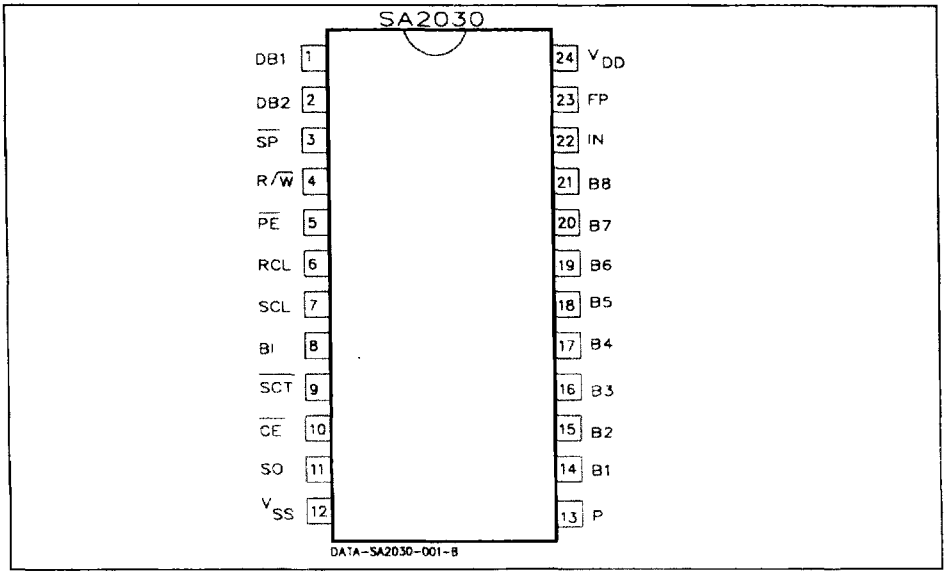
APPLICATIONS

- Delay compensation and clock alignment between 2,048MHz PCM-30 transmission lines, and terminating equipment.
- Control of Jitter and Wander within Digital Networks.
- Delay compensation between switching stages.
- Interfacing of PCM systems operating with different clocks.
- PCM concentrators and subscriber multiplexers.

GENERAL DESCRIPTION

The SA2030 is designed to interface PCM-30 routes with switching systems. The device synchronises with the frame-format of the incoming data, and outputs this data in accordance with the bit and frame timing of the terminating equipment. The circuit is designed to tolerate delay, drift, wander and jitter of the incoming data and clock, and thus simplifies the design of data- and clock-recovery hardware. The internal 1½ frames elastic buffer provides for delay compensation and wander immunity. If the bounds of the buffer are exceeded, the SA2030 will either repeat or drop a frame. The circuit will accurately detect incoming Alarm-Indication-Signal (AIS) conditions, in accordance with CCITT recommendation G.737. Loss of frame alignment is indicated on both dedicated outputs and by outputting of AIS. The circuit includes a bidirectional alarm port for interrogation of alarm conditions.

PIN CONFIGURATION



BLOCK DIAGRAM