

Quad MECL-to-TTL Translator

The MC10H125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic section of digital systems. The 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

Outputs of unused translators will go to low state when their inputs are left open.

- Propagation Delay, 2.5 ns Typical
- Improved Noise Margin 150 mV
- Voltage Compensated
- MECL 10K-Compatible (Over Operating Voltage and Temperature Range)

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply ($V_{CC} = 5.0$ V)	V_{EE}	-8.0 to 0	Vdc
Power Supply ($V_{EE} = -5.2$ V)	V_{CC}	0 to +7.0	Vdc
Input Voltage ($V_{CC} = 5.0$ V)	V_I	0 to V_{EE}	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic	T_{stg}	-55 to +150	°C
— Ceramic		-55 to +165	°C

ELECTRICAL CHARACTERISTICS ($V_{EE} = -5.2$ V $\pm 5\%$; $V_{CC} = 5.0$ V $\pm 5.0\%$)

(See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Negative Power Supply Drain Current	I_E	—	44	—	40	—	44	mA
Positive Power Supply Drain Current	I_{CCH}	—	63	—	63	—	63	mA
	I_{CCL}	—	40	—	40	—	40	mA
Input Current	I_{IH}	—	225	—	145	—	145	μ A
Input Leakage Current	I_{CBO}	—	1.5	—	1.0	—	1.0	μ A
High Output Voltage $I_{OH} = -1.0$ mA	V_{OH}	2.5	—	2.5	—	2.5	—	Vdc
Low Output Voltage $I_{OL} = +20$ mA	V_{OL}	—	0.5	—	0.5	—	0.5	Vdc
High Input Voltage(1)	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage(1)	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
Short Circuit Current	I_{OS}	60	150	60	150	50	150	mA
Reference Voltage	V_{BB}	-1.38	-1.27	-1.35	-1.25	-1.31	-1.19	Vdc
Common Mode Range (3)	V_{CMR}	—	—	-2.85 to -0.3				V
		Typical						
Input Sensitivity (4)	V_{PP}	150						mV

AC PARAMETERS

Parameter	Symbol	0.6	3.3	0.85	3.35	0.9	3.4	ns
Propagation Delay	t_{pd}							
Rise Time(5)	t_r	0.3	1.2	0.3	1.2	0.3	1.2	ns
Fall Time(5)	t_f	0.3	1.2	0.3	1.2	0.3	1.2	ns

NOTES:

- When V_{BB} is used as the reference voltage.
- Each MECL 10H series circuit has been designed to meet the specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
- Differential input not to exceed 1.0 Vdc.
- 150 mV $_{PP}$ differential input required to obtain full logic swing on output.
- 1.0 V to 2.0 V w/25 pF into 500 Ω .

MC10H125



L SUFFIX
CERAMIC PACKAGE
CASE 620-10

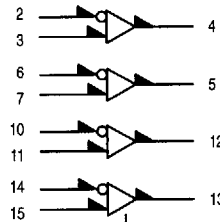


P SUFFIX
PLASTIC PACKAGE
CASE 648-08



FN SUFFIX
PLCC
CASE 775-02

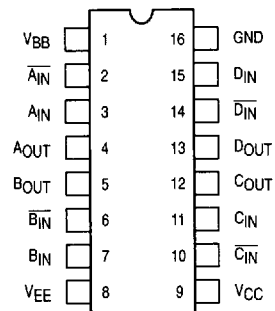
LOGIC DIAGRAM



V_{BB}^*
GND = PIN 16
 V_{CC} (+5.0 VDC) = PIN 9
 V_{EE} (-5.2 VDC) = PIN 8

* V_{BB} to be used to supply bias to the MC10H125 only and bypassed (when used) with 0.01 μ F to 0.1 μ F capacitor to ground (0 V). V_{BB} can source < 1.0 mA.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 6-11.



APPLICATION INFORMATION

The MC10H125 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on Pin 1 for use in single-ended input biasing. The outputs of the MC10H125 go to a low-logic level whenever the inputs are left floating, and a high-logic

output level is achieved with a minimum input level of 150 mV_{p-p}.

An advantage of this device is that MECL-level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL-logic from the noisy TTL environment. Power supply requirements are ground, +5.0 volts and -5.2 volts.

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