AMD 20-Pin PAL* Family

20-Pin IMOX™ Programmable Array Logic Elements

DISTINCTIVE CHARACTERISTICS

- **Fast**
  - High speed "A" versions (t_{pd} = 25ns, t_s = 20ns, t_{co} = 15ns, max)
  - Standard speed versions (t_{pd} = 35ns, t_s = 30ns, t_{co} = 25ns, max)
- **Flexible**
  - User programmability allows customized designs
  - Eases design updates in prototype or product
- **Low Cost**
  - Reduces board space/chip count
  - Reduces design time
  - Reduces inventory cost
- **Reliable**
  - Proven Platinum-Silicide fuse technology
  - Fully AC and DC tested
  - Preload of output registers allows full logical testing

GENERAL DESCRIPTION

AMD PALs are high speed electrically programmable array logic elements. They utilize the familiar sum-of-products (AND-OR) structure allowing users to program custom logic functions to fit most applications precisely.

Initially the AND gates are connected, via fuses, to both the true and complement of every input. By selective programming of fuses the AND gates may be "connected" to only the true input (by blowing the complement fuse), to only the complement input (by blowing the true fuse), or to neither type of input (by blowing both fuses) establishing a logical "don't care." When both the true and complement fuses are left intact a logical false results on the output of the AND gate. An AND gate with all fuses blown will assume the logical true state. The outputs of the AND gates are connected to fixed OR gates. The only limitations imposed are the number of inputs to the AND gates (up to 16) and the number of AND gates per OR (up to 8).

The part types in the AMD PAL family are differentiated by the allocation of registered (with internal feedback) and combinatorial (bi-directional and dedicated) outputs. All combinatorial AMD PALs are available in both active HIGH (AND-OR) and active LOW (AND-OR-INVERT) versions.

AMD PAL FAMILY CHARACTERISTICS

All members of the AMD PAL family have common electrical characteristics and programming procedures. All parts in this family are produced with a fusible link at each input to the AND gate array. Connections may be selectively removed by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming, highly reliable Platinum-Silicide Fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields (> 98%), and provide extra test paths to achieve excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable, long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link programmable logic.

The AMD PAL family is manufactured using Advanced Micro Devices' selective oxidation process, IMOX. This advanced process permits an increase in density and a decrease in internal capacitance resulting in the fastest possible programmable logic devices.

The AMD PAL family also incorporates the unique capability of preloading the output registers during testing to any desired value. Preload is invaluable when testing the logical functionality of a programmed AMD PAL.

AMD PAL FAMILY TABLE

Part Number	Array Inputs	Logic	OE	Outputs	t_{pd} (MAX) STD	t_{pd} (MAX) A	t_s (MAX) STD	t_s (MAX) A	t_{co} (MAX) STD	t_{co} (MAX) A	
AmPAL16R8	(8) Dedicated (8) Feedback	(8) 8-Wide AND-OR	Dedicated	Registered Inverting	–	–	30	20	25	15	ns
AmPAL16R6	(8) Dedicated (6) Feedback (2) *Bidirectional*	(6) 8-Wide AND-OR	Dedicated	Registered Inverting	35	25	30	20	25	15	ns
		(2) 7-Wide AND-OR-INVERT	*Programmable*	*Bidirectional*							
AmPAL16R4	(8) Dedicated (4) Feedback (4) Bidirectional	(4) 8-Wide AND-OR	Dedicated	Registered Inverting	35	25	30	20	25	15	ns
		(4) 7-Wide AND-OR-INVERT	Programmable	Bidirectional							
AmPAL16L8	(10) Dedicated (6) Bidirectional	(8) 7-Wide-AND-OR-INVERT	Programmable	(6) Bidirectional (2) Dedicated	35	25	–	–	–	–	ns
AmPAL16H8	(10) Dedicated (6) Bidirectional	(8) 7-Wide AND-OR	Programmable	(6) Bidirectional (2) Dedicated	35	25	–	–	–	–	ns
AmPAL16LD8	(10) Dedicated (6) Bidirectional	(8) 8-Wide AND-OR-INVERT	–	Dedicated	35	25	–	–	–	–	ns
AmPAL16HD8	(10) Dedicated (6) Bidirectional	(8) 8-Wide AND-OR	–	Dedicated	35	25	–	–	–	–	ns

*PAL is a registered trademark of Monolithic Memories, Inc.
IMOX is a trademark of Advanced Micro Devices, Inc.

Refer to Page 13-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient) Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 20 to Pin 10) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs (Except
During Programming) ..... −0.5V to +V_{CC} max
DC Voltage Applied to Outputs
During Programming 21V
Output Current Into Outputs During
Programming (Max Duration of 1 sec) 200mA
DC Input Voltage ..... −0.5 to +5.5mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2mA	COM'L	2.4	3.5		Volts
			I_{OH} = −2mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	COM'L			0.5	Volts
			I_{OL} = 12mA	MIL				
V_{IH} (Note 2)	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL} (Note 2)	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V				−20	−250	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					25	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.5V (Note 3)			−30	−60	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX	16L8, 16H8, 16HD8, 16LD8 16L8A, 16H8A, 16HD8A, 16LD8A			110	155	mA
			16R8, 16R6, 16R4 16R8A, 16R6A, 16R4A			120	180	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−0.9	−1.2	Volts
I_{OZH}	Output Leakage Current (Note 4)	V_{CC} = MAX, V_{IL} = 0.8V V_{IH} = 2.0V	V_O = 2.7V				100	μA
I_{OZL}			V_O = 0.4V				−100	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @f = 1MHz (Note 5)				6		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @f = 1MHz (Note 5)				9		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
5. These parameters are not 100% tested, but are periodically sampled.

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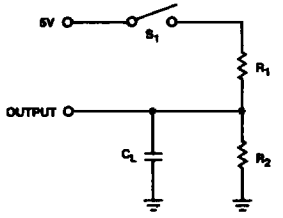
AC TEST LOAD



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SWITCHING CHARACTERISTICS over operating range unless otherwise specified
HIGH SPEED

Parameters	Description	Test Conditions	Typ (Note 1)	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PD}	Input or Feedback to Non-Registered Output 16L8A, 16R6A, 16R4A, 16LD8A, 16H8A, 16HD8A	COM'L $R_1 = 200$ $R_2 = 390$	12		25		30	ns
t_{EA}	Input to Output Enable 16L8A, 16R6A, 16R4A, 16H8A		12		25		30	ns
t_{ER}	Input to Output Disable 16L8A, 16R6A, 16R4A, 16H8A		12		25		30	ns
t_{PZX}	Pin 11 to Output Enable 16R8A, 16R6A, 16R4A		8		20		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8A, 16R6A, 16R4A		8		20		25	ns
t_{CO}	Clock to Output 16R8A, 16R6A, 16R4A		8		15		20	ns
t_s	Input or Feedback Setup Time 16R8A, 16R6A, 16R4A	MIL $R_1 = 390$ $R_2 = 750$	10	20		25		ns
t_H	Hold Time 16R8A, 16R6A, 16R4A		−10	0		0		ns
t_P	Clock Period			35		45		ns
t_W	Clock Width			15		20		ns
t_{MAX}	Maximum Frequency				28.5		22	MHz

Notes: 1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50pF$.
3. For three-state outputs, output enable times are tested with $C_L = 50pF$ to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5pF$. HIGH to high impedance tests are made to an output voltage of $V_{OH} - 0.5V$ with S_1 open; LOW to high impedance tests are made to the $V_{OL} + 0.5V$ level with S_1 closed.

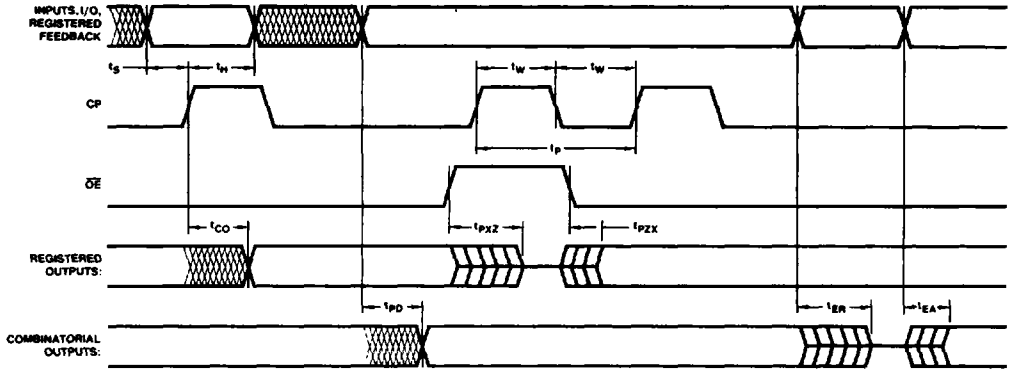
SWITCHING CHARACTERISTICS over operating range unless otherwise specified
STANDARD SPEED

Parameters	Description	Test Conditions	Typ (Note 1)	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4, 16LD8, 16H8, 16HD8	COM'L $R_1 = 200$ $R_2 = 390$	17		35		40	ns
t_{EA}	Input to Output Enable 16L8, 16R6, 16R4, 16H8		17		35		40	ns
t_{ER}	Input to Output Disable 16L8, 16R6, 16R4, 16H8		17		35		40	ns
t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4		12		25		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4		12		25		25	ns
t_{CO}	Clock to Output 16R8, 16R6, 16R4		12		25		25	ns
t_s	Input or Feedback Setup Time 16R8, 16R6, 16R4	MIL $R_1 = 390$ $R_2 = 750$	15	30		35		ns
t_H	Hold Time 16R8, 16R6, 16R4		−10	0		0		ns
t_P	Clock Period			55		60		ns
t_W	Clock Width			20		25		ns
f_{MAX}	Maximum Frequency				18		16.5	MHz

Notes: 1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50pF$.
3. For three-state outputs, output enable times are tested with $C_L = 50pF$ to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5pF$. HIGH to high impedance tests are made to an output voltage of $V_{OH} - 0.5V$ with S_1 open; LOW to high impedance tests are made to the $V_{OL} + 0.5V$ level with S_1 closed.

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING WAVEFORMS



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KEY TO SWITCHING WAVEFORM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

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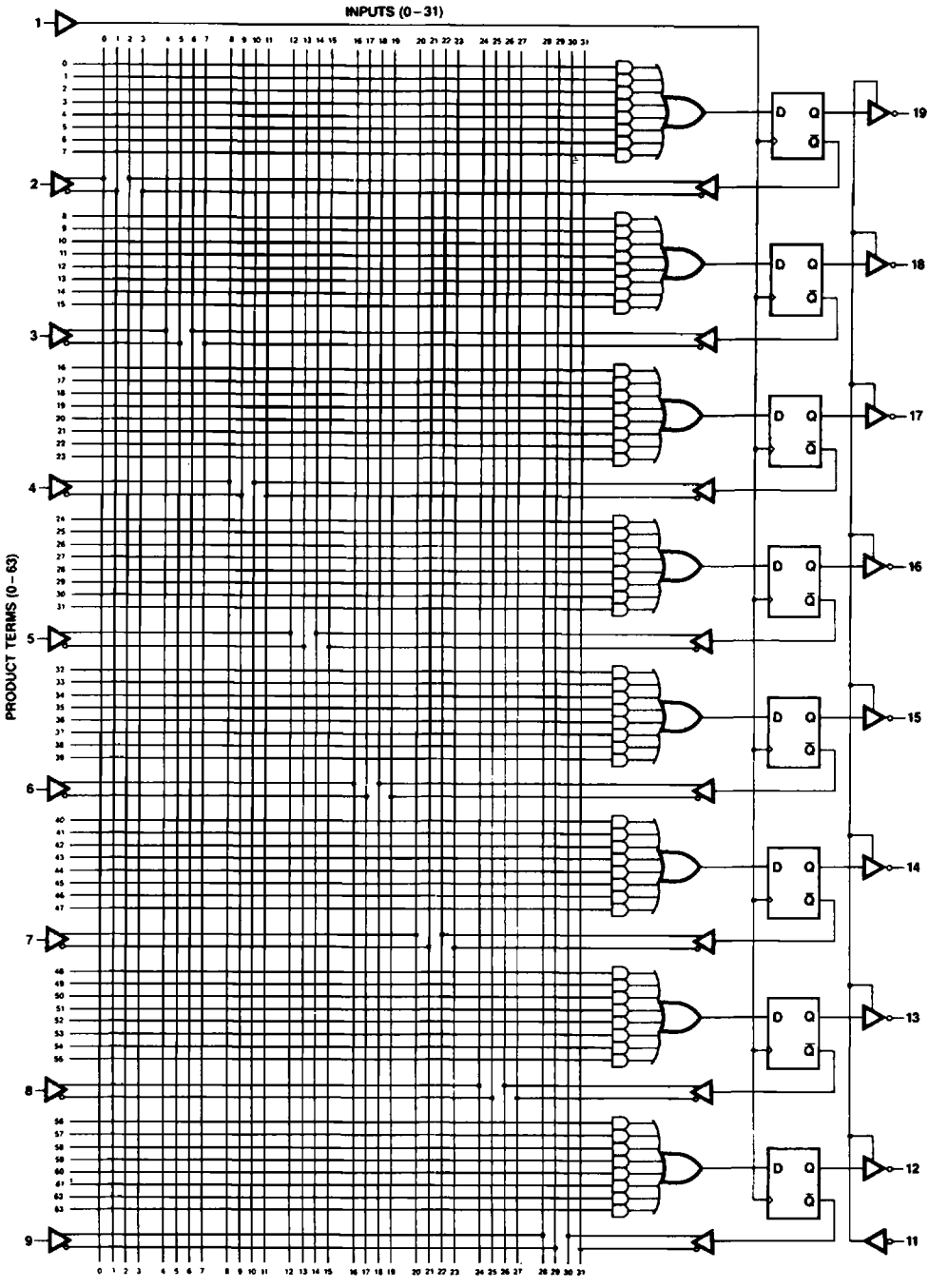
BLOCK DIAGRAM AmPAL16R8/AmPAL16R8A



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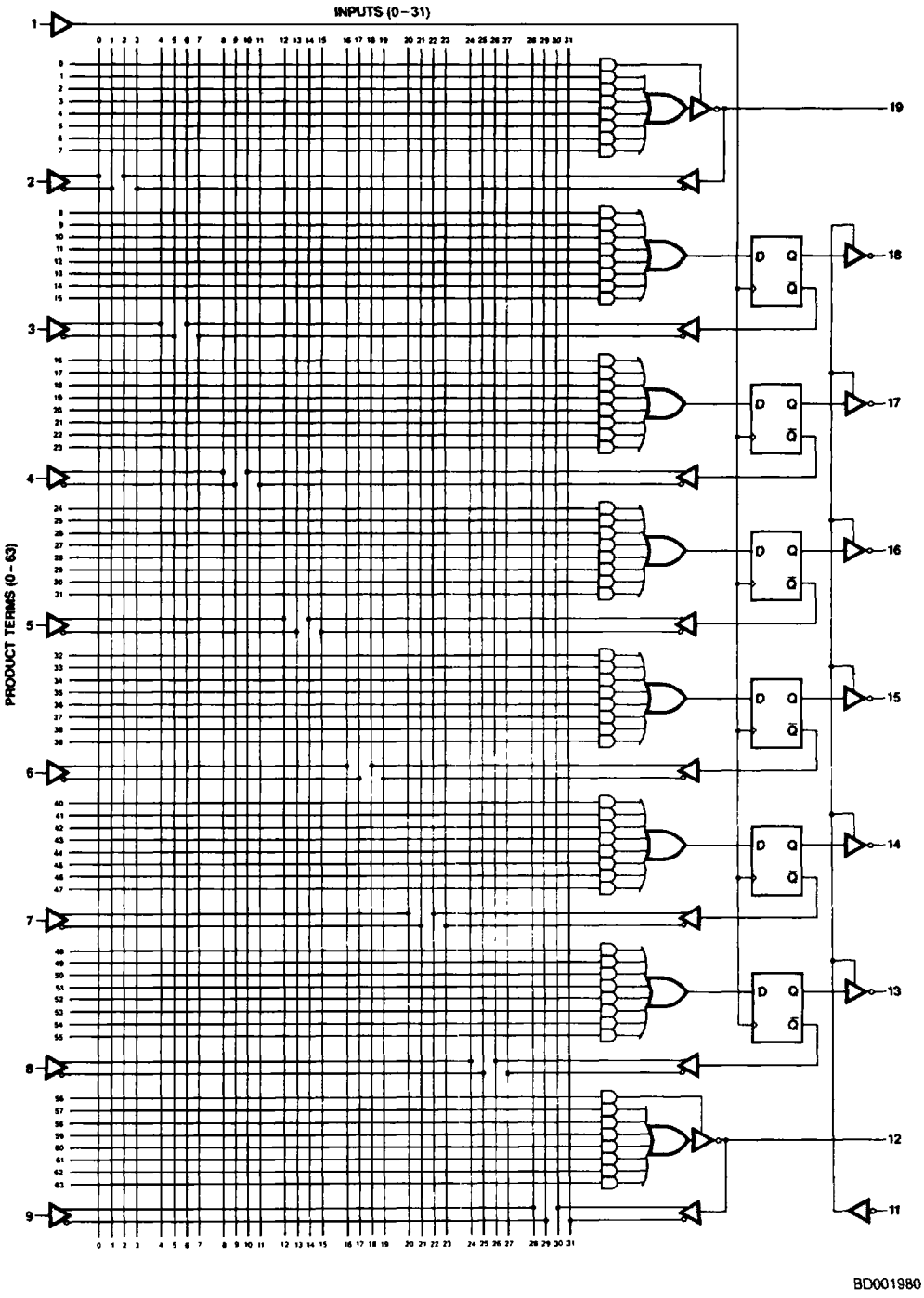
BLOCK DIAGRAM AmPAL16R6/AmPAL16R6A



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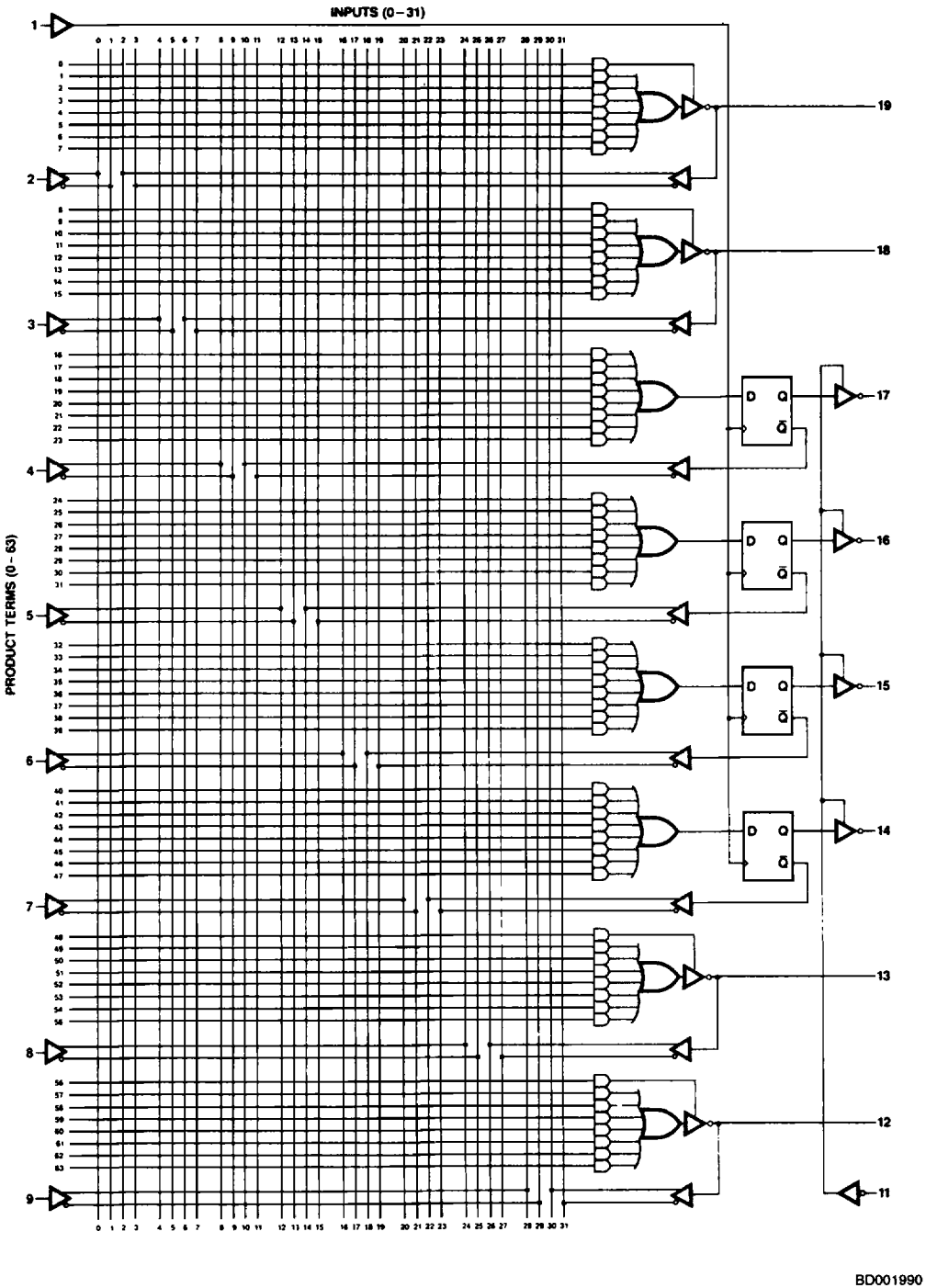
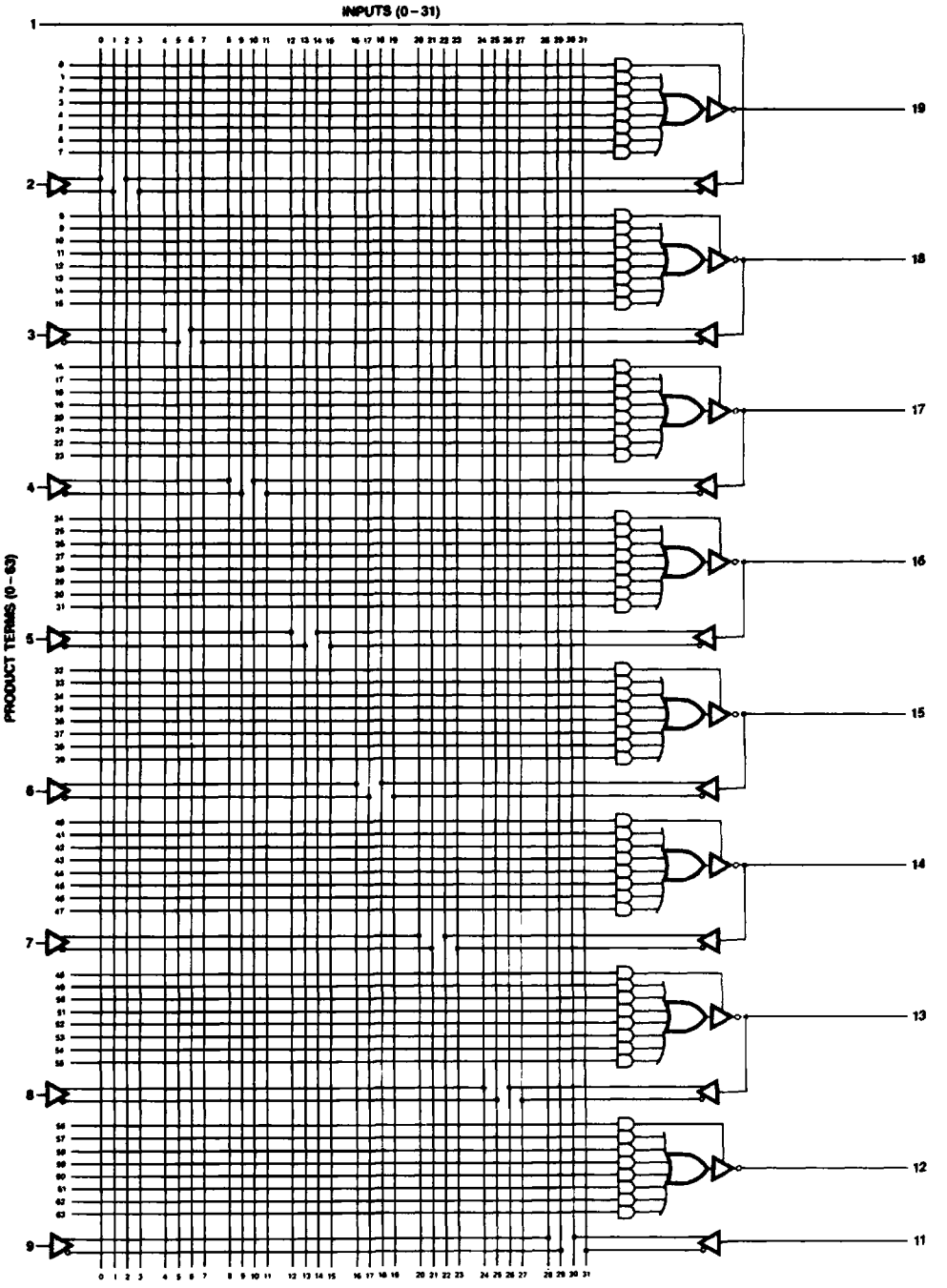
BLOCK DIAGRAM AmPAL16R4/AmPAL16R4A



BLOCK DIAGRAM AmPAL16L8/AmPAL16L8A



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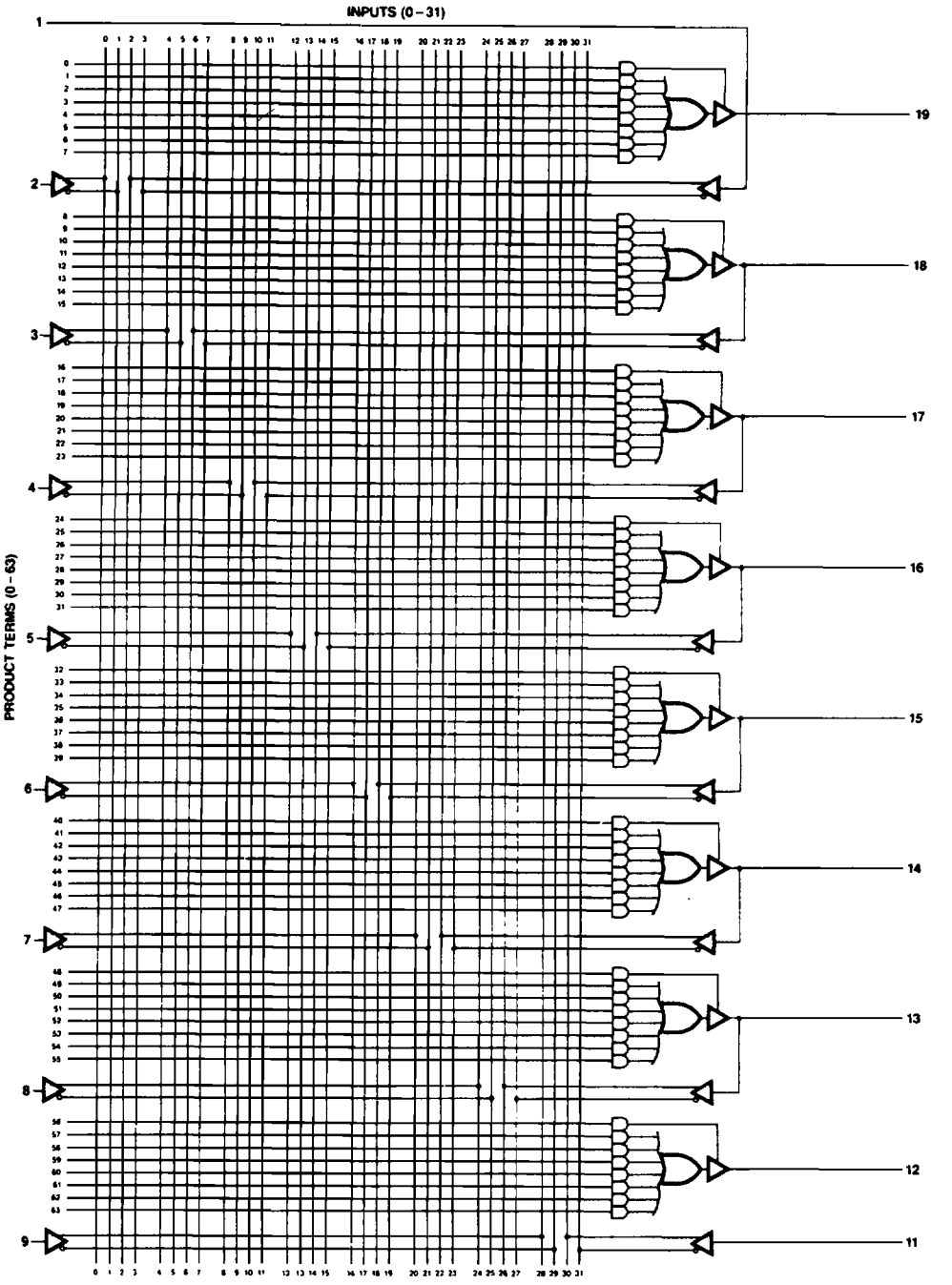
BLOCK DIAGRAM AmPAL16H8/AmPAL16H8A



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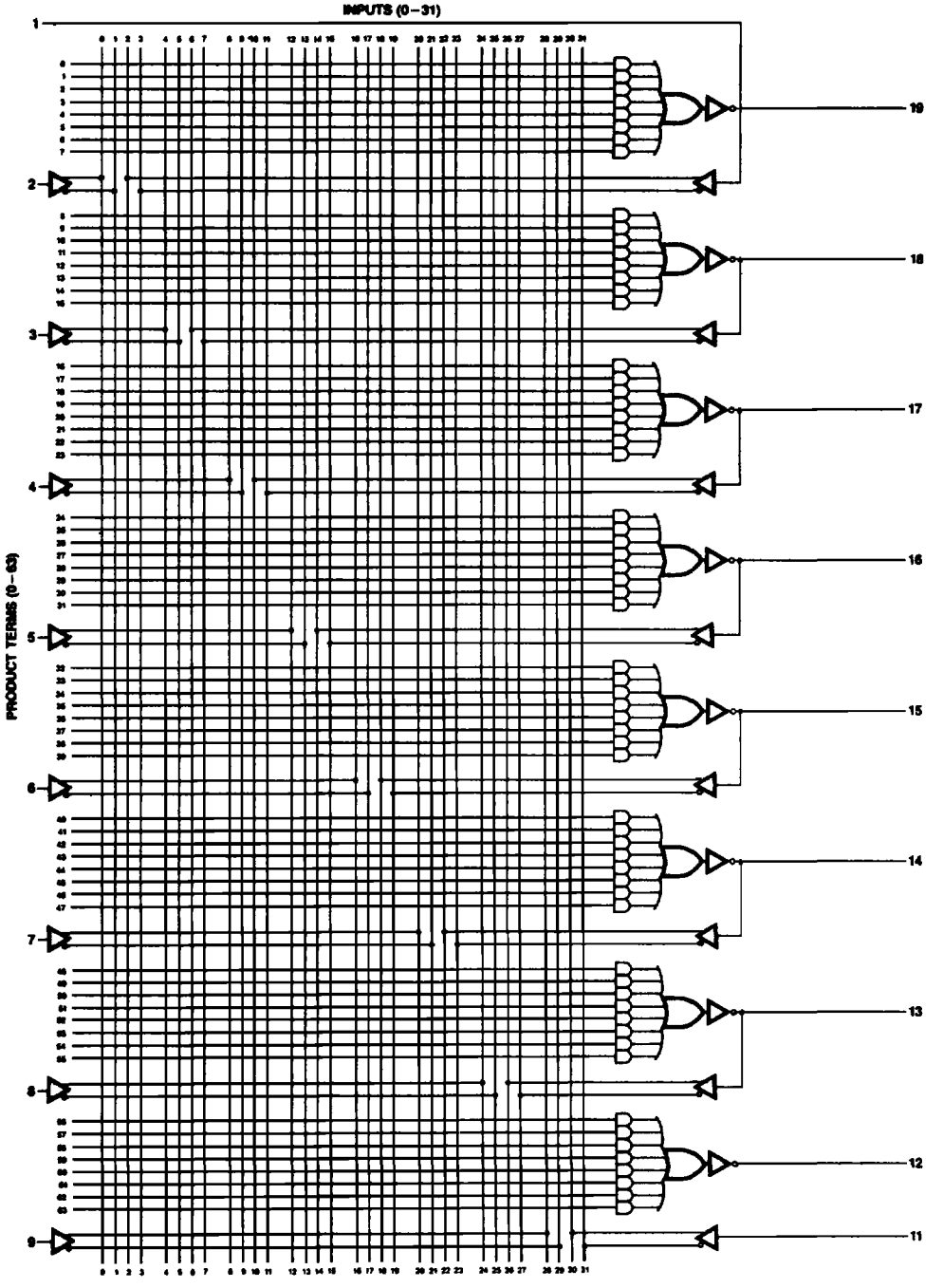
BLOCK DIAGRAM AmPAL16LD8/AmPAL16LD8A



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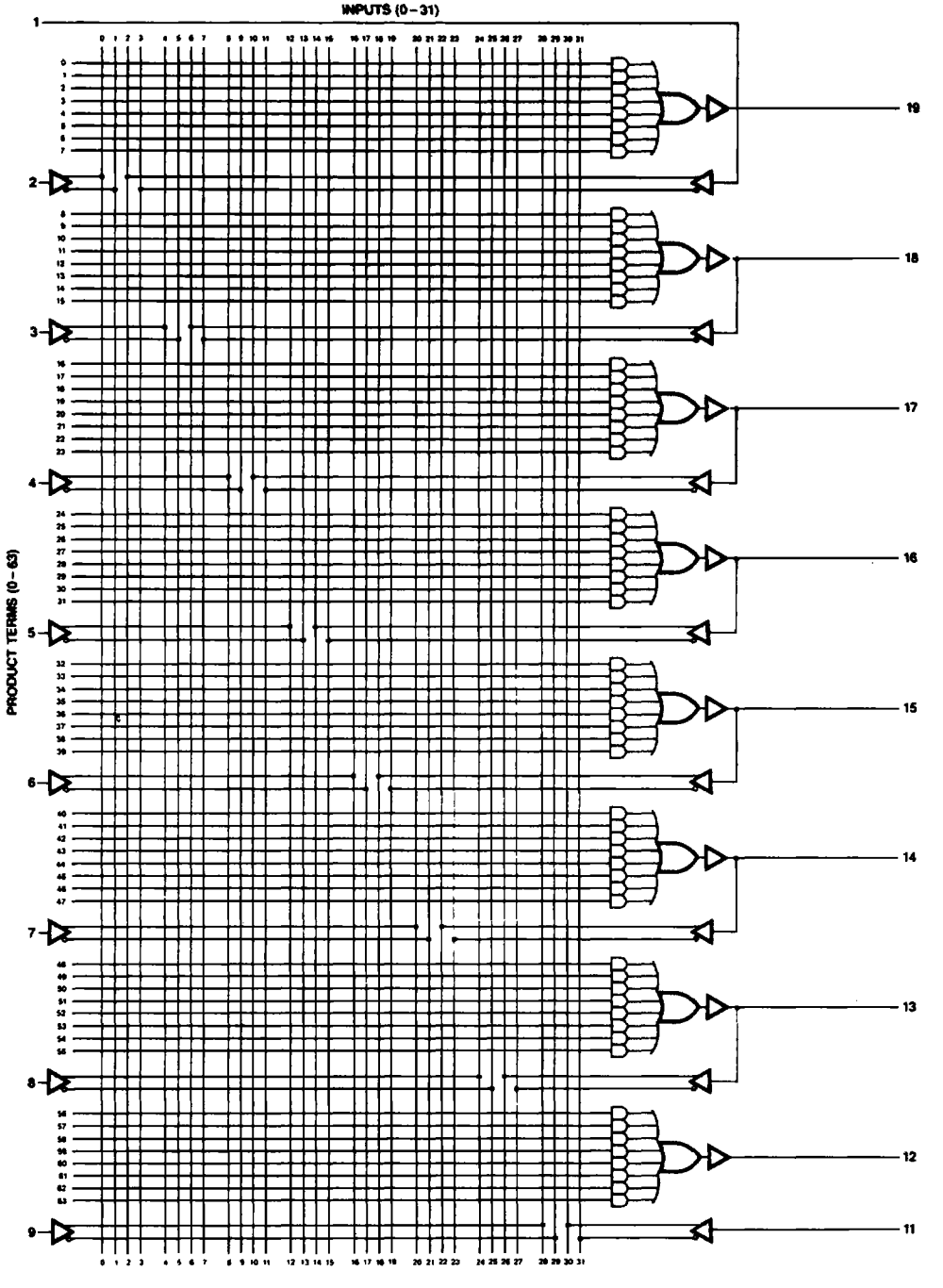
BLOCK DIAGRAM AmPAL16HD8/AmPAL16HD8A



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PROGRAMMING

Each AMD PAL fuse is programmed with a simple sequence of voltages applied to two control pins (1 and 11) and a programming voltage pulse applied to the output under programming. Addressing of the 2048 element fuse array is accomplished with normal TTL levels on eight input pins (five select the input line number and three select the product term number). V_{CC} is maintained at a normal level throughout the programming and verify cycle – no extra high levels are required.

The necessary sequence of levels for programming any fuse is shown in the Programming Timing Diagram. The address of each fuse in terms of Input Line Number and Product Term Line Number is defined by the Fuse Address Tables 1 and 2. Current, voltage and timing requirements for each pin are specified in the Programming Parameter Table below.

The 16L8, 16R8, 16R6, 16R4, 16H8, 16LD8 and 16HD8 use identical programming conditions and sequences.

After all programming has been completed, the entire array should be reverified at V_{CCL} and again at V_{CCH}. Reverification can be accomplished by reading all eight outputs in parallel rather than one at a time. The array fuse verification cycle checks that the correct array fuses have been blown and can be sensed by the outputs.

AMD PALs have been designed with many internal test features that are used to assure high programming yield and correct logical operation for a correctly programmed part.

An additional fuse is provided on each AMD PAL circuit to prevent unauthorized copying of AMD PAL fuse patterns when design security is desired. Blowing the security fuse blocks entry to the fuse pattern verify mode.

To blow the security fuse:

1. Power up part to V_{CCP}
2. Raise Pin 5 to V_{HH}.
3. Pulse Pin 11 from ground to V_{OP} for a 50μsec duration.
4. Perform a normal end-of-programming verify cycle at V_{CCL} and V_{CCH}. All fuse locations should be sensed as blown if the security fuse has been successfully blown.

Note that parts with the security fuse blown may not be returned as programming rejects.

AMD PALs normally have high programming yields (> 98%). Programming yield losses are frequently due to poor socket contact, equipment out of calibration or improperly used.

PROGRAMMING PARAMETERS T_A = 25°C

Parameters	Description		Min	Typ	Max	Units
V_{HH}	Control Pin Extra High Level	Pin 1 @ 10-40mA	10	11	12	Volts
		Pin 11 @ 10-40mA	10	11	12	
V_{OP}	Program Voltage Pins 12-19 @ 15-200mA		18	20	22	Volts
V_{IHP}	Input High Level During Programming and Verify		2.4	5	5.5	Volts
V_{ILP}	Input Low Level During Programming and Verify		0.0	0.3	0.5	Volts
V_{CCP}	V_{CC} During Programming @ I_{CC} = 50-200mA		5	5.2	5.5	Volts
V_{CCL}	V_{CC} During First Pass Verification @ I_{CC} = 50-200mA		4.1	4.3	4.5	Volts
V_{CCH}	V_{CC} During Second Pass Verification @ I_{CC} = 50-200mA		5.4	5.7	6.0	Volts
V_{Blown}	Successful Blown Fuse Sense Level @ Output	16L8, 16R8, 16R6, 16R4, 16LD8 16L8A, 16R8A, 16R6A, 16R4A, 16LD8A		0.3	0.5	Volts
		16H8, 16HD8, 16H8A, 16HD6A	2.4	3		
dV_{OP}/dt	Rate of Output Voltage Change		20		250	V/μsec
dV_{11}/dt	Rate of Fusing Enable Voltage Change (Pin 11 Rising Edge)		100		1000	V/μsec
t_p	Fusing Time First Attempt		40	50	100	μsec
	Subsequent Attempts		4	5	10	msec
t_D	Delays Between Various Level Changes		100	200	1000	ns
t_V	Period During which Output is Sensed for V_{Blown} Level				500	ns
V_{ONP}	Pull-Up Voltage On Outputs Not Being Programmed		V_{CCP} – 0.3	V_{CCP}	V_{CCP} + 0.3	Volts
R	Pull-Up Resistor On Outputs Not Being Programmed		1.9	2	2.1	KΩ

AMD PAL PROGRAMMING EQUIPMENT INFORMATION

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Kontron Electronics, Inc. 630 Price Avenue Redwood City, CA 94063	Stag Microsystems 528-5 Weddel Drive Sunnyvale, CA 94086
Programmer Model(s)	Model-100, 29, 19 or 17	Model-MPP-80S or EPP80	Model-PPX
AMD PAL Personality Module	Logicpak 950-1942-001	MOD-33	PPM2200
Socket Adapter	715-1947-003	SA37	Am202S

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PROGRAMMING WAVEFORMS

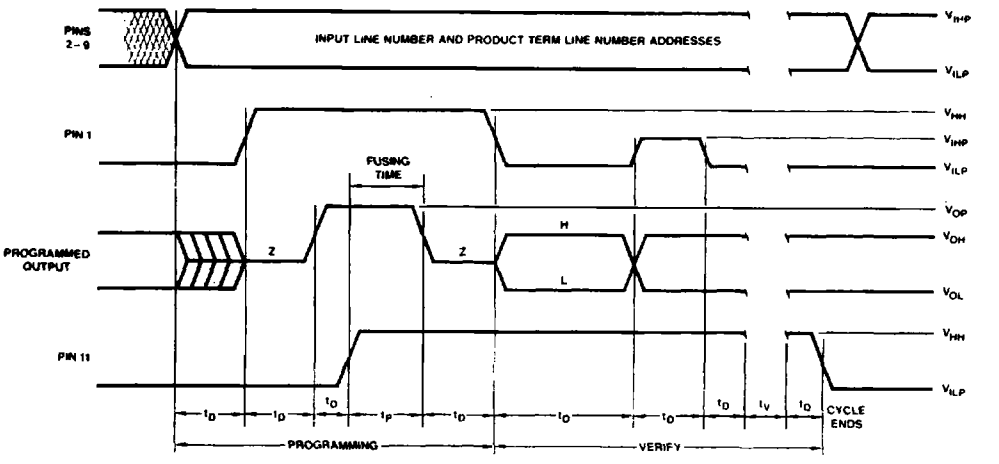

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TABLE 1. INPUT ADDRESSING

Input Line Number	Input Line Number Address Pin States				
	9	8	7	6	5
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	L	H	L	L	H
10	L	H	L	H	L
11	L	H	L	H	H
12	L	H	H	L	L
13	L	H	H	L	H
14	L	H	H	H	L
15	L	H	H	H	H
16	H	L	L	L	L
17	H	L	L	L	H
18	H	L	L	H	L
19	H	L	L	H	H
20	H	L	H	L	L
21	H	L	H	L	H
22	H	L	H	H	L
23	H	L	H	H	H
24	H	H	L	L	L
25	H	H	L	L	H
26	H	H	L	H	L
27	H	H	L	H	H
28	H	H	H	L	L
29	H	H	H	L	H
30	H	H	H	H	L
31	H	H	H	H	H

L = V_{ILP}
H = V_{IHP}

SIMPLIFIED PROGRAMMING DIAGRAM

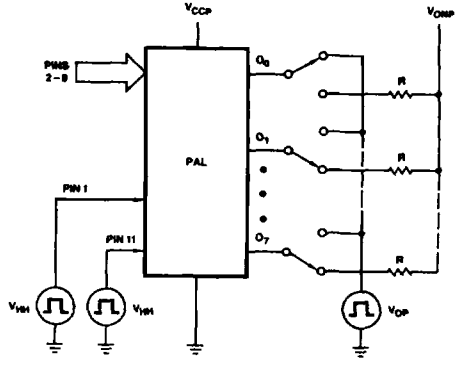

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TABLE 2. PRODUCT TERM ADDRESSING

Product Term Line Number								Product Term Select Address Pin		
								4	3	2
0	8	16	24	32	40	48	56	L	L	L
1	9	17	25	33	41	49	57	L	L	H
2	10	18	26	34	42	50	58	L	H	L
3	11	19	27	35	43	51	59	L	H	H
4	12	20	28	36	44	52	60	H	L	L
5	13	21	29	37	45	53	61	H	L	H
6	14	22	30	38	46	54	62	H	H	L
7	15	23	31	39	47	55	63	H	H	H
Pin 19	Pin 18	Pin 17	Pin 16	Pin 15	Pin 14	Pin 13	Pin 12			
Programming Access and Verify Pin										

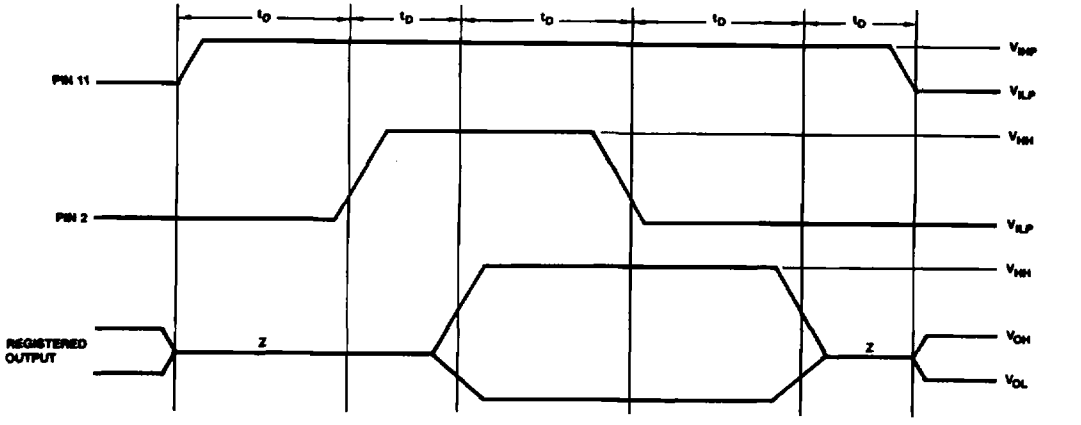
L = V_{ILP}
H = V_{IHP}

Refer to Page 13-1 for Essential Information on Military Devices

PRELOAD OF REGISTERED OUTPUTS

AMD PAL registered outputs are designed with extra circuitry to allow loading each register asynchronously to either a HIGH or LOW state. This feature simplifies testing since any initial state for the registers can be set to optimize test sequencing.

The pin levels and timing necessary to perform the PRELOAD function are detailed below:



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Level forced on registered output pin during preload cycle	Output state at the output pin after cycle
V_{HH}	HIGH
0 V to V_{CCH} or OPEN	LOW

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

AmPAL XXXXX X X X X

- Screening
  - C = 883C Basic Flow
  - B = 883B (Burn-in)
- Temperature Range
  - C = Commercial
  - M = Military
- Package
  - P = Molded DIP (Commercial Only)
  - D = Hermetic DIP
  - L = Chip-Pak™*
- Speed Selection
  - = Standard
  - A = High Speed
- Basic Device
  - 16R8
  - 16R6
  - 16R4
  - 16L8
  - 16H8
  - 16LD8
  - 16HD8

*Chip-Paks are rated a maxium case temperature only.

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