

54AC/74AC323 • 54ACT/74ACT323 .

8-Bit Universal Shift/Storage Register With Synchronous Reset and Common I/O Pins

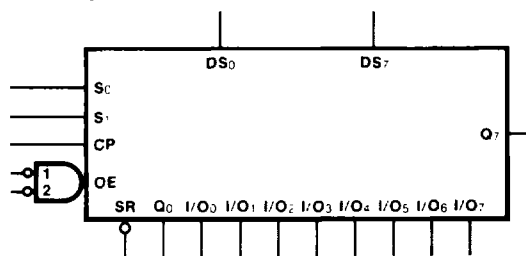
Description

The 'AC/'ACT323 is an 8-bit universal shift/storage register with 3-state outputs. Its function is similar to the 'AC/'ACT299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q₀ and Q₇ to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

- Common Parallel I/O for Reduced Pin Count
- Additional Serial Inputs and Outputs for Expansion
- Four Operating Modes: Shift Left, Shift Right, Load and Store
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24mA
- 'ACT323 has TTL-Compatible Inputs

Ordering Code: See Section 6

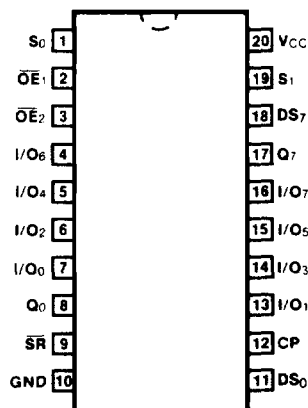
Logic Symbol



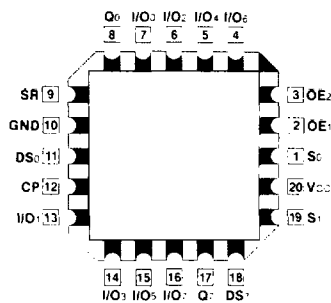
Pin Names

- | | |
|-------------------------------------|---|
| CP | Clock Pulse Input |
| DS ₀ | Serial Data Input for Right Shift |
| DS ₇ | Serial Data Input for Left Shift |
| S ₀ , S ₁ | Mode Select Inputs |
| SR | Synchronous Reset Input |
| OE ₁ , OE ₂ | 3-State Output Enable Inputs |
| I/O ₀ - I/O ₇ | Multiplexed Parallel Data Inputs or 3-State Parallel Data Outputs |
| Q ₀ , Q ₇ | Serial Outputs |

Connection Diagrams



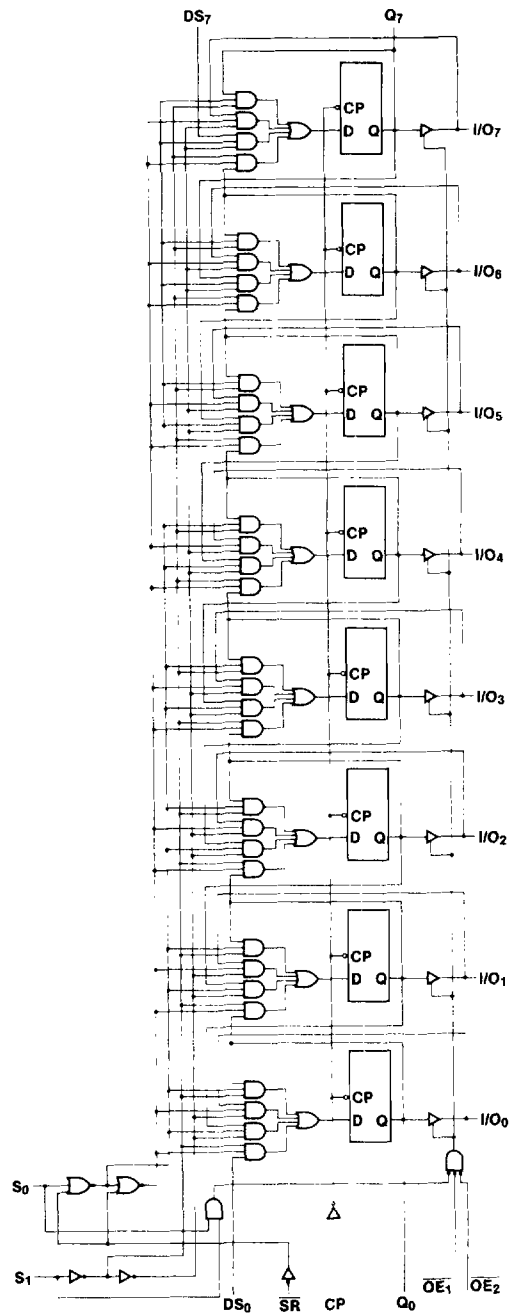
Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

AC323 • ACT323

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'AC/ACT323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S₀ and S₁ as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q₀ and Q₇ are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on \overline{SR} overrides the Select inputs and allows the flip-flops to be reset by the next

rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either \overline{OE}_1 or \overline{OE}_2 disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S₀ and S₁ in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
\overline{SR}	S ₁	S ₀	CP	
L	X	X	J	Synchronous Reset; Q ₀ -Q ₇ = LOW
H	H	H	J	Parallel Load; I/O _n → Q _n
H	L	H	J	Shift Right; DS ₀ → Q ₀ , Q ₀ → Q ₁ , etc.
H	H	L	J	Shift Left; DS ₇ → Q ₇ , Q ₇ → Q ₆ , etc.
H	L	L	X	Hold

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 J = LOW-to-HIGH Clock Transition

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DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I _{CC}	Maximum Quiescent Supply Current	160	80	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = Worst Case
I _{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = 25°C
I _{CC(T)}	Maximum Additional I _{CC} /Input ('ACT323)	1.6	1.5	mA	V _{IN} = V _{CC} - 2.1 V, V _{CC} = 5.5 V, T _A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC			54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Input Frequency	3.3 5.0	55 130							MHz	3-3
t _{PLH}	Propagation Delay CP to Q ₀ or Q ₇	3.3 5.0	31.0 12.0							ns	3-6
t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇	3.3 5.0	30.0 13.0							ns	3-6
t _{PLH}	Propagation Delay CP to I/O _n	3.3 5.0	28.0 11.0							ns	3-6
t _{PHL}	Propagation Delay CP to I/O _n	3.3 5.0	28.0 12.0							ns	3-6
t _{PZH}	Output Enable Time	3.3 5.0	24.0 10.0							ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0	24.0 10.0							ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0	25.0 13.0							ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0	24.0 12.0							ns	3-8

*Voltage Range 3.3 is 3.0 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC		54AC	74AC	Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF		
			Typ	Guaranteed Minimum				
ts	Setup Time, HIGH or LOW S0 or S1 to CP	3.3 5.0	12.0 5.0				ns	3-9
th	Hold Time, HIGH or LOW S0 or S1 to CP	3.3 5.0	0 0				ns	3-9
ts	Setup Time, HIGH or LOW I/O _n , DS ₀ , DS ₇ to CP	3.3 5.0	5.0 5.0				ns	3-9
th	Hold Time, HIGH or LOW I/O _n , DS ₀ , DS ₇ to CP	3.3 5.0	0 0				ns	3-9
ts	Setup Time, HIGH or LOW SR to CP	3.3 5.0	4.0 2.0				ns	3-9
th	Hold Time, HIGH or LOW SR to CP	3.3 5.0	0 0				ns	3-9
tw	CP Pulse Width HIGH or LOW	3.3 5.0	9.0 4.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Input Frequency	5.0	125							MHz	3-3
t _{PLH}	Propagation Delay CP to Q ₀ or Q ₇	5.0	12.0							ns	3-6
t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇	5.0	13.0							ns	3-6
t _{PLH}	Propagation Delay CP to I/O _n	5.0	10.0							ns	3-6
t _{PHL}	Propagation Delay CP to I/O _n	5.0	12.0							ns	3-6
t _{PZH}	Output Enable Time	5.0	10.0							ns	3-7
t _{PZL}	Output Enable Time	5.0	10.0							ns	3-8
t _{PHZ}	Output Disable Time	5.0	12.0							ns	3-7
t _{PLZ}	Output Disable Time	5.0	11.0							ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT		54ACT	74ACT	Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF		
			Typ	Guaranteed Minimum				
ts	Setup Time, HIGH or LOW S0 or S1 to CP	5.0	5.0				ns	3-9
th	Hold Time, HIGH or LOW S0 or S1 to CP	5.0	0				ns	3-9
ts	Setup Time, HIGH or LOW I/O _n , DS ₀ , DS ₇ to CP	5.0	3.0				ns	3-9
th	Hold Time, HIGH or LOW I/O _n , DS ₀ , DS ₇ to CP	5.0	0				ns	3-9
ts	Setup Time, HIGH or LOW SR to CP	5.0	2.0				ns	3-9
th	Hold Time, HIGH or LOW SR to CP	5.0	0				ns	3-9
tw	CP Pulse Width HIGH or LOW	5.0	4.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C _{IN}	Input Capacitance	4.5	pF	Vcc = 5.5 V
C _{PD}	Power Dissipation Capacitance		pF	Vcc = 5.5 V