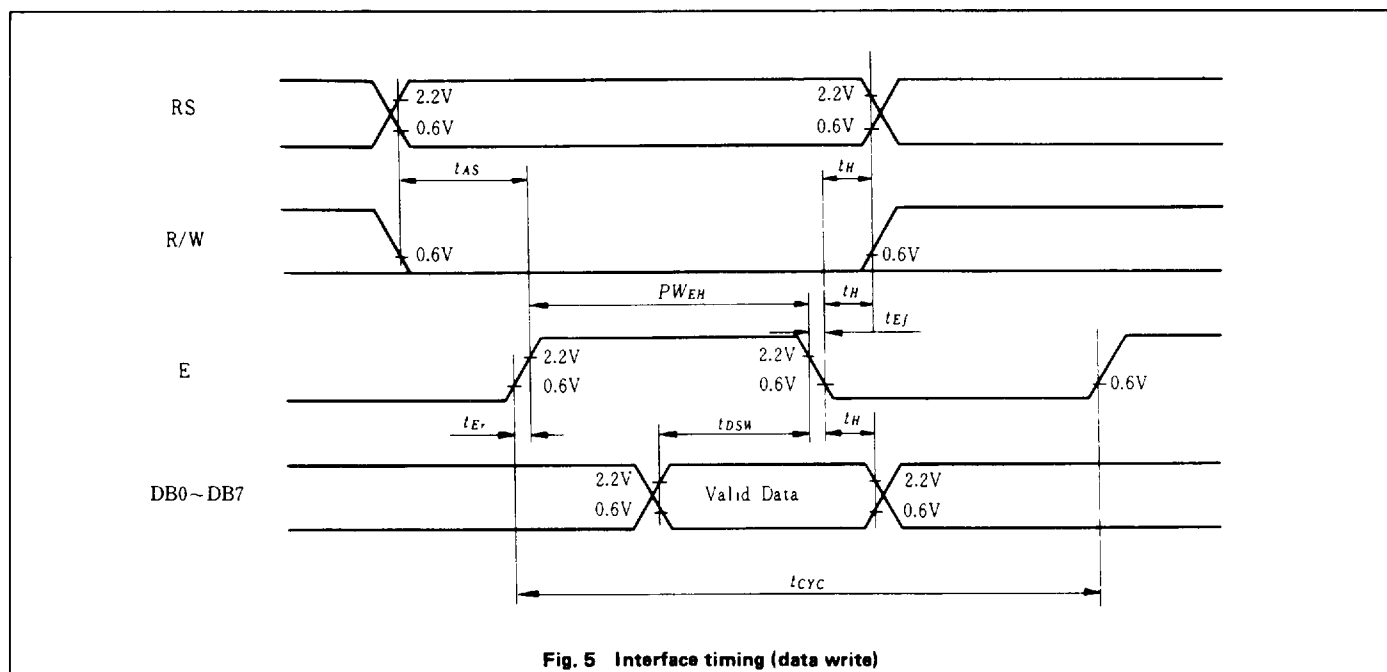
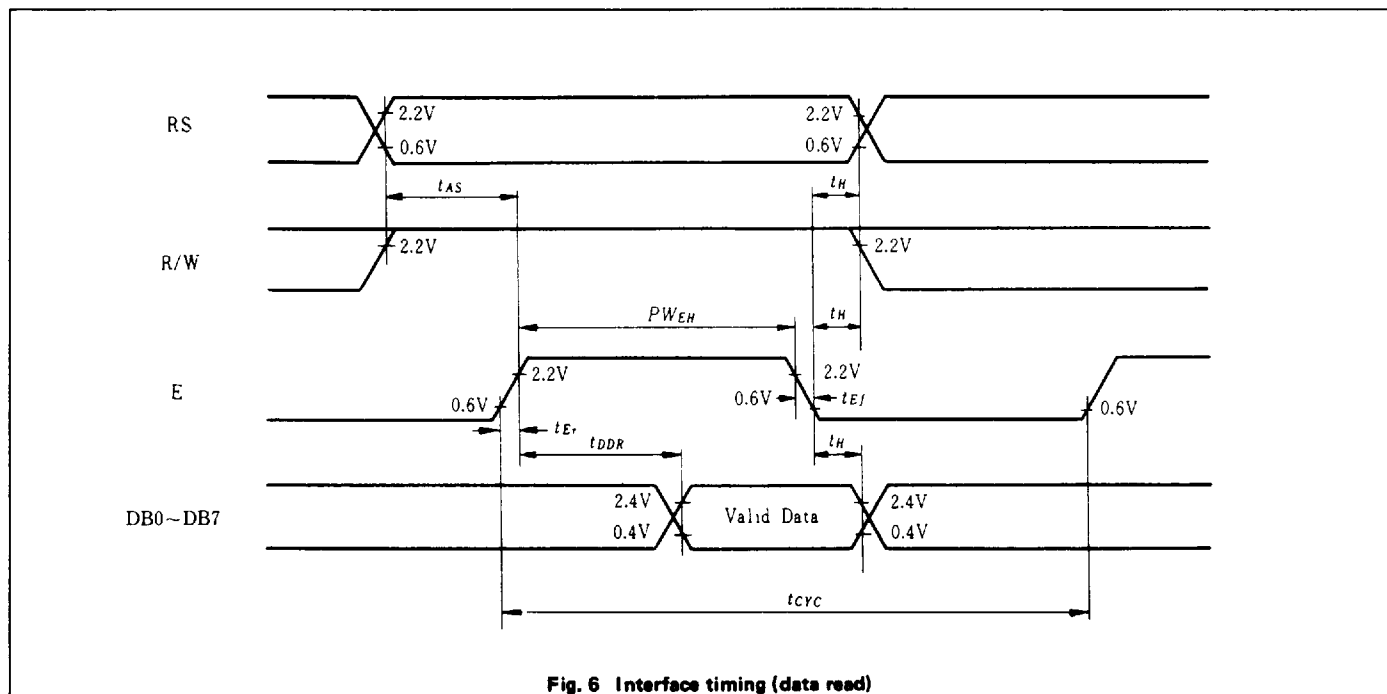


**TIMING CHARACTERISTICS**

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	$t_{cyc}$	Fig. 5, Fig. 6	1.0	—	—	$\mu s$
Enable pulse width	$PW_{EH}$	Fig. 5, Fig. 6	450	—	—	ns
Enable rise/fall time	$t_{Er}, t_{Ef}$	Fig. 5, Fig. 6	—	—	25	ns
RS, R/W set up time	$t_{AS}$	Fig. 5, Fig. 6	140	—	—	ns
Data delay time	$t_{DDR}$	Fig. 6	—	—	320	ns
Data set up time	$t_{DSW}$	Fig. 5	195	—	—	ns
Hold time	$t_H$	Fig. 5, Fig. 6	20	—	—	ns



**Fig. 5 Interface timing (data write)**



**Fig. 6 Interface timing (data read)**