

BIPOLAR ANALOG INTEGRATED CIRCUIT

μ PC844GR-9LG, 4744GR-9LG

SINGLE SUPPLY VOLTAGE, HIGH SPEED, WIDE BAND, DUAL OPERATIONAL AMPLIFIERS

DESCRIPTION

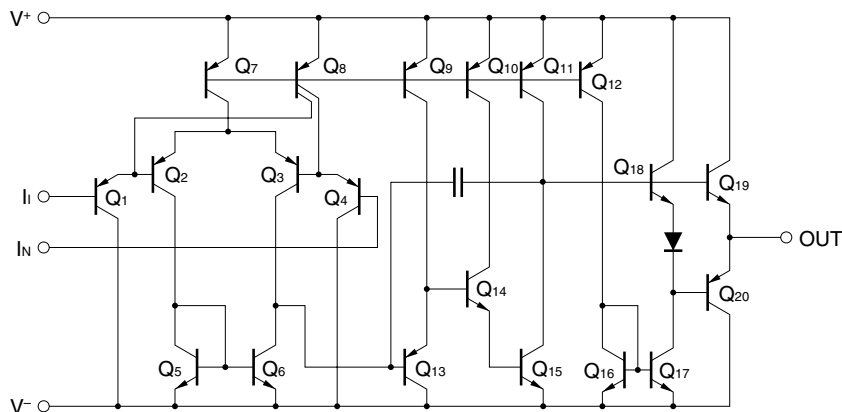
The μ PC844GR-9LG, 4744GR-9LG are quad high speed, wide band operational amplifiers designed for single supply operation from +3 V to +32 V with low supply current drain. By using high speed PNP transistors for input and output circuits, the excellent AC performance is achieved without degrading capacitive load drive capability.

With no crossover distortion and wide output voltage range characteristics, the μ PC844GR-9LG, 4744GR-9LG are optimum choice for single supply AC amplifier, and active filters.

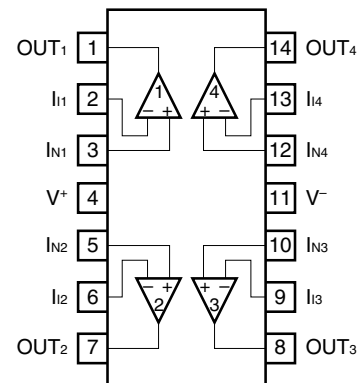
FEATURES

- High slew rate: 8.5 V/ μ s TYP. ($V^+ = +5$ V, $V^- = \text{GND}$)
- Wide gain band width product: 3.5 MHz TYP. ($V^+ = +5$ V, $V^- = \text{GND}$)
- Wide supply voltage range: +3 V to +32 V
- Wide output voltage swing
- Common mode input voltage range includes V^-
- Internal frequency compensation
- Output short circuit protection

EQUIVALENT CIRCUIT (1/4 Circuit)



PIN CONFIGURATION (Top View)



ORDERING INFORMATION

Part Number	Package
μ PC844GR-9LG-A	14-pin plastic TSSOP (5.72 mm (225))
μ PC4744GR-9LG-A	14-pin plastic TSSOP (5.72 mm (225))

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	μPC844GR-9LG	μPC4744GR-9LG	Unit
Voltage between V ⁺ and V ⁻ ^{Note 1}	V ⁺ - V ⁻	-0.3 to +36		V
Differential Input Voltage	V _{ID}	±36		V
Input Voltage ^{Note 2}	V _I	V ⁻ - 0.3 to V ⁻ + 36		V
Output Voltage ^{Note 3}	V _O	V ⁻ - 0.3 to V ⁺ + 0.3		V
Power Dissipation ^{Note 4}	P _T	550		mW
Output Short Circuit Duration ^{Note 5}		Indefinite		sec
Operating Ambient Temperature	T _A	-40 to +125	-40 to +85	°C
Storage Temperature	T _{stg}	-55 to +150	-55 to +125	°C

Notes 1. Reverse connection of supply voltage can cause destruction.

2. The input voltage should be allowed to input without damage or destruction independent of the magnitude of V⁺. Either input signal should not be allowed to go negative by more than 0.3 V. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

3. This specification is the voltage which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.

4. The thermal deleting factor of these IC are same value as -7.0 mW/°C, but the delete beginning temperature in different as follows.

$$\mu\text{PC844GR-9LG} : 71^{\circ}\text{C} \quad \mu\text{PC4744GR-9LG} : 46^{\circ}\text{C}$$

The calculated junction to ambient thermal resistance at above conditions is 144°C/W.

5. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage (Split)	V [±]	±1.5		±16	V
Supply Voltage (V ⁻ = GND)	V ⁺	+3		+32	V
Output Current	I _o			±10	mA
Capacitive Load (A _v = +1, R _f = 0 Ω)	C _L			1000	pF

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, V[±] = ±15 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V _{IO}			±1.0	±6.0	mV
Input Offset Current	I _{IO}			±6	±75	nA
Input Bias Current ^{Note 6}	I _B			140	500	nA
Large Signal Voltage Gain	A _V	R _L ≥ 2 kΩ, V _O = ±10 V	25000	300000		
Supply Current ^{Note 7}	I _{CC}	I _O = 0 A		7.5	11	mA
Common Mode Rejection Ratio	CMR		70	86		dB
Supply Voltage Rejection Ratio	SVR		70	93		dB
Output Voltage Swing	V _{OM}	R _L ≥ 10 kΩ	±13.7	+14 -14.3		V
Output Voltage Swing	V _{OM}	R _L ≥ 2 kΩ	±13.5			V
Common Mode Input Voltage Range	V _{ICM}		V ⁻		V ⁺ - 1.8	V
Slew Rate (Rise)	SR	A _V = 1, R _L ≥ 2 kΩ		8.5		V/μS
Gain Band Width Product	GBW	f _O = 100 kHz		3.5		MHz
Channel Separation		f = 20 Hz to 20 kHz		120		dB

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, V⁺ = 5 V, V⁻ = GND)

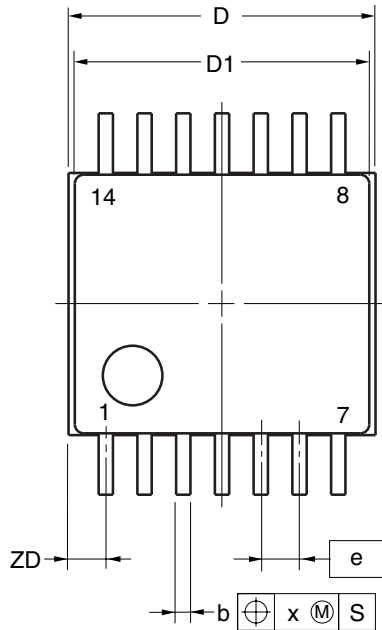
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V _{IO}			±1.0	±5	mV
Input Offset Current	I _{IO}			±6	±75	nA
Input Bias Current ^{Note 6}	I _B			160	500	nA
Large Signal Voltage Gain	A _V	R _L ≥ 2 kΩ	25000	300000		
Supply Current ^{Note 7}	I _{CC}	I _O = 0 A		6.0	9.0	mA
Common Mode Rejection Ratio	CMR		70	80		dB
Supply Voltage Rejection Ratio	SVR		70	95		dB
Output Voltage Swing	V _{OM}	R _L ≥ 2 kΩ (Connect to GND)	3.7 0	4.0 0		V
Common Mode Input Voltage Range	V _{ICM}		0		V ⁺ - 1.8	V
Output Current (SOURCE)	I _{O SOURCE}	V ⁺ _{IN} = +1 V, V ⁻ _{IN} = 0 V	10	30		mA
Output Current (SINK)	I _{O SINK}	V ⁺ _{IN} = 0 V, V ⁻ _{IN} = +1 V	10	30		mA
Slew Rate (Rise)	SR	A _V = 1, R _L ≥ 2 kΩ		8.5		V/μS

Notes 6. Input bias currents flow out from IC. Because each currents are base current of PNP-transistor on input stage.

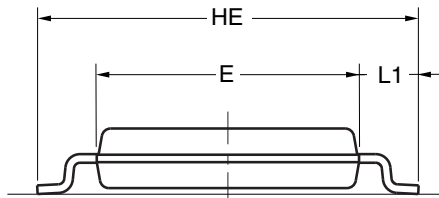
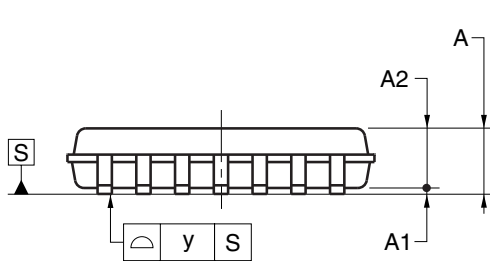
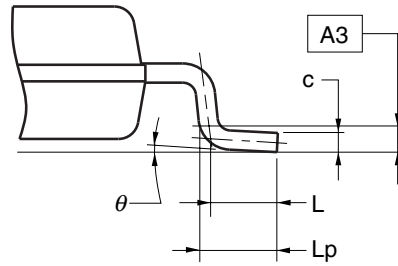
7. This current flows irrespective of the existence of use.

PACKAGE DRAWINGS

14-PIN PLASTIC TSSOP (5.72mm (225))



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	5.15±0.15
D1	5.00±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.20 MAX.
A1	0.10±0.05
A2	1.00±0.05
A3	0.25
b	0.24 ^{+0.06} _{-0.05}
c	0.145±0.055
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	3° ^{+5°} _{-3°}
e	0.65
x	0.10
y	0.10
ZD	0.625

P14GR-65-9LG

NOTE

Each lead centerline is located within 0.10mm of its true position at maximum material condition.

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RECOMMENDED SOLDERING CONDITIONS

The μPC844GR-9LG, 4744GR-9LG should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

Type of Surface Mount Device

Process	Conditions	Symbol
Infrared ray reflow	Peak temperature: 260 °C or below (Package surface temperature), Reflow time: 60 seconds or less (at 220 °C or higher), Maximum number of reflow processes: 3 time.	IR60-00-3
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120 °C or below (Package surface temperature).	WS60-00-1
Partial heating method	Pin temperature: 350 °C or below, Heat time: 3 seconds or less (Per each side of the device).	P350

Caution Apply only one kind of soldering condition to a device, except for “partial heating method”, or the device will be damaged by heat stress.

REFERENCE DOCUMENTS

Document Name	Document No.
QUALITY GRADES ON NEC SEMICONDUCTOR DEVICES	C11531E
SEMICONDUCTOR DEVICE MOUNT MANUAL	http://www.necel.com/pkg/en/mount/index.html
NEC SEMICONDUCTOR DEVICE RELIABILITY/QUALITY CONTROL SYSTEM - STANDARD LINEAR IC	IEI-1212

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