August 1993
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FUJITSU

DATA SHEET

MB818255-70/-80

2097,152 Bits (262,144 x 8 Bits) Multi-port CMOS Dynamic RAM

The Fujitsu MB818255 is a fully decoded dual port CMOS Dynamic RAM (DRAM) 256K words by 8 bits random access parallel port and 512 words by 8 bits Static RAM (SRAM) serial access memory (SAM) port. The MB818255 is ideally suited for mainframes, video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Multiplexed row and column address inputs permit the MB818255 to be housed in 400mil wide 40-pin SOJ, 475mil height 40-pin Shrink ZIP and 400mil wide 44-pin TSOP. Pinouts conform to the JEDEC approved pinout. The MB818255 features a **write per bit** operation whereby the user can inhibit writing to particular bits and a **split transfer operation** whereby the user can design serial access timing easily and programmable stop operation suitable for tile mapping. The MB818255 has **hyper page mode** current data output is latcheded until next CAS falling edge.

Parameter		MB818255-70	MB818255-80
DRAM Access Time		70ns max.	80ns max.
SAM Access Time		20ns max.	25ns max.
DRAM Cycle Time		125ns min.	140ns min
SAM Cycle Time		20ns min.	25ns min.
Power Dissipation	DRAM: Active SAM: Standby	605mW max.	550mW max.
	DRAM: Standby SAM: Active	440mW max.	358mW max.
	DRAM: Standby SAM: Standby	16.5mW max.	

- Same pinout as MB818251 with enhanced (••) features
- 2MB Dynamic Random Access Memory (DRAM)
  - 512 x 512 x 8 bit array (256K x 8 bit)
  - multiplexed Selective write per bit mask input through RAM port I/O pins
  - 512 refresh cycles every 8 msec.
  - Automatic CAS-before-RAS refresh
  - Flash Write (same bit, entire row) function
  - •• Hyper Page mode (Latched RAM port data output)
- 4KB Independent serial access memory (SAM)
  - 512 x 8 bit Static Random Access Memory (SRAM) array
  - Split option: read from 128 x 8 half, write to other
  - Addressable Start sequential I/O function
  - Boundary sequential wrap-around
  - •• Programmable Stop sequential I/O function
- Bidirectional synchronous transfers between DRAM and SRAM array
  - One DRAM row (512 x 8) to/from SAM start address
  - Split option: Read from 128 x 8 half, write to other
  - Standard JEDEC pinout

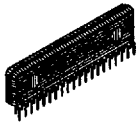
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	VIN, VOUT	−1 to +7	V
Voltage of Vcc supply relative to VSS	VCC	−1 to +7	V
Power Dissipation	PD	2.0	W
Short circuit Output Current	IOUT	50	mA
Storage Temperature	TSTG	−55 to +125	°C

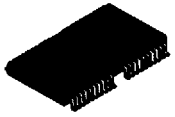
NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY

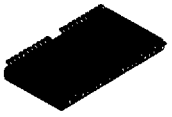
Plastic SOJ
(LCC–40P–M01)



Plastic ZIP
(ZIP–40P–M02)



Plastic TSOP
(normal bend leads)
(FPT–44P–M07)



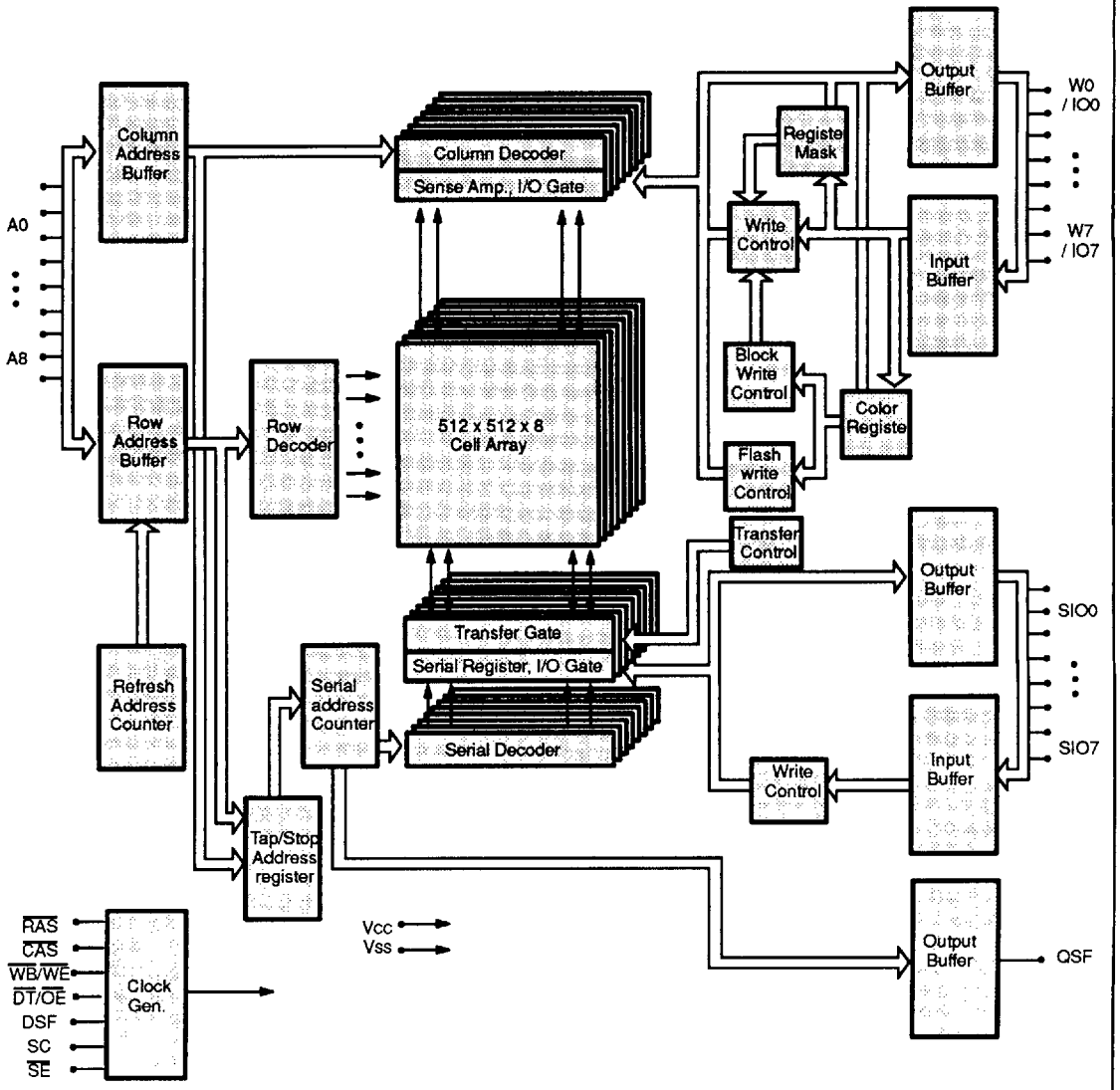
Plastic TSOP
(reverse bend leads)
(FPT–44P–M08)

Package and Ordering Information

- 40-pin plastic (400 mil) SOJ, order as MB818255-xxPJ
- 40-pin plastic (475 mil H) S-ZIP, order as MB818255-xxPZS
- 44-pin plastic (400 mil) TSOP with normal bend leads, order as MB818255-xxPFTN
- 44-pin plastic (400 mil) TSOP with reverse bend leads, order as MB818255-xxPFTR

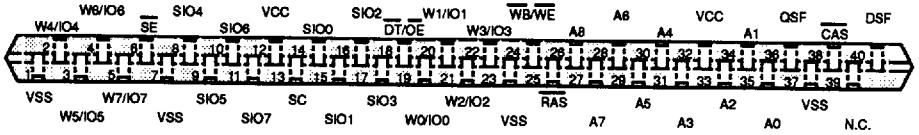
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB818255 Multi-port DYNAMIC RAM – BLOCK DIAGRAM

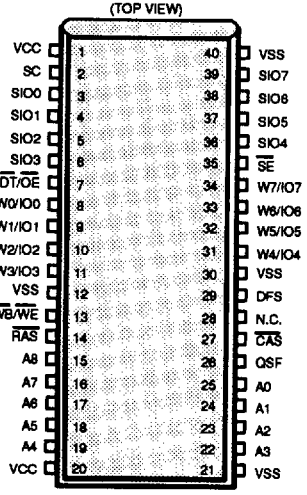


PIN ASSIGNMENTS AND DESCRIPTIONS

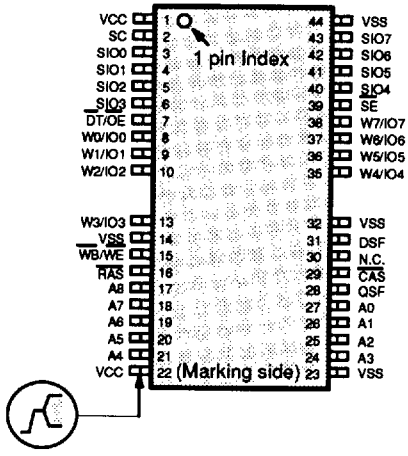
40-Pin ZIP:
(TOP VIEW)



40-Pin SOJ:
(TOP VIEW)



44-Pin FPT:
(TOP VIEW)
<Normal Bend : FPT-44P-M07>



Pin Number SOJ	Symbol	Parameter	Mode
25, 24, 23, 22 19, 18, 17, 16, 15	A0 to A8	Address inputs.	Input
14	$\overline{RAS}$	Row address strobe.	Input
27	$\overline{CAS}$	Column address strobe.	Input
2	SC	Serial Access Memory Strobe	Input
7	$\overline{DT/OE}$	Data transfer/Output Enable	Input
13	$\overline{WB/WE}$	Write-Per-Bit / Write Enable	Input
8, 9, 10, 11 31, 32, 33, 34	W0/IO0 to W7/IO7	Write-Per-Bit Data / Random Data Input/Output	I/O
29	DSF	Special Function	Input
35	$\overline{SE}$	Serial Port Enable	Input
3, 4, 5, 6 36, 37, 38, 39	SIO0 to SIO7	Serial Data Input/Output	I/O
26	QSF	Special flag	Output
1, 20	VCC	Supply Voltage +5V	–
40, 30, 21, 12	VSS	Circuit ground.	–
28	N.C.	No connection.	–

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DESCRIPTION

This description covers the three operations of the MB818255: DRAM Operation, Serial Access Operation, and Transfer Operation.

DRAM OPERATION

$\overline{RAS}$:
This pin is used to strobe the nine row address inputs (A0 to A8) with its low-going transition and to provide the timing that determines the first function ($\overline{DT}$, $\overline{WB}$,W0 to W7) of the dual-function pins ($\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, W0/IO0 to W7/IO7). A certain time after this timing, these pins play the role of their second function ($\overline{OE}$, $\overline{WE}$, IO0 to IO7). When $\overline{RAS}$ is high, the DRAM is placed in a standby state, resulting in greatly reduced power consumption.

$\overline{CAS}$:
This pin is used to strobe the nine column address inputs (A0 to A8) with its low-going transition. Since MB818255 has extended fast page mode, it can not control the output impedance of the DRAM port (IO0 to IO7).

$\overline{WB}/\overline{WE}$:
This pin functions as $\overline{WB}$ (mask mode enable) at the low-going transition of $\overline{RAS}$, and as $\overline{WE}$ (write enable) after that transition. If WB is low at the falling edge of $\overline{RAS}$, write-per-bit mode is enabled. In this case, particular bits can be inhibited from write as specified by W0 to W7 in case of new mask mode. If $\overline{WB}$ is high, normal read/write mode is entered. The DRAM port is set for the read or write mode by $\overline{WE}$. Read mode is selected when $\overline{WE}$ is high; write mode is selected when $\overline{WE}$ is low. No data can be input during read mode. Even when $\overline{OE}$ is low, if $\overline{WE}$ goes low before $\overline{CAS}$ does, the data input/output pins are placed in a write cycle executable state (high-impedance state).

$\overline{DT}/\overline{OE}$:
This pin functions as data transfer ($\overline{DT}$) enable at the falling edge of $\overline{RAS}$ and then as output enable ($\overline{OE}$). $\overline{DT}$ = "L" at the falling edge of $\overline{RAS}$ enables data transfer between DRAM and SAM; $\overline{DT}$ = "H" enables DRAM operation that is independent of the serial port. In this mode, $\overline{OE}$ may be used to control the output impedance of the DRAM port.

DSF :
This pin functions as a special function input pin at the falling edges of $\overline{RAS}$ and $\overline{CAS}$. When DSF = "H" at the falling edge of RAS, it enables flash write or split read/write transfer or register read/load operation, depending on the input conditions of $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$. When DSF = "L" at the falling edge of $\overline{RAS}$ and DSF = "H" at the falling edge of $\overline{CAS}$, it enables block write operation. For normal read/write or transfer operation, DSF should be set "L" at the falling edge of $\overline{RAS}$.

Address Inputs (A0 to A8) :
The MB818255 requires a total of 18 binary inputs to select the desired cell from its 262,144 x 8 storage cells. First, 9-bit row addresses are set to address input pins A0-A8 and the row address strobe ($\overline{RAS}$) is pulled low, causing the row address information to be latched into the internal circuit. Then, 9-bit column addresses are added to address input pins A0-A8 and the column address strobe ($\overline{CAS}$) is pulled low, causing the column address information to be internally latched. All address inputs must be valid before $\overline{RAS}$ goes low. $\overline{CAS}$ is internally controlled (gated) by the $\overline{RAS}$ signal, so that $\overline{CAS}$ can be input immediately after the designated row address hold time (tRAH).

W0/IO0 to W7/IO7 :
These pins function as mask data (W0 to W7) at the low-going transition of $\overline{RAS}$ and then as data input/output pins (IO0 to IO7). During Write-Per-Bit mode for new mask, write operation is enabled for any of the W0-W7 pins that are high at the falling edge of $\overline{RAS}$, and is disabled and the internal data retained for pins which are low. When old mask mode, writes to memory cells cab be inhibited by data of mask register.

Data Inputs (IO0 to IO7) :
Information on the data input pins is written to the internal logic of the MB818255 only when the device is set to the write or read/write cycle. The data input register is strobed by the falling edge of $\overline{WE}$ or $\overline{CAS}$ whichever occurs later. If $\overline{WE}$ goes low (write mode) before $\overline{CAS}$ falls in a write cycle, for example, the data input is strobed by $\overline{CAS}$ and the setup and hold times are regulated from the low-going transition of $\overline{CAS}$. Conversely, if WE goes low after the fall of $\overline{CAS}$, as in the case of a read- write cycle, the data input is strobed by the falling edge of $\overline{WE}$ and the setup and hold times are regulated from the low-going transition of $\overline{WE}$. In the read-write or read-modify-write cycle, the output buffer must be placed in a high-impedance state (by forcing $\overline{OE}$ high) before adding data to the input/output lines.

Data Outputs (IO0 to IO7) :

The MB818255 output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data output has the same polarity as data input. Outputs are kept in high-impedance state until both $\overline{CAS}$ and $\overline{OE}$ go low. In the read cycle, the output becomes valid after timing requirements tRAC, tAA, tCAC, and tOEA are met. In the early write cycle, outputs are always in a high-impedance state. In the read-write and read-modify-write cycles, the output operates in the same way as in the read cycle.

Output Control :

Since the output control of MB818255 is featured by the function of extended fast page mode, it should be performed according to the signals presented on $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and $\overline{OE}$ pins. (1) Both $\overline{RAS}$ and $\overline{CAS}$ are high level. (2) $\overline{WE}$ is low level. (3) $\overline{OE}$ is high level. If either of (1), (2), and (3), the output level becomes high-impeadance state. In order to keep output level, all conditions should be filled that either $\overline{RAS}$ or $\overline{CAS}$ is low level, $\overline{WE}$ is high level and $\overline{OE}$ is low level.

Read Cycle :

Read operation begins when both $\overline{RAS}$ and $\overline{CAS}$ are set low. When $\overline{RAS}$ goes low, the row address information is internally latched, and is followed by the falling edge of $\overline{CAS}$. However, $\overline{WE}$ must be returned high before $\overline{CAS}$ can be asserted. ($\overline{WE}$ must be held high until either $\overline{RAS}$ or $\overline{CAS}$ goes high.) The column address information is internally latched when goes low. The output information on IO pins is retained until both $\overline{RAS}$ = "H" and $\overline{CAS}$ = "H", or $\overline{OE}$ = "H".

Note : Because the access time is determined by one of the timing parameters tRAC, tCAC, tAA, or tOEA, $\overline{CAS}$ **must** be set low within tRCD (max.) and, at the same time, the column address **must** be valid within tRAD

Write Cycle :

The write cycle begins with the low-going transition of $\overline{WE}$, after setting both of RAS and $\overline{CAS}$ ow. When $\overline{RAS}$ goes low, the row address information is internally latched. When the setup and hold time requirements relative to $\overline{CAS}$ are met, $\overline{WE}$ initiates an early write cycle operation with outputs placed in the high-impedance state. In the delayed write or read- modify-write cycle, $\overline{WE}$ goes low after $\overline{CAS}$. When $\overline{CAS}$ goes low, the column address information is internally latched. When a write operation beings, the input data is latched into the internal logic by the falling edge of $\overline{CAS}$ or $\overline{WE}$ whichever occurs last.

For all write operations to be executed without failure, the timing requirements of tRAL, tCAL, tRWL, and tCWL must be met.

Read-modify-write Cycle :

The read-modify-write cycles hold $\overline{WE}$ high when $\overline{CAS}$ goes low to complete the read cycle and then forces $\overline{WE}$ low to initiate a write operation within the same cycle. In this cycle, the new data is correctly written back to the read address, provided that the input delay time from $\overline{OE}$ and the setup and hold time requirements relative to $\overline{WE}$ are met.

Hyper Page Mode Read Cycle :

The hyper page-mode read cycle can be initiated after the normal read or write cycle is completed. In this mode, the read operation is controlled by $\overline{CAS}$, with $\overline{RAS}$ kept low and $\overline{WE}$ held high. The column address information is latched on the falling edge of $\overline{CAS}$, and valid data is output to the IO pins. Column address latch is disabled by the rising edge of $\overline{CAS}$. Any of the 512 x 8 bits data sent to the sense amp can be read at random by changing the column addresses. Hyper page-mode, data output level is latched untill replaced by falling $\overline{CAS}$.

Note : Since refresh operation in the hyper page-mode read cycle is not supported, the refresh time requirement **must** be met and the RAS timing **must** be fully considered to be in a normal read mode.

Hyper Page Mode Write Cycle :

The hyper page-mode write cycle can be initiated after the normal read or write cycle is completed. In this mode, the write operation is controlled by $\overline{CAS}$, after pulling $\overline{WE}$ low while $\overline{RAS}$ is kept low. The column address information is latched on the falling edge of $\overline{CAS}$ and valid data is input from the IO pins. When a write operation begins, the input data is internally latched by the falling edge of $\overline{CAS}$ or $\overline{WE}$ whichever occurs last. (When executing $\overline{CAS}$-controlled write operation, $\overline{WE}$ can be fixed low during consecutive hyper page-mode write cycles.) Data can be written to any of the 512 x 8 bit cells sent to the sense amp at random by changing the column addresses.

Note : Since refresh operation in the hyper page-mode write cycle is not supported, the refresh time requirement **must** be met and the RAS timing **must** be fully considered to be in a normal write mode.

Hyper Page Mode Read-modify-write Cycle :

The read-modify-write operation can be executed the same way in the hyper page-mode cycle as in the normal cycle: set WE low after valid data is output by a hyper page-mode read operation.

Note : The three modes of operation described above – read, write, and read-modify-write cycles – can be used in any desired combination in the hyper page mode as in normal mode.

Refresh Cycle :

Since the MB818255 uses dynamic memory cells, it requires that memory contents at each of the 512 bits (A0 to A8) of row addresses be refreshed every 8.2 ms (maximum). The following describes how memory cells are refreshed.

For example, when access is made on a row address by the execution of a read, write, or a read-modify-write cycle within the designated refresh time, the cells connected to the row of the selected cell are automatically refreshed (512 x 8 cells, including the selected cell in the read mode; the selected cell contains IO information in the write mode).

The refresh cycle described above is the simplest mode of all cycles. Information in the 512 x 8 cells connected to one row are amplified by a sense amp and rewritten into the cells. All cells of 262,144 x 8 bits are refreshed by repeating this refresh operation 512 times. There are three refresh modes used by the MB818255.

1. **$\overline{\text{RAS}}$ -only Refresh**
   In this mode, all cells are refreshed by strobing $\overline{\text{RAS}}$ for each of the 512 bits (A0 to A8) of externally given row addresses. Since $\overline{\text{CAS}}$ is held high till rising edge of $\overline{\text{RAS}}$ (disabled) in the RAS -only refresh mode, outputs are in a high-impedance state during this refresh cycle.

2. **$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh**
   The MB818255 supports a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh mode which does not require external refresh addresses. In this refresh mode, the refresh control circuit on the chip is activated when $\overline{\text{CAS}}$ goes low before $\overline{\text{RAS}}$ is forced low with its setup time (tCSR) satisfied and when refreshes are executed using the internal refresh address counter. In this refresh mode, therefore, external refresh address circuits can be eliminated.

   When a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh operation is executed, the internal refresh address counter is automatically incremented for the next $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle.

   $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle of MB818255 has also the function of stop address set up (refer to programmable stop) and of old mask mode set up. There are three modes in detail:

   2–1 **$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh (Stop Address Set)**
   This cycle switches a new mask mode onto an old mask mode as setting up stop address. Setting up the stop address depends on address signals (A0 to A8) in the falling edge of $\overline{\text{RAS}}$ as the following table. The stop address which has been set up is not valid till the first split transfer will execute.

Level of address in the falling edge of RAS by $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle									Stop address to be set (Decimal)
A8	A7	A6	A5	A4	A3	A2	A1	A0	
X	1	1	1	1	1	1	1	1	255, 511 (Default)
X	0	1	1	1	1	1	1	1	127, 255, 383, 511
X	0	0	1	1	1	1	1	1	63, 127, 191, 255, 319, 383, 447, 511
X	0	0	0	1	1	1	1	1	31, 63, 95, 127, 159, 191, 223, 255, ... , 511
X	0	0	0	0	1	1	1	1	15, 31, 47, 63, 79, ..., 511

2–2 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh (Option Reset)
This cycle switches an old mask mode onto a new mask mode as resetting stop address to 255 and 511.

2–3 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh (Option No-Reset)
This cycle can retain the previous state in the stop register and setting up of a new/old mask mode by the refresh operation only.

3. Hidden Refresh
Since output data is changed only on falling $\overline{\text{CAS}}$, the hidden refresh mode makes it possible to refresh other addresses. This refresh mode also eliminates the need for external refresh address circuits because an internal refresh address counter is used as in $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh mode.

When a hidden refresh is executed, $\overline{\text{CAS}}$ must be pulled high with the designated timing (tCRP) before a read, write, a read-modify-write cycle, or a page mode cycle can be executed.

Write-per-bit Mode:

This mode has a function which enable data to be written only to the IO pin which is designated in the writing operation at RAM portion. Two modes are featured by means of the write-per-bit function in MB818255. These are "New mask mode" and "Old mask mode". The former designates writing IO by each writing cycle, and the later sets up a write IO in Mask register in advance whose content controls writing.

Write cycle by New Mask Mode
Write-per-bit mode is designated by $\overline{\text{WB/WE}}$ in falling edge of RAS. When $\overline{\text{WB/WE}}$ = "L", at the falling edge of $\overline{\text{RAS}}$ each IO is designated writing by W0 to W7. When Wi = "L", the write operation is inhibited. The old mask mode is changed into the new mask mode by the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh (option reset) cycle or by the old mask mode reset cycle.

Write cycle by Old Mask Mode
It is necessary in advance to set writing IO in mask register by load mask register cycle. When IO = "L", the write operation is inhibited. After setting mask register, as well as new mask mode, $\overline{\text{WB/WE}}$ which are falling edge of $\overline{\text{RAS}}$ become write-per-bit mode under the condition "L" level, the content of mask register, write control is executed. After execution of load mask register cycle, it becomes old mask mode and keeps the previous state till $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh (option reset) cycle or mask mode reset cycle are executed.

Flash Write Cycle:

In this cycle, data is collectively written to one row of memory cells (512 x 8 bits) specified by the row address. The contents of data thus written is determined by the color register data. If the i'th bit (i = 0 to 7) is "H", for example, then "H" is written to all cells of the partial row (512 bits) that corresponds to IOi. Furthermore, the write-per-bit function is enabled by the input level of W0-W7 at the low-going transition of $\overline{\text{RAS}}$, making it possible to control an executing or inhibiting flash write operation. If Wj (j = 0 to 7) is "L" at the falling edge of $\overline{\text{RAS}}$, for example, then a write to the partial row that corresponds to IOj is disabled.

The color register data can be written into all DRAM cells by repeating this flash write cycle 512 times, providing a convenient way to clear the display screen.

Block Write Cycle :

The block write operation is entered when DSF is high, at the low-going transition of $\overline{CAS}$ during a normal write cycle. In a block write cycle, data is collectively written to a selected block of four contiguous columns (4x8 bits) within the row specified by the row address. Column addresses A0 and A1 at the falling edge of $\overline{CAS}$ are ignored.

The contents of data thus written is determined by the color register data. If the i'th bit (i=0 to 7) is "H", for example, then "H" is written to all cells in the selected block that corresponds to IOi.

The write-per-bit function is also enabled the same as it is in a normal write cycle. Similarly, selection or non-selection within a selected block (4 bits) can be controlled by the input level of IO0-IO3 at the falling edge of $\overline{CAS}$ or $\overline{WE}$ whichever occurs last. If IOi (i=0 to 3) is high, for example, the function is selected (data written). If IOi is low, the function is not selected (not written) and the previous data is retained. IO0 corresponds to column addresses in the block A0 ="L", A1 ="L". Similarly, IO1 corresponds to A0 ="H", A1="L"; IO2 corresponds to A0 ="L", A1 ="H"; and IO3 corresponds to A0 ="H", A1 ="H". Data IO4-IO7 are ignored.

The block write operation can be used in combination with a hyper page-mode cycle.

Load Register / Register Read cycle :

This cycle reads and writes data to and from the color registers and mask register. The color register data is used as write data during flash write or block write cycles. And the mask register data is used as the mask data during old mask mode. The selection of the color register and the mask register depends on the state of DSF pin in the falling edge of $\overline{CAS}$. When DSF = "H", the color register is selected and when DSF = "L", the mask register is selected.

Note : Cells corresponding to the row address at the low-going transition of $\overline{RAS}$ are refreshed simultaneously with read/write operations to the color registers in this cycle.

4

SERIAL ACCESS OPERATION

The MB818255 incorporates 512 words by 8 bits of serial access memory (SAM) that corresponds to its 256K words by 8 bits of memory cell array. This SAM architecture enables data read/write operations at high speed.

Although data is input and output via common I/O pins (SIO0 to SIO7), read/write control is applied during transfer mode. That is, the port is set for output after a read transfer cycle (DRAM to SAM transfer), thus providing output data onto the bus. After a write transfer cycle (SAM to DRAM transfer), the port is set for input which allows data to be written through the SIO0 to SIO7 pins. Serial port operation is controlled by $\overline{SE}$ (serial port enable) which controls the output impedance in output mode; it controls write operation in input mode. Serial port operation can be performed asynchronously with the DRAM port.

Serial Access Memory (SAM) Refresh :

Since serial access memory (SAM) is configured with static memory cells, it does not require periodical refreshes.

SC :

This is a serial port control clock, with serial access initiated by its rising edge. In the input mode, data on SIO0 to SIO7 is latched by the rising edge of SC and written into serial memory. In the output mode, output is obtained tSCA, after the rising edge of the clock. This output remains valid until new output is obtained by the next SC clock. When the SC clock is input in succession, memory is accessed at sequentially incremented addresses. If the SC clock is input after the last address of serial memory (#511) is reached, the access address returns to the first address (#0)

$\overline{SE}$:

This pin is used to control the serial port input/output. In the output mode, it functions as an output enable signal, controlling the output impedance. In the input mode, it functions as a write control pin with write operation enabled when $\overline{SE}$ is low and disabled when $\overline{SE}$ is high. Although input and output are both disabled when $\overline{SE}$ is high, accessed addresses are sequentially incremented by one as long as SC is input.

SIO0 to SIO7 :

These pins are used for input and output to and from serial memory (SAM). They are switched for input or output using a transfer cycle. Once set, the input or output mode is maintained until the next transfer cycle is executed. To write data to SAM via SIO0 to SIO7, execute a write transfer cycle. The pins are set for input, and data is written from SIO0 to SIO7 into SAM on the rising edge of the SC clock. To read data from SAM, execute a read transfer cycle. The pins are set for output, and data is read from SAM via SIO0 to SIO7 synchronously with the SC clock.

QSF :
This pin is used for output. In a split SAM mode, the state of QSF shows which SAM has the pointer, upper or lower. The following chart shows the relationship between accessing SAM, QSF output, and the SAM to be transferred by split transfer.

Accessing SAM	QSF Output	SAM To Be Transferred by Split Transfer
Lower SAM (0–255)	L	Upper SAM (256–511)
Upper SAM (256–511)	H	Lower SAM (0–255)

The QSF output goes from "L" to "H" by accessing the last address (255) in lower SAM. The QSF goes from "H" to "L" by accessing the last address (511) in upper SAM.

TRANSFER OPERATION

The MB818255 allows 512 words x 8 bits of data to be transferred between its one row of memory cell array and SAM, collectively, in one transfer cycle. Transfer is controlled by $\overline{DT}/\overline{OE}$. The direction of transfer is determined by the status of $\overline{WB}/\overline{WE}$ at the low-going transition of RAS. If WB is high, for example, data is transferred from DRAM to SAM (read transfer). If $\overline{WB}$ is low, data is transferred from SAM to DRAM (write transfer). The serial port is simultaneously set for input or output in the transfer cycle. A split transfer capability is available, allowing you to design serial access timing easily.

$\overline{DT}/\overline{OE}$:
The status of this pin at the low-going transition of $\overline{RAS}$ determines if a cycle is a transfer cycle. If $\overline{DT}$ is low, the cycle is a transfer cycle. If DT is high, the cycle is a DRAM/SAM independent operation cycle, i.e., it is not a transfer cycle.

$\overline{WB}/\overline{WE}$:
In a transfer cycle, this pin determines the direction of transfer. If $\overline{WB}$ is high at the low-going transition of $\overline{RAS}$, data can be transferred from a selected row of DRAM to SAM. If $\overline{WB}$ is low at the low-going transition of $\overline{RAS}$, data can be transferred from SAM to a selected row of DRAM.

Memory Refresh During Transfer Mode :
During a transfer mode, DRAM is refreshed as follows:
During a read transfer, data in a selected row address of DRAM is refreshed.
During a write transfer, new data is written from SAM to a selected row address of DRAM. This row address must be refreshed within 8.2 ms.

Address Input :
During a transfer cycle, address (A0 to A8) is input two times, one time at the falling edge of $\overline{RAS}$ and one time at the falling edge of $\overline{CAS}$. The address (A0 to A8), input at the fall of $\overline{RAS}$, specifies a row address (to which data is to be transferred) among the 512 rows of the memory cell array. The address (A0 to A8), input at the low-going transition of $\overline{CAS}$, specifies the first address of serial memory to be accessed after the completion of the transfer. After a read transfer, the data (transferred from DRAM to SAM by SC clock input) is serially output from one address after another beginning with the one specified by this address. After a write transfer, the input data is serially written to one address after another beginning with the one specified by this address.

Real-time Read Transfer :
Transfer in a read transfer operation is executed at the high-going transition of $\overline{DT}/\overline{OE}$ within this cycle. For SC clock input before this timing, the contents of SAM (before the transfer) are output. For the SC clock input after this timing, the new contents of SAM (after the read transfer) are output. By applying consecutive SC clocks during a read transfer, the SAM outputs before and after the read transfer can be obtained in succession. In this case, the SC clock must only be synchronized to the rising edge of $\overline{DT}/\overline{OE}$.

Write Transfer :
A write transfer cycle (SAM to DRAM) is executed in write-per-bit mode, depending on the input level of W0/IO0 to W7/IO7 at the low-going transition of $\overline{RAS}$. If Wj (j = 0 to 7) at the fall of $\overline{RAS}$ is "L", for example, a write transfer from SAM to DRAM for IOj is disabled. If the status of all W0 to W7 at the fall of $\overline{RAS}$ is "L", no data is transferred from SAM to DRAM and only SIO0 to SIO7 are switched for input.

Split Transfer :

The split transfer allows bidirectional data transfer of SAM that has organizations of 256-word x 8-bit each. When the upper SAM locations (256 to 511) are accessed (QSF pin out put "H" level.), the contents of lower SAM (0 to 256) are transferred to RAM. When the lower SAM locations (0 to 256) are accessed (QSF pin output "L" level.), the contents of upper SAM (256 to 511) are transferred to RAM. The SAM start address is determined by setting the address bits A0 to A7 and the state of QSF internally. When QSF = "H", A8 = "L"; and when QSF = "L", A8 = "H". Note that the "end address" and "end address – 1" of SAM, namely 254, 256, 510, 511, can not be set as the initial split-transfer address. Besides, the initial split-transfer address is not effective until the final address (255 or 511) of the currently accessed SAM is finished. The direction of data, transfer data bits, and switching of SIO are determined by the transfer mode as listed below. Note that in split transfer, SIO is not switched. This means that the input or output mode of the previous transfer cycle is maintained.

Transfer Mode	Direction of Data	Transfer Data Bit	Switching of SIO
Read Transfer	RAM → SAM	512 x 8	Input → Output
Write Transfer	SAM → RAM	512 x 8	Output → Intput
Split Read Transfer	RAM → SAM	256 x 8	———
Split Write Transfer	SAM → RAM	256 x 8	———

4

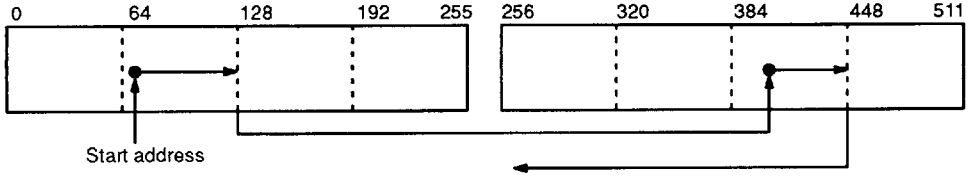
Programmable Stop :

This function is considered as the extention of the split transfer function. In the split trnsfer, the final address of the upper/lower SAM is fixed at the address 255 and 511. But programmable stop function enables to set five types of boundary final addresses, where are by every 16, 32, 64, 128, or 256 address by means of the binary boundary.

Stop address is set by $\overline{CAS}$-before-$\overline{RAS}$ refresh (stop register set), and after that, prpgrammable stop function is effective by the execution of split transfer cycle. And after boundary final address which is set by the clocking of the serial clock is accessed, SAM address jumped to a initial address, which is set by the split transfer before the access to the final address, in the oposite SAM, to upper SAM if final address in lower SAM and vice versa. These continuous operation enable one word data in RAM port to match with the rectangle display area on the screen. It is effective for the application of the tile mapping.

Programmable stop function can be cancelled by the execution mof $\overline{CAS}$-before-$\overline{RAS}$ refresh (option reset) cycle.

Example of Prpgrammable Stop Address



After boundary final address is accessed, SAM address jumped to initial address in the oposite SAM.

DESCRIPTION (Continued)

FUNCTIONAL TRUTH TABLE 1 (RAM READ/WRITE)

Falling edge of $\overline{RAS}$						Falling edge of $\overline{CAS}$			W0/IO0 to W7/IO7		Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DSF	A0 to A8	W0/IO0 to W7/IO7	$\overline{WB}/\overline{WE}$	DSF	A0 to A8	Input at $\overline{CAS}$ or $\overline{WE}$ falling edge	Output	
L	X	L	H	STOP	X	–	–	–	–	High-Z	CBR Refresh (Stop Register Set)
L	X	H	H	X	X	–	–	–	–	High-Z	CBR Refresh (Option Non-Reset)
L	X	X	L	X	X	–	–	–	–	High-Z	CBR Refresh (Option Reset)
H	H	X	L	Row	X	–	–	–	–	High-Z	$\overline{RAS}$ only Refresh
H	H → L	X	L	Row	X	H	X	Col.	High-Z	Low-Z	Read
H	H	H	L	Row	X	L	L	Col.	D-In	High-Z	Early Write (No Mask)
						H → L				Low-Z →High-Z	Delayed Write (No Mask)
H	H	L *1	L	Row	L *1	L	L	Col.	D-In	High-Z	Early Write (Mask)
					H *1						Early Write (No Mask)
H	H	L *1	L	Row	L *1	H → L	L	Col.	D-In	Low-Z →High-Z	Delayed Write (Mask)
					H *1						Delayed Write (No Mask)
H	H	H	L	Row	X	X	H	Col. *2 A2 to A8	L(Col) *3	High-Z	Block Write (Col.Mask)
									H(Col) *3		Block Write (Col.Select)
H	H	L *1	L	Row	L *1	X	H	Col. *2 A2 to A8	X	High-Z	Block Write (Mask)
					H *1				L(Col) *3		Block Write (Col.Mask)
									H(Col) *3		Block Write (Col.Select)
H	H	L	H	Row	L *1	X	X	X	X	High-Z	Flash Write (Mask)
					H *1						Flash Write (No Mask)

Note; H: High Level, L: Low Level, X: "H" or "L" Row: Row Add , Col: Col Add, (Col): Col. Select

*1. If $\overline{WB}/\overline{WE}$ is low at the falling edge of $\overline{RAS}$, a write, a block write, or a flash write operation can be disabled for particular I/O (bits) depending on the input level of Wi/IOi (write-per-bit function). When Wi/IOi is low, the corresponding bit is masked. When Wi/IOi is high, the bit is not masked.

*2. In block write mode, two bits of Col addresses A0 and A1 are ignored.

*3. In block write mode, a write operation can be disabled for specific columns within a selected block depending on the input level of W0/IO0–W3/IO3 at the falling edge of $\overline{CAS}$ or $\overline{WE}$ (Column Select function). When this input level is low, the corresponding column is masked. When this input level is high, the column is selected.

W0/IO0 corresponds to CA0 = "L", CA1 = "L".
W1/IO1 corresponds to CA0 = "H", CA1 = "L".
W2/IO2 corresponds to CA0 = "L", CA1 = "H".
W3/IO3 corresponds to CA0 = "H", CA1 = "H".
W4/IO4 to W7/IO7 are ignored.

4

DESCRIPTION (Continued)

FUNCTIONAL TRUTH TABLE 2 (RAM -SAM TRANSFER)

Falling edge of $\overline{RAS}$						$\overline{CAS}$	W0/IO0 to W7/IO7	SIO0 to SIO7		Function
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	DSF	A0 to A8	W0/IO0 to W7/IO7	A0 to A8	Output	Input	Output	
H	L	L *1	L	Row	L *1	TAP A0-8	High-Z	$\overline{SE}$ control	High-Z	Write transfer (MASK)
					H *1					Write transfer (NO MASK)
H	L	H	L	Row	X	TAP A0-8	High-Z	High-Z	$\overline{SE}$ control	Read transfer
H	L	L *1	H	Row	L *1	TAP *2 A0-7	High-Z	$\overline{SE}$ control	High-Z	Split Write transfer (MASK)
					H *1					Split Write transfer (NO MASK)
H	L	H	H	Row	X	TAP *2 A0-7	High-Z	High-Z	$\overline{SE}$ control	Split Read transfer

Note; H: High Level, L: Low Level, X: "H" or "L" Row: Row Add , TAP: TAP ADD. (SAM START ADD.)

*1. Write transfer is enabled when $\overline{WB/WE}$ is low at the falling edge of $\overline{RAS}$. In this case, the write transfer can be disabled for specific I/O (bits), depending on the input level of Wi/IOi at the low-going transition of $\overline{RAS}$ (write- per-bit function). When the input level is low, the write transfer is masked (data not transferred). When the input level is high, the operation is not masked (data transferred).

*2 In a split transfer, the initial SAM address A8 is internally set in the QSF state.

FUNCTIONAL TRUTH TABLE 3 (RAM LOAD REGISTER / REGISTER READ) *1

Falling edge of $\overline{RAS}$						Falling edge of $\overline{CAS}$			W0/IO0 to W7/IO7		Function
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	DSF	A0 to A8	W0/IO0 to W7/IO7	$\overline{WB/WE}$	DSF	A0 to A8	Input at $\overline{CAS}$ or $\overline{WE}$ falling edge	Output	
H	H	H	H	Row	X	L	H	X	Color D-IN	High-Z	Load color register early write
						H → L					Load color register delayed write
H	H	H	H	Row	X	H	H	X	High-Z	Low-Z	Color register read
H	H	H	H	Row	X	L	L	X	Mask D-IN	High-Z	Load mask register early write
						H → L					Load mask register delayed write
H	H	H	H	Row	X	H	L	X	High-Z	Low-Z	Mask register read

Note; H: High Level, L: Low Level, X: "H" or "L" Row: Row Add .

*1. The DRAM port is refreshed simultaneously with the load register/register read operation, according to the row address at the falling edge of $\overline{RAS}$.

Fig. 2 - EXAMPLE OF WRITE-PER-BIT OPERATION FOR NEW MASK

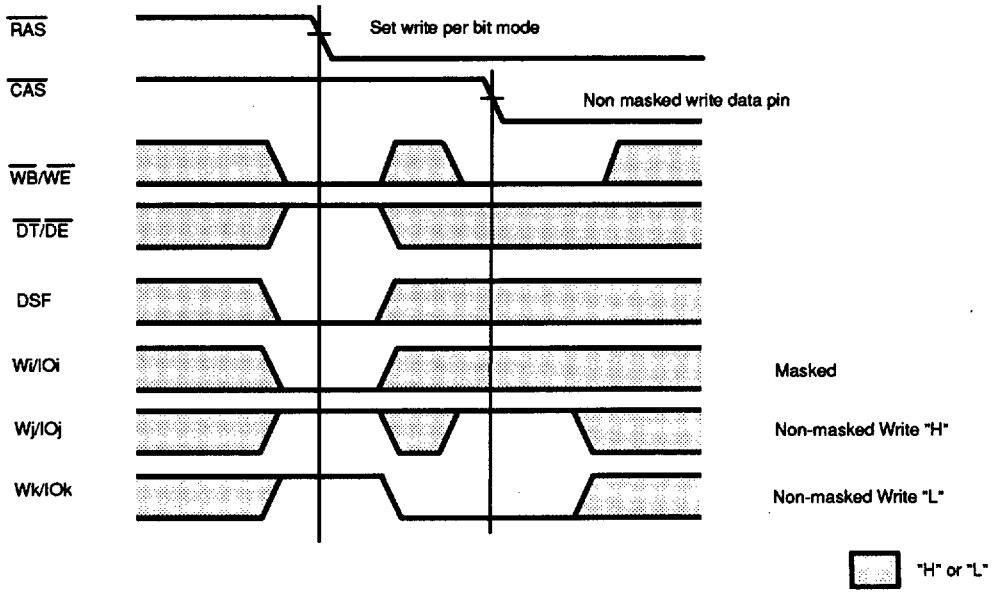


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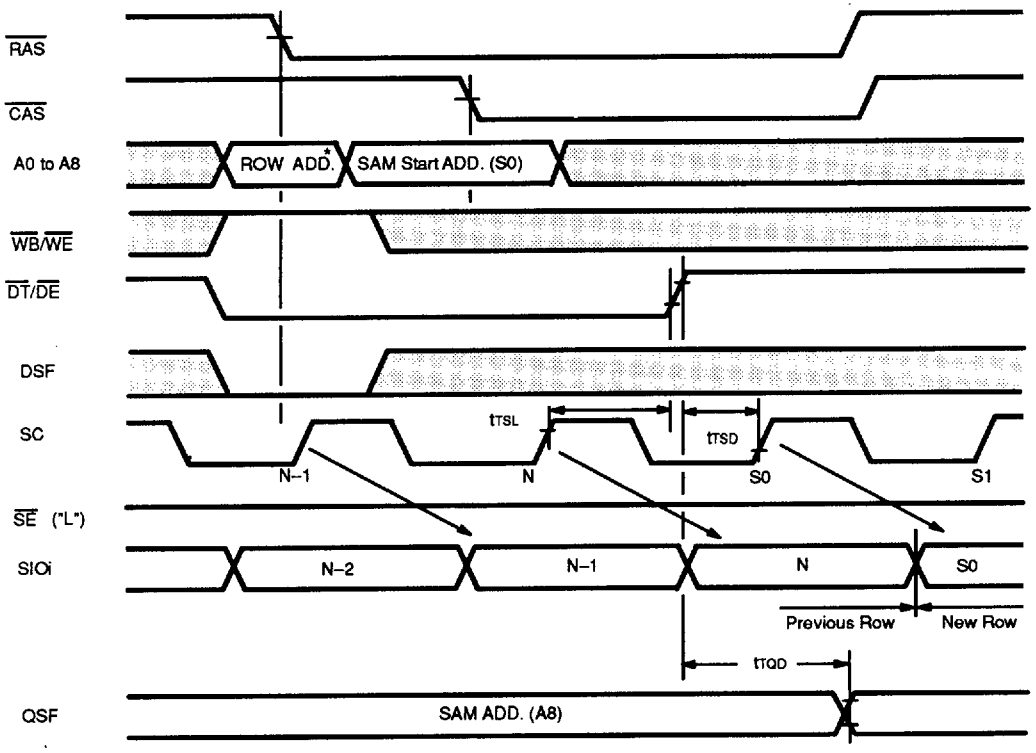
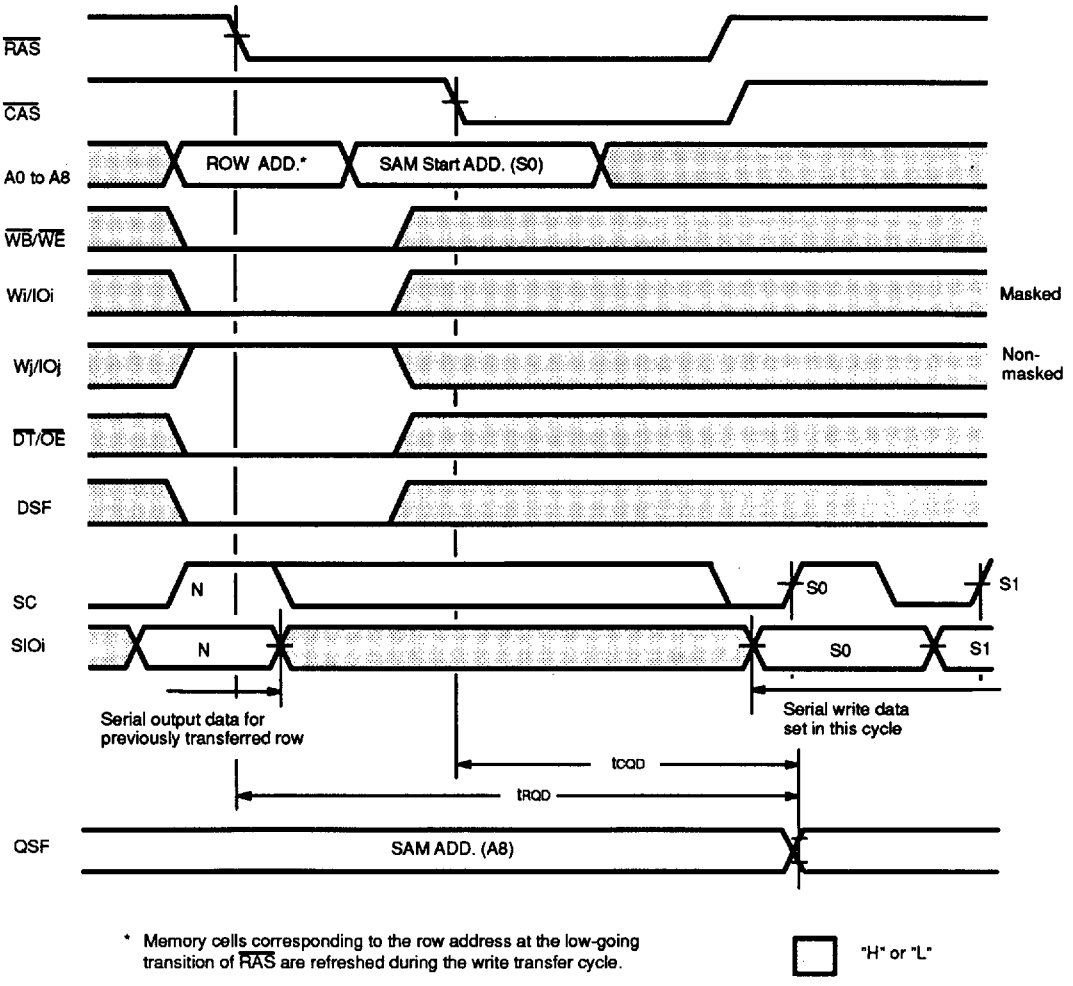
Fig. 3 - EXAMPLE OF REAL TIME READ TRANSFER OPERATION



* Memory cells corresponding to the row address at the low-going transition of $\overline{RAS}$ are refreshed during the read transfer cycle.

"H" or "L"

Fig. 4 - EXAMPLE OF WRITE TRANSFER CYCLE FOR NEW MASK

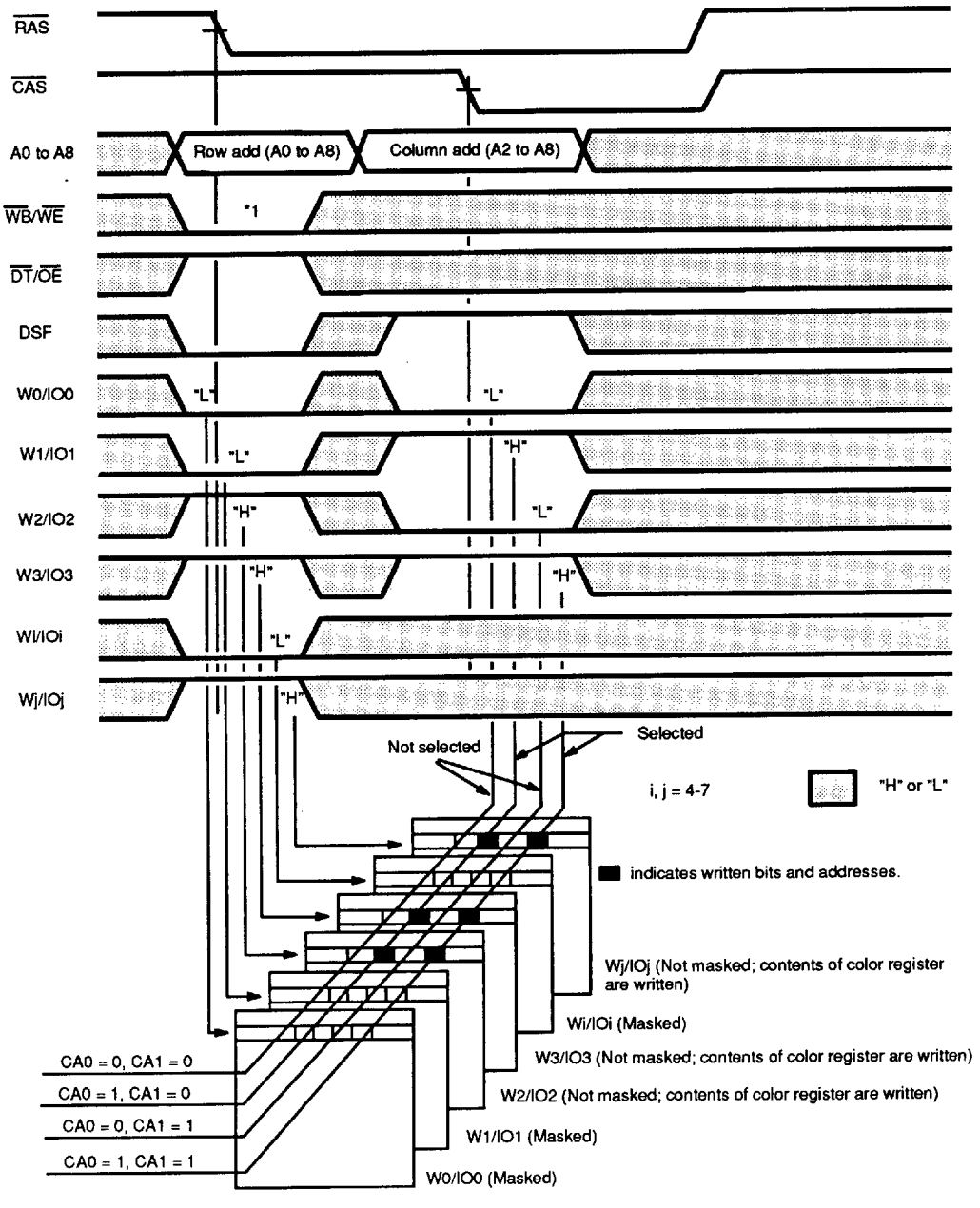


* Memory cells corresponding to the row address at the low-going transition of $\overline{RAS}$ are refreshed during the write transfer cycle.

"H" or "L"

4

Fig. 5 - EXAMPLE OF BLOCK WRITE OPERATION FOR NEW MASK



Note: * 1 No I/Os are masked when "H".

RECOMMENDED OPERATING CONDITIONS

(All voltages referenced to ground; T_A = 0°C to 70°C)

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage	Note 1	V_{CC}	4.5	5.0	5.5	V
		V_{SS}	0	0	0	
Input High Voltage, all inputs	Note 1	V_{IH}	2.4	—	6.5	V
Input Low Voltage, all inputs	Note 1	V_{IL}	–2.0	—	0.8	V
Input Low Voltage, Wi/IOi pins, SIOi pins	Note 1	V_{ILD}	–1.0 *	—	0.8	V

* Undershoots up to -2.0 volts with a pulse width not exceeding 20ns are acceptable.

Note 1: Voltages are referenced to VSS.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) See Note 1

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Output High Voltage	V_{OH}	I_{OH} = Wi/IOi: -5mA, SIOi, QSF: –2.5mA)	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = Wi/IOi: 4.2mA, SIOi, QSF: 2.1mA)	—	—	0.4	
Input Leakage Current (Any Input)	$I_{I(L)}$	0 V ≤ V_{IN} ≤ 5.5 V ; 4.5 V ≤ Vcc ≤ 5.5 V ; All other pins not under test = 0V	–10	—	10	µA
Output Leakage Current	$I_{O(L)}$	0 V ≤ V_{OUT} ≤ 5.5 V ; Data out is disabled	–10	—	10	

Note 1: A pause time of at least 200 µs after power-up followed by several dummy cycles are required for memory to operate properly. These dummy cycles may generally be 8 refresh cycles, 8 transfer cycles, and 8 pulses or more of SC clock. When using an internal refresh counter, add 8 or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles as dummy cycles. (Within the power-up and pause time, all control and address signals should be fixed high or low, or should 'be turned on in compliance with Vcc.)

DC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted) See Note 1

Parameter	Notes	Symbol	Conditions	Value Min	Value Typ	Value Max	Unit
SAM: STANDBY, $\overline{SE}$ = V_{IH}, SC = V_{IL}							
Operating Current Average power supply current	MB818255-70	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	110	mA
	MB818255-80					100	
Standby Current power supply current		I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	3.0	mA
			$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC}–0.2V			2.0	
$\overline{RAS}$ Only Refresh Average power supply current	MB818255-70	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling t_{RC} = min	—	—	110	mA
	MB818255-80					100	
Hyper Page Mode Average power supply current	MB818255-70	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{HPC} = min	—	—	115	mA
	MB818255-80					100	
$\overline{CAS}$–Before–$\overline{RAS}$ Refresh Average power supply current	MB818255-70	I_{CC5}	$\overline{CAS}$–before–$\overline{RAS}$; t_{RC} = min	—	—	90	mA
	MB818255-80					80	
Transfer Mode Average power supply current	MB818255-70	I_{CC6}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	120	mA
	MB818255-80					110	
Flash Write Mode Average power supply current	MB818255-70	I_{CC7}	$\overline{RAS}$ cycling; t_{RC} = min	—	—	100	mA
	MB818255-80					90	
Block Write Mode Average power supply current	MB818255-70	I_{CC8}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	110	mA
	MB818255-80					100	
Color/Mask Register Mode Average power supply current	MB818255-70	I_{CC9}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	110	mA
	MB818255-80					100	

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Notes :

1. A pause time of at least 200 us after power-up followed by several dummy cycles are required for memory to operate properly. These dummy cycles may generally be 8 refresh cycles, 8 transfer cycles, and 8 pulses or more of SC clock. When using an internal refresh counter, add 8 or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles as dummy cycles. (Within the power-up and pause time, all control and address signals should be fixed high or low, or should be turned on in compliance with VCC.)
2. The output pins are left open. ICC depends on the output load conditions and cycle rates. The indicated values are for VIL > -0.5V. The specified values of ICC1, ICC1A, ICC3, ICC3A, ICC5, ICC5A, ICC6, ICC6A, ICC8, and ICC8A indicate the supply current when addresses are switched over one time between $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH. Similarly, ICC4 and ICC4A indicate the supply current when addresses are switched over one time during one-page cycle.

DC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted) See Note 1

Parameter	Notes	Symbol	Conditions	Value Min	Value Typ	Value Max	Unit
SAM: ACTIVE, $\overline{SE}$ = VIL, tSCC = min							
Operating Current Average power supply current [2]	MB818255-70	ICC1A	$\overline{RAS}$ & $\overline{CAS}$ cycling; tRC = min	—	—	190	mA
	MB818255-80					165	
Standby Current Average power supply current [2]	MB818255-70	ICC2A	$\overline{RAS}$ = $\overline{CAS}$ = VIH	—	—	80	mA
	MB818255-80					65	
$\overline{RAS}$ Only Refresh Average power supply current [2]	MB818255-70	ICC3A	$\overline{CAS}$ = VIH, $\overline{RAS}$ cycling tRC = min	—	—	190	mA
	MB818255-80					165	
Hyper Page Mode Average power supply current [2]	MB818255-70	ICC4A	$\overline{RAS}$ = VIL, $\overline{CAS}$ cycling tHPC = min	—	—	195	mA
	MB818255-80					165	
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Average power supply current [2]	MB818255-70	ICC5A	$\overline{CAS}$-before-$\overline{RAS}$; tRC = min	—	—	170	mA
	MB818255-80					145	
Transfer Mode Average power supply current [2]	MB818255-70	ICC6A	$\overline{RAS}$ & $\overline{CAS}$ cycling; tRC = min	—	—	200	mA
	MB818255-80					175	
Flash Write Mode Average power supply current [2]	MB818255-70	ICC7A	$\overline{RAS}$ cycling; tRC = min	—	—	180	mA
	MB818255-80					155	
Block Write Mode Average power supply current [2]	MB818255-70	ICC8A	$\overline{RAS}$ & $\overline{CAS}$ cycling; tRC = min	—	—	190	mA
	MB818255-80					165	
Color/Mask Register Mode Average power supply current [2]	MB818255-70	ICC9A	$\overline{RAS}$ & $\overline{CAS}$ cycling; tRC = min	—	—	190	mA
	MB818255-80					165	

Notes :

1. A pause time of at least 200 us after power-up followed by several dummy cycles are required for memory to operate properly. These dummy cycles may generally be 8 refresh cycles, 8 transfer cycles, and 8 pulses or more of SC clock. When using an internal refresh counter, add 8 or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles as dummy cycles. (Within the power-up and pause time, all control and address signals should be fixed high or low, or should be turned on in compliance with VCC.)
2. The output pins are left open. ICC depends on the output load conditions and cycle rates. The indicated values are for VIL > -0.5V. The specified values of ICC1, ICC1A, ICC3, ICC3A, ICC5, ICC5A, ICC6, ICC6A, ICC8, and ICC8A indicate the supply current when addresses are switched over one time between $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH. Similarly, ICC4 and ICC4A indicate the supply current when addresses are switched over one time during one-page cycle.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) See Note 3,4 and 5 on page 4-182

No.	Parameter	Symbol	MB818255-70		MB818255-80		Unit	Note
			Min	Max	Min	Max		
1	Time Between Refresh	tREF	—	8.2	—	8.2	ms	—
2	Random Read/Write Cycle Time	tRC	125	—	140	—	ns	—
3	Read-Modify-Write Cycle Time	tRWC	170	—	190	—	ns	—
4	Access Time from $\overline{RAS}$	tRAC	—	70	—	80	ns	6,9
5	Access Time from $\overline{CAS}$	tCAC	—	20	—	20	ns	7,9
6	Access Time from Column Address	tAA	—	35	—	40	ns	8,9
7	Output Hold Time from $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	tOH	0	—	0	—	ns	—
8	Output Hold Time from $\overline{CAS}$	tOHC	5	—	5	—	ns	—
9	Output Buffer Turn On Delay Time from $\overline{CAS}$, $\overline{OE}$	tON	0	—	0	—	ns	—
10	Output Buffer Turn Off Delay Time from $\overline{CAS}$, $\overline{OE}$	tOFF	—	15	—	20	ns	10
11	Output Buffer Turn Off Delay Time from $\overline{RAS}$	tOFR	—	15	—	20	ns	—
12	Output Buffer Turn Off Delay Time from $\overline{WE}$	tWEZ	—	15	—	20	ns	—
13	Transition Time	tT	2	50	2	50	ns	—
14	$\overline{RAS}$ Precharge Time	tRP	45	—	50	—	ns	—
15	$\overline{RAS}$ Pulse Width	tRAS	70	100000	80	100000	ns	—
16	$\overline{RAS}$ Hold Time	tRSH	20	—	20	—	ns	—
17	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	0	—	0	—	ns	—
18	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	20	50	20	60	ns	11, 12
19	$\overline{CAS}$ Pulse Width	tCAS	12	—	15	—	ns	—
20	$\overline{CAS}$ Hold Time	tCSH	70	—	80	—	ns	—
21	$\overline{CAS}$ Precharge Time	tCPN	10	—	10	—	ns	19
22	Row Address Set Up Time	tASR	0	—	0	—	ns	—
23	Row Address Hold Time	tRAH	10	—	10	—	ns	—
24	Column Address Set Up Time	tASC	0	—	0	—	ns	—
25	Column Address Hold Time	tCAH	12	—	15	—	ns	—
26	$\overline{RAS}$ to Column Address Delay Time	tRAD	15	35	15	40	ns	13
27	Column Address to $\overline{RAS}$ Lead Time	tRAL	35	—	40	—	ns	—
28	Column Address to $\overline{CAS}$ Lead Time	tCAL	25	—	30	—	ns	—
29	Read Command Set Up Time	tRCS	0	—	0	—	ns	—
30	Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	0	—	0	—	ns	14

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) **See Note 3,4, and5 on page 4-182**

No.	Parameter	Symbol	MB818255-70		MB818255-80		Unit	Note
			Min	Max	Min	Max		
31	Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0	—	0	—	ns	14
32	Write Command Set Up Time	tWCS	0	—	0	—	ns	15
33	Write Command Hold Time	tWCH	10	—	12	—	ns	—
34	Write Pulse Width	tWP	10	—	12	—	ns	—
35	Write Command to $\overline{RAS}$ Lead Time	tRWL	20	—	20	—	ns	—
36	Write Command to $\overline{CAS}$ Lead Time	tCWL	12	—	15	—	ns	—
37	DIN Set Up Time	tDS	0	—	0	—	ns	—
38	DIN Hold Time	tDH	12	—	15	—	ns	—
39	$\overline{RAS}$ to $\overline{WE}$ Delay Time	tRWD	90	—	105	—	ns	—
40	$\overline{CAS}$ to $\overline{WE}$ Delay Time	tCWD	40	—	45	—	ns	—
41	Column Address to $\overline{WE}$ Delay Time	tAWD	55	—	65	—	ns	—
42	$\overline{CAS}$ to Data In Delay Time	tCDD	15	—	20	—	ns	—
43	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time	tRPC	0	—	0	—	ns	—
44	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before $\overline{RAS}$ Refresh	tCSR	0	—	0	—	ns	—
45	$\overline{CAS}$ Hold Time for $\overline{CAS}$–before $\overline{RAS}$ Refresh	tCHR	10	—	12	—	ns	—
46	Access Time from $\overline{OE}$	tOEA	—	20	—	20	ns	9
47	Output Buffer Turn Off Delay from $\overline{OE}$	tOEZ	—	15	—	20	ns	10
48	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data	tOEL	10	—	10	—	ns	—
49	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	tOEH	0	—	0	—	ns	16
50	$\overline{OE}$ to Data In Delay Time	tOED	15	—	20	—	ns	
51	DIN to $\overline{CAS}$ Delay Time	tDZC	0	—	0	—	ns	17
52	DIN to $\overline{OE}$ Delay Time	tDZO	0	—	0	—	ns	17
53	$\overline{OE}$ Precharge Time	tOEP	10	—	10	—	ns	—
54	$\overline{CAS}$ to $\overline{OE}$ Set Up Time	tECS	10	—	10	—	ns	—
55	$\overline{OE}$ to $\overline{CAS}$ Hold Time	tECH	10	—	10	—	ns	—
56	Hyper Page Mode $\overline{RAS}$ Pulse Width	tRASP	—	200000	—	200000	ns	—
57	Hyper Page Mode Read/Write Cycle Time	tHPC	35	—	40	—	ns	—
58	Hyper Page Mode Read–Modify–Write Cycle	tHPRWC	88	—	100	—	ns	—

4

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) **See Notes 3,4, and 5 on page** 4-182

No.	Parameter	Symbol	MB818255-70		MB818255-80		Unit	Note
			Min	Max	Min	Max		
59	Access Time from $\overline{CAS}$ Precharge	tCPA	—	40	—	45	ns	9, 18
60	Hyper Page Mode $\overline{CAS}$ PrechargeTime	tCP	10	—	10	—	ns	—
61	Hyper Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	tRHCP	40	—	45	—	ns	—
62	Hyper Page Mode Wrtie Command Delay Time from $\overline{CAS}$ Precharge	tCPWD	60	—	70	—	ns	—
63	Serial Clock Cycle Time	tSCC	20	—	25	—	ns	—
64	Access Time from SC	tSCA	—	20	—	25	ns	20
65	Access Time from $\overline{SE}$	tSEA	—	20	—	20	ns	20
66	SC Precharge Time	tSCP	5	—	7	—	ns	—
67	SC Pulse Width	tSC	5	—	7	—	ns	—
68	$\overline{SE}$ Precharge Time	tSEP	10	—	12	—	ns	—
69	$\overline{SE}$ Pulse Width	tSE	10	—	12	—	ns	—
70	Serial Data Out Hold Time after SC High	tSOH	5	—	5	—	ns	—
71	Serial Output Buffer Turn Off Delay from $\overline{SE}$	tSEZ	—	15	—	20	ns	—
72	Serial Data In Setup Time	tSDS	0	—	0	—	ns	—
73	Serial Data In Hold Time	tSDH	10	—	12	—	ns	—
74	Transfer Command $\overline{RAS}$ Setup Time	tTLS	0	—	0	—	ns	—
75	Transfer Command $\overline{RAS}$ Hold Time	tRTH	55	—	60	—	ns	—
76	Transfer Command $\overline{CAS}$ Hold Time	tCTH	10	—	10	—	ns	—
77	Transfer Command SAM Start Address Hold Time	tATH	20	—	20	—	ns	—
78	$\overline{RAS}$ to First SC Delay Time (during Read Transfer)	tRSD	70	—	80	—	ns	22
79	$\overline{CAS}$ to First SC Delay Time (during Read Transfer)	tCSD	25	—	30	—	ns	22
80	Column Address to First SC Delay Time (during Read Transfer)	tASD	35	—	40	—	ns	22
81	Output Turn On Delay Time (SAM Port)	tSON	0	—	0	—	ns	—
82	Transfer Command $\overline{RAS}$ Hold Time (Write Transfer)	tTLH	10	—	10	—	ns	—
83	$\overline{DT}$ to RAS Precharge Time	tTRP	60	—	70	—	ns	—
84	$\overline{DT}$ Precharge Time (during Read Transfer)	tTP	20	—	20	—	ns	—
85	Transfer Command SC Lead Time	tTSL	0	—	0	—	ns	—
86	First SC Edge to Transfer Command Delay Time	tTSD	10	—	15	—	ns	—

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) **See Notes 3, 4, and 5 on page 4-182**

No.	Parameter	Symbol	MB818255-70		MB818255-80		Unit	Note
			Min	Max	Min	Max		
87	$\overline{WB}$ to $\overline{RAS}$ Set Up Time	tWSR	0	—	0	—	ns	—
88	$\overline{WB}$ to $\overline{RAS}$ Hold Time	tRWH	10	—	10	—	ns	—
89	Mask Data (Wi) $\overline{RAS}$ Set Up Time	tMS	0	—	0	—	ns	—
90	Mask Data (Wi) $\overline{RAS}$ Hold Time	tMH	10	—	10	—	ns	—
91	Serial Output Buffer Turn Off Delay Time from $\overline{RAS}$	tSDZ	0	35	0	40	ns	
92	SC to $\overline{RAS}$ Setup Time	tSRS	20	—	25	—	ns	—
93	Serial Data Input to $\overline{SE}$ Delay Time	tSZE	0	—	0	—	ns	—
94	Serial Data Input Delay Time from $\overline{RAS}$	tSDD	35	—	40	—	ns	21
95	Serial Data Input to SC Delay Time	tSZS	0	—	0	—	ns	22
96	Serial Write Enable Set Up Time	tSWS	0	—	0	—	ns	—
97	Serial Write Enable Hold Time	tSWH	10	—	12	—	ns	—
98	Serial Write Disable Set Up Time	tSWIS	0	—	0	—	ns	—
99	Serial Write Disable Hold Time	tSWIH	10	—	12	—	ns	—
100	Transfer Inhibit Command to $\overline{RAS}$ Set Up Time	tTHS	0	—	0	—	ns	—
101	Asynchronous Command to $\overline{RAS}$ Set Up Time	tTHH	10	—	10	—	ns	—
102	DSF to $\overline{RAS}$ Set Up Time	tFSR	0	—	0	—	ns	—
103	DSF to $\overline{RAS}$ Hold Time	tRFH	10	—	10	—	ns	—
104	DSF to $\overline{CAS}$ Setup Time	tFSC	0	—	0	—	ns	—
105	DSF to $\overline{CAS}$ Hold Time	tCFH	12	—	15	—	ns	—
106	Split Transfer Set Up Time	tSTS	20	—	25	—	ns	—
107	$\overline{RAS}$ to SC Delay Time (during Split Transfer)	tRST	70	—	80	—	ns	—
108	$\overline{CAS}$ to SC Delay Time (during Split Transfer)	tCST	25	—	30	—	ns	—
109	Column Address to SC Delay Time (during Split Transfer)	tAST	35	—	40	—	ns	—
110	SC to QSF Delay Time	tSQD	—	30	—	35	ns	23
111	DT to QSF Delay Time	tTQD	—	30	—	35	ns	23
112	$\overline{CAS}$ to QSF Delay Time	tCQD	—	30	—	35	ns	23
113	$\overline{RAS}$ to QSF Delay Time	tRQD	—	70	—	80	ns	23
114	QSF Hold Time Referenced to SC	tSQH	5	—	5	—	ns	—
115	QSF Hold Time Referenced to $\overline{DT}$	tTQH	5	—	5	—	ns	—

Notes:

1. Voltages are referenced to VSS.
2. The output pins are left open. ICC depends on the output load conditions and cycle rates. The indicated values are for VIL > -0.5V. The specified values of ICC1, ICC1A, ICC3, ICC3A, ICC5, ICC5A, ICC6, ICC6A, ICC8, and ICC8A indicate the supply current when addresses are switched over one time between $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH. Similarly, ICC4 and ICC4A indicate the supply current when addresses are switched over one time during one-page cycle.
3. A pause time of at least 200 us after power-up followed by several dummy cycles are required for memory to operate properly. These dummy cycles may generally be 8 refresh cycles, 8 transfer cycles, and 8 pulses or more of SC clock. When using an internal refresh counter, add 8 or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles as dummy cycles. (Within the power-up and pause time, $\overline{RAS}$, $\overline{DT/OE}$ signals should be fixed high and other control and address signals should be fixed high or low, or should be turned on in compliance with VCC.)
4. AC characteristics values are measured with tT = 5 ns.
5. VIH (min) and VIL (max) are the reference levels for measuring the input signal timing. Transition time (tT) is a duration of time required for transition between VIH and VIL.
6. tRAC (max) is guaranteed under conditions tRCD < tRCD (max), tRAD < tRAD (max). Therefore, if tRCD > tRCD (max), tRAD > tRAD (max), tRAC will be increased by the amount equivalent to an excess over the maximum value. Refer to Figures 6 and 7.

4

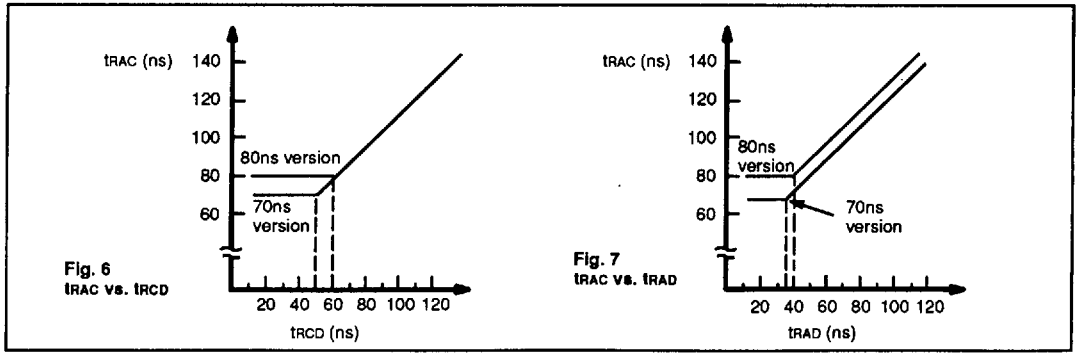


Fig. 6 tRAC vs. tRCD

Fig. 7 tRAC vs. tRAD

7. If tASC > tAA - tCAC - tT when tRCD > tRCD (max), tRAD > tRAD (max), the access time is governed by $\overline{CAS}$.
8. If tASC > tAA - tCAC - tT when tRAD > tRAD (max), the access time is governed by the column address.
9. Measured with two TTL loads plus 50 pF.
10. tOFF and tOEZ are regulated by the time the internal output buffer goes to a high-impedance state.
11. tRCD (max) indicates the maximum point of tRCD where tRAC (max) is guaranteed, and not an operational limit point. If tRCD > tRCD (max), the access time is governed by tCAC or tAA.
12. tRCD (min) = tRAH (min) + 2tT + tASC (min)

13. tRAD (max) indicates the maximum point of tRAD where tRAC (max) is guaranteed, and not an operational limit point. If tRAD > tRAD (max), the access time depends on tCAC or tAA.
14. Operation is guaranteed whichever timing requirement tRCH or tRRH is met.
15. tWCS indicates a point where early write operation mode is regulated, and not an operational limit point of the device. If tWCS > tWCS (min), the Wi/IOi (output) pin is left open (high-impedance) during that cycle period.
16. Applies only when tWCS < tWCS (min).
17. Operation is guaranteed whichever timing requirement tDZC or tDZO is met.
18. tCPA regulates the access time when the column address is unlatched and the first new column address is selected by forcing $\overline{CAS}$ from low to high. Therefore, if tCP is long, tCPA lags tCPA (max) as shown in Figure 8.

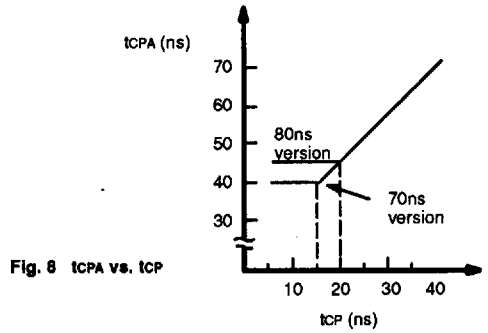


Fig. 8 tCPA vs. tCP

19. Stipulated for only $\overline{CAS}$-before-$\overline{RAS}$ refresh.
20. Measured with one TTL load plus 30 pF.
21. Stipulated for operation in write transfer when the preceding transfer was a read transfer.
22. Stipulated for operation in read transfer when the previous transfer was a write transfer.
23. Measured with one TTL load plus 30 pF.

4

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Max			Unit
		S-ZIP	SOJ	TSOP	
Input Capacitance (A0 to A8)	C_{IN1}	7	7	7	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, DSF)	C_{IN2}	7	7	7	pF
Input Capacitance (SC, $\overline{SE}$)	C_{IN3}	7	7	7	pF
Input/Output Capacitance (W0/IO0 to W7/IO7)	C_{IO1}	8	7	7	pF
Input/Output Capacitance (SIO0 to SIO7)	C_{IO2}	7	7	7	pF
Output Capacitance (QSF)	C_{OUT1}	7	7	7	pF

4

AC TEST CONDITIONS

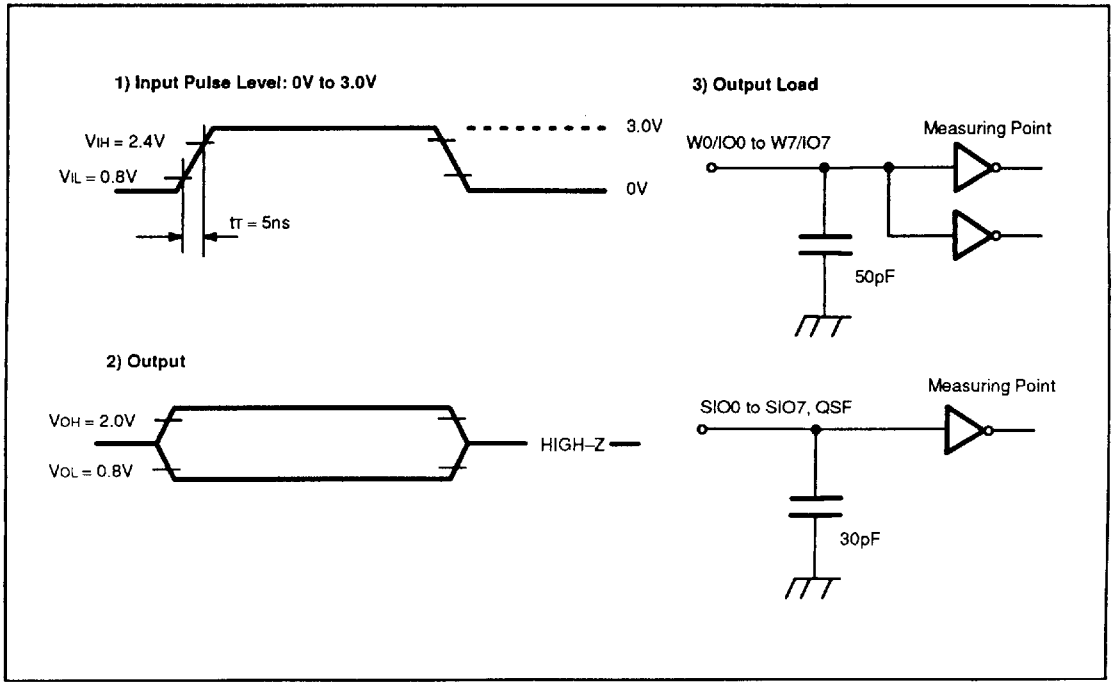
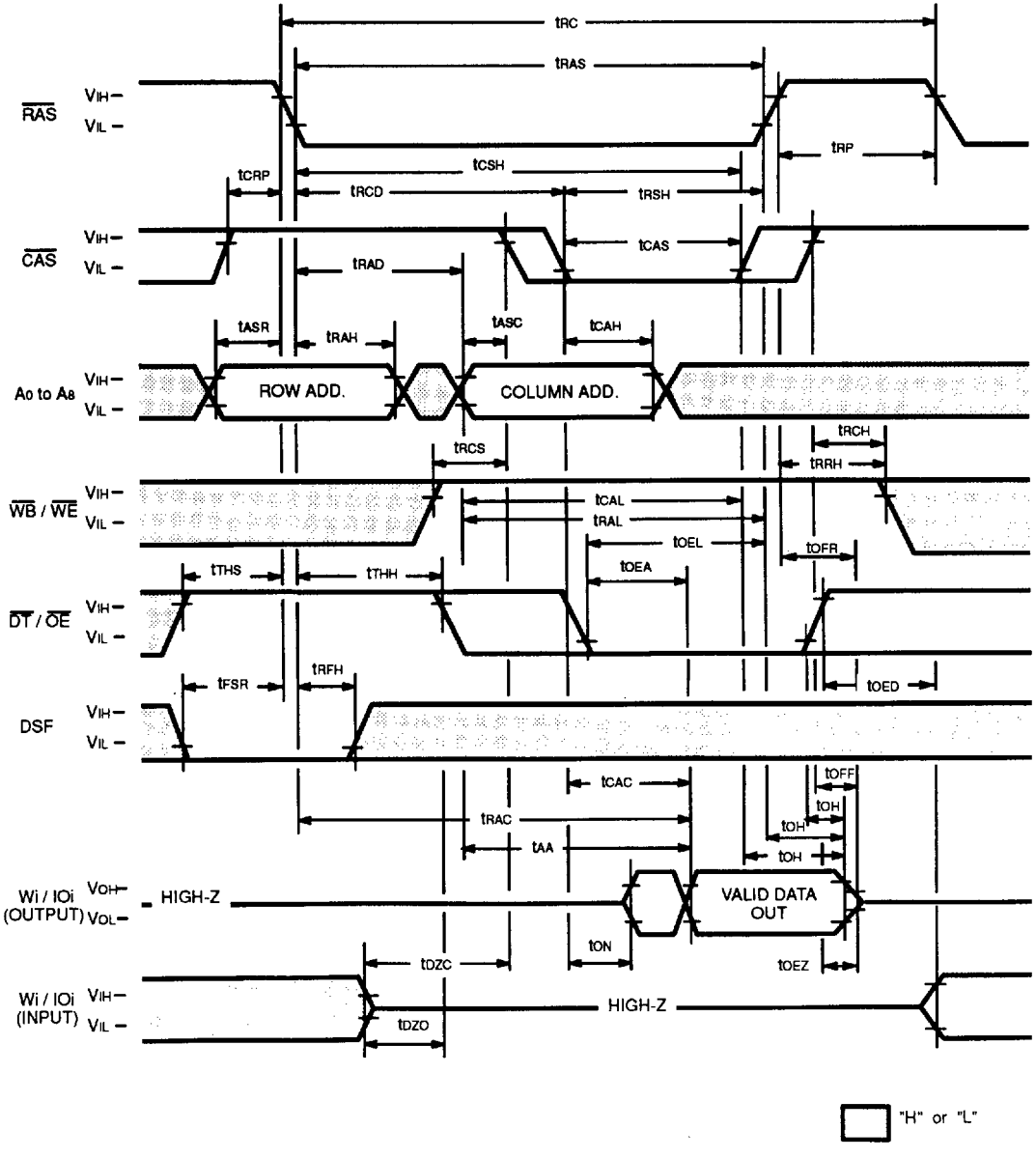
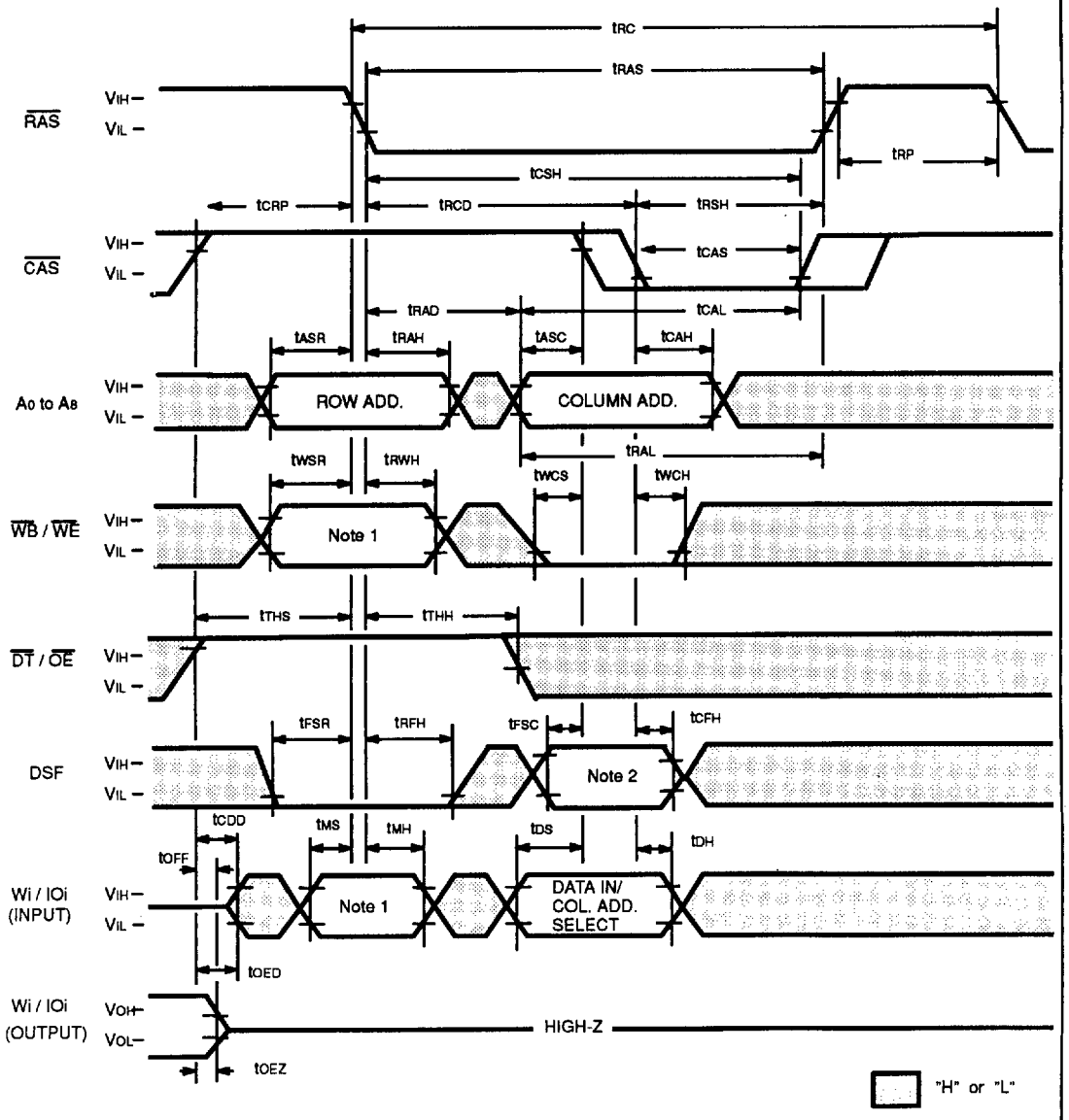


Fig. 9 – READ CYCLE



4

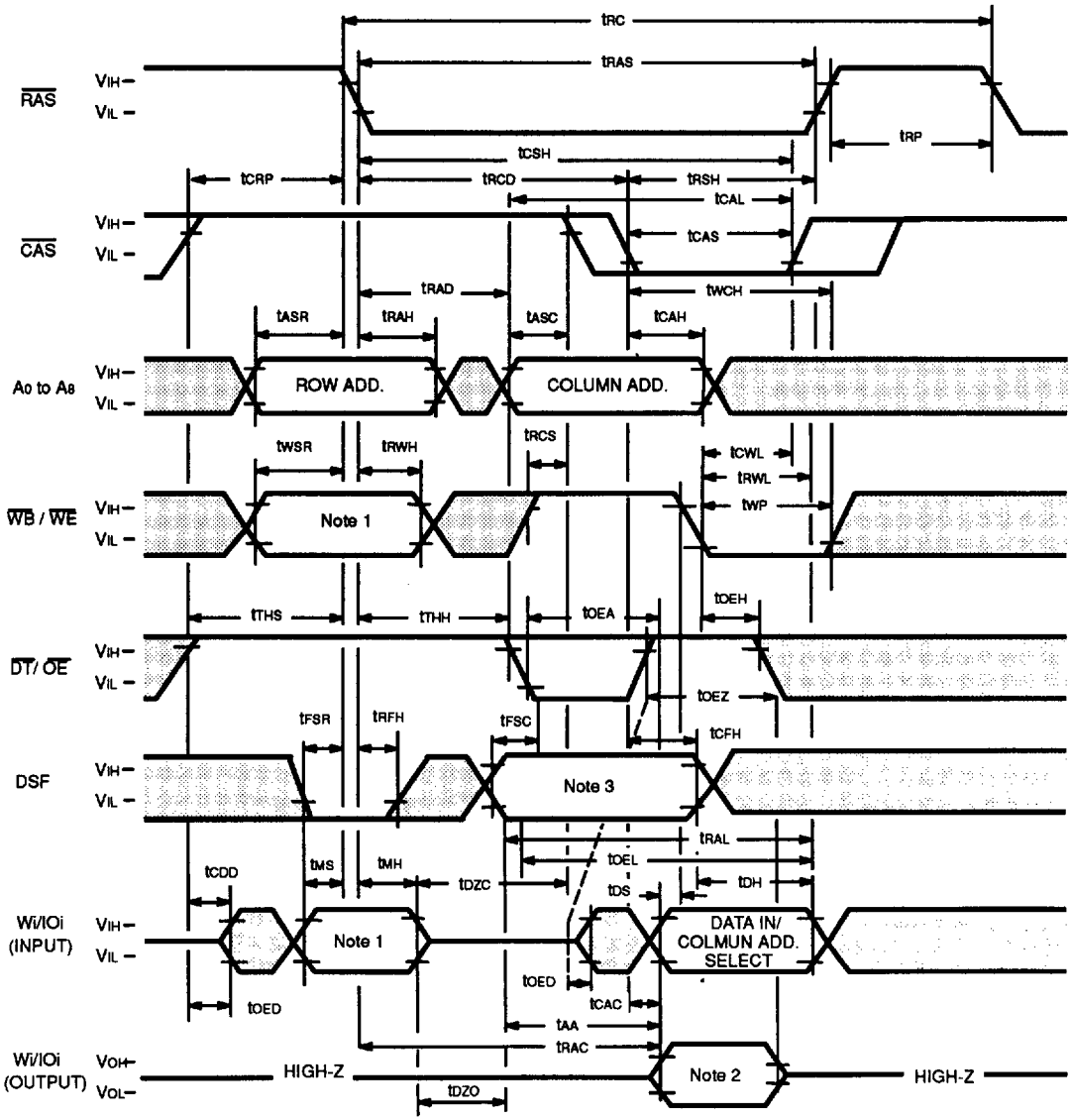
Fig. 10 – WRITE CYCLE (EARLY WRITE)



Note 1 : When $\overline{WB/WE}$ = "H", all data of Wi/IOi can be written into the cell.
When $\overline{WB/WE}$ = "L", write-per-bit mode is entered and writes to memory cells can be inhibited by data of Wi/IOi in case of new mask mode and by data of mask register in case of old mask mode.

Note 2: When DSF = "H", block write mode is entered and the contents of the color register can be written into the cell.

Fig. 11 – WRITE CYCLE ($\overline{OE}$ CONTROL)



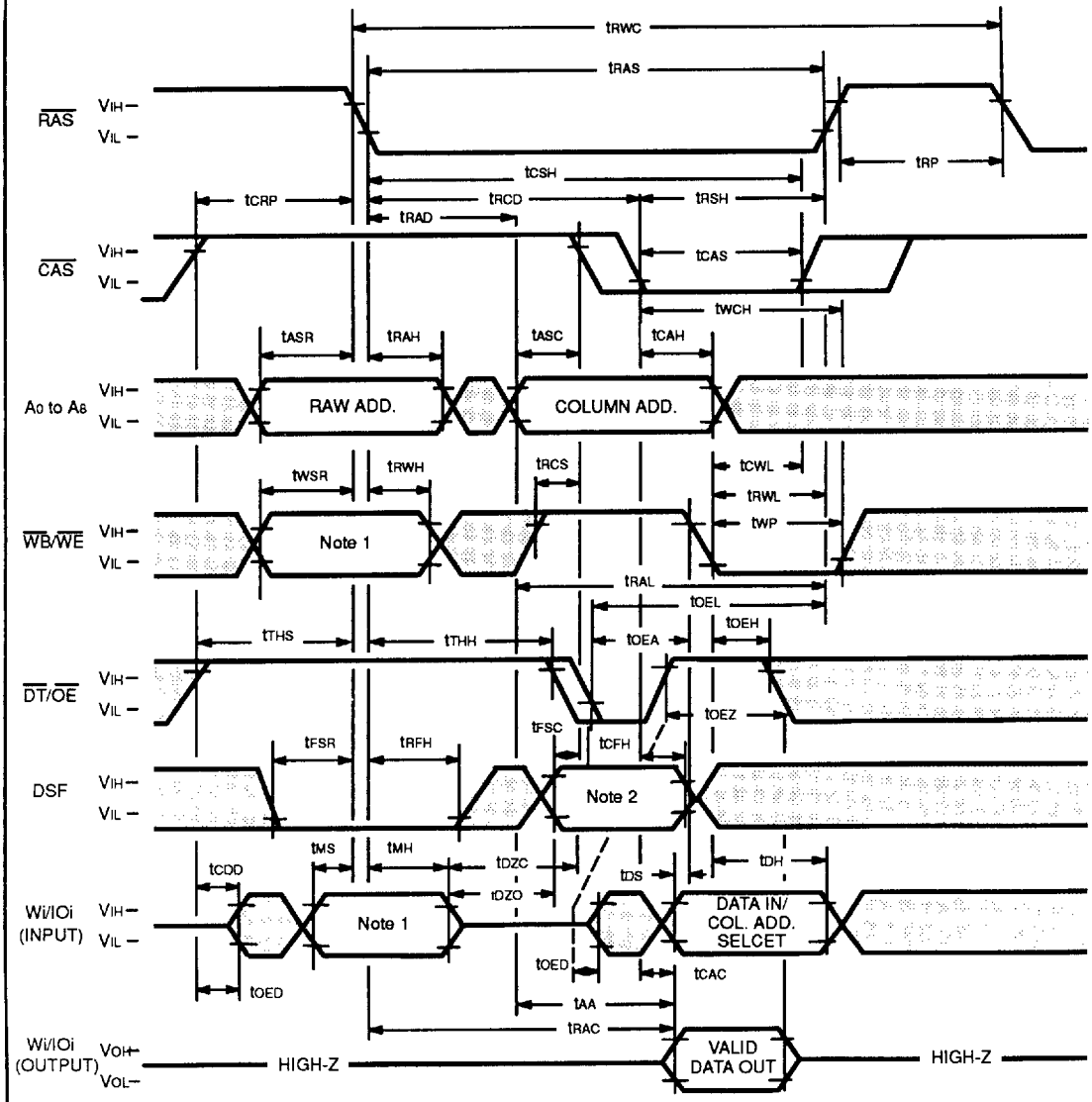
Note 1: When $\overline{WB}/\overline{WE}$ = "H", all data of Wi/IOi can be written into the cell.
When $\overline{WB}/\overline{WE}$ = "L", write-per-bit mode is entered and writes to memory cells can be inhibited by data of Wi/IOi in case of new mask mode and by data of mask register in case of old mask mode.

Note 2: If $\overline{DT}/\overline{OE}$ is kept "H" during the cycle, Wi/IOi are placed in the high-impedance state.

Note 3: When DSF = "H", block write mode is entered and the contents of the color register can be written into the cell.

4

Fig. 12 – READ•WRITE/READ-MODIFY-WRITE CYCLE

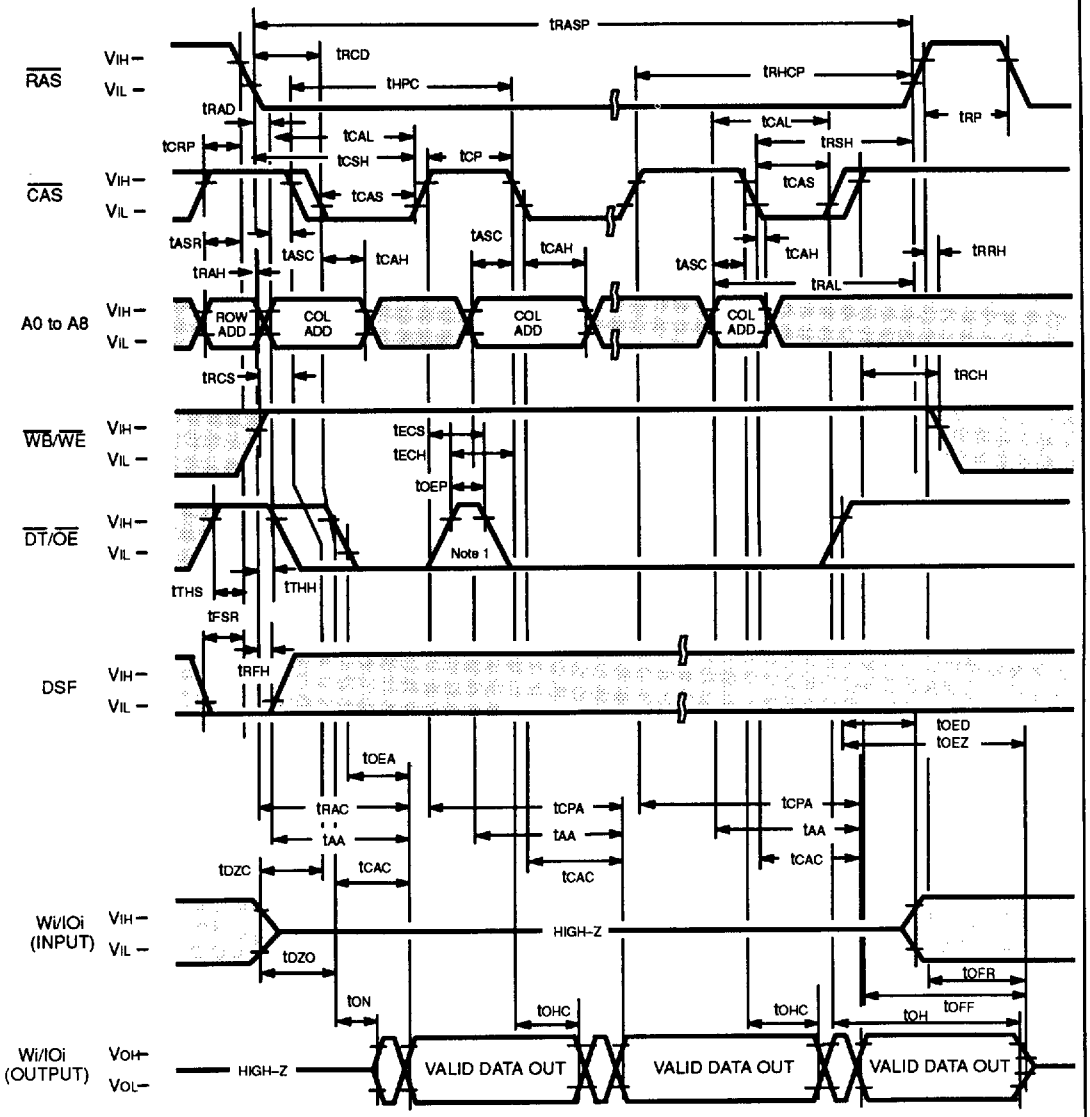


Note 1 : When $\overline{WB/WE}$ = "H", all data of Wi/IOi can be written into the cell.
When $\overline{WB/WE}$ = "L", write-per-bit mode is entered and writes to memory cells can be inhibited by data of Wi/IOi in case of new mask mode and by data of mask register in case of old mask mode.

Note 2: When DSF = "H", block write mode is entered and the contents of the color register can be written into the cell.

□ "H" or "L"

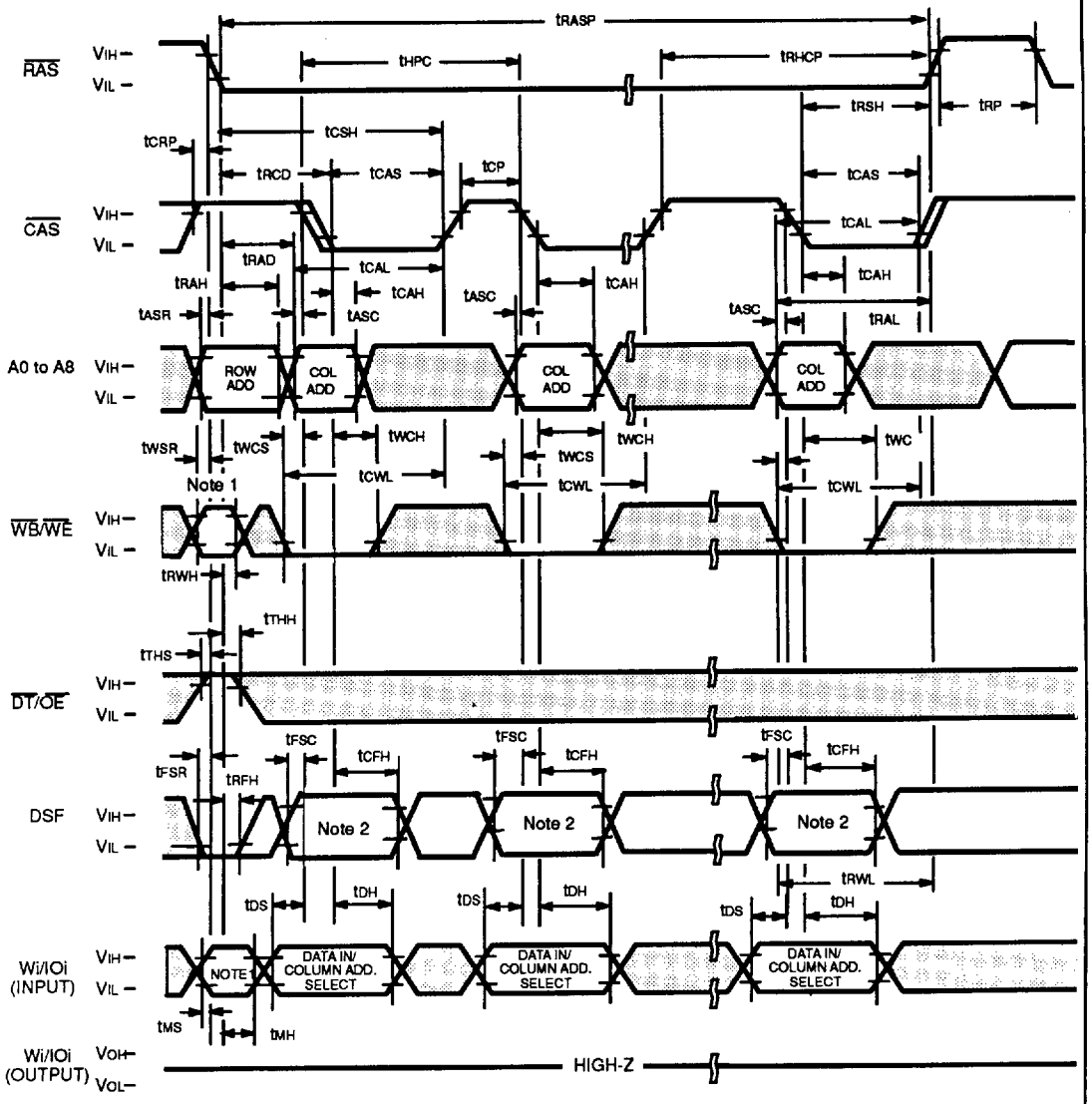
Fig. 13 – HYPER PAGE MODE READ CYCLE



Note 1: When $\overline{OE}$ goes to "H", output becomes high impedance state. After that when $\overline{OE}$ goes "L" during $\overline{CAS}$ = "H" output is remain high impedance state.

"H" or "L"

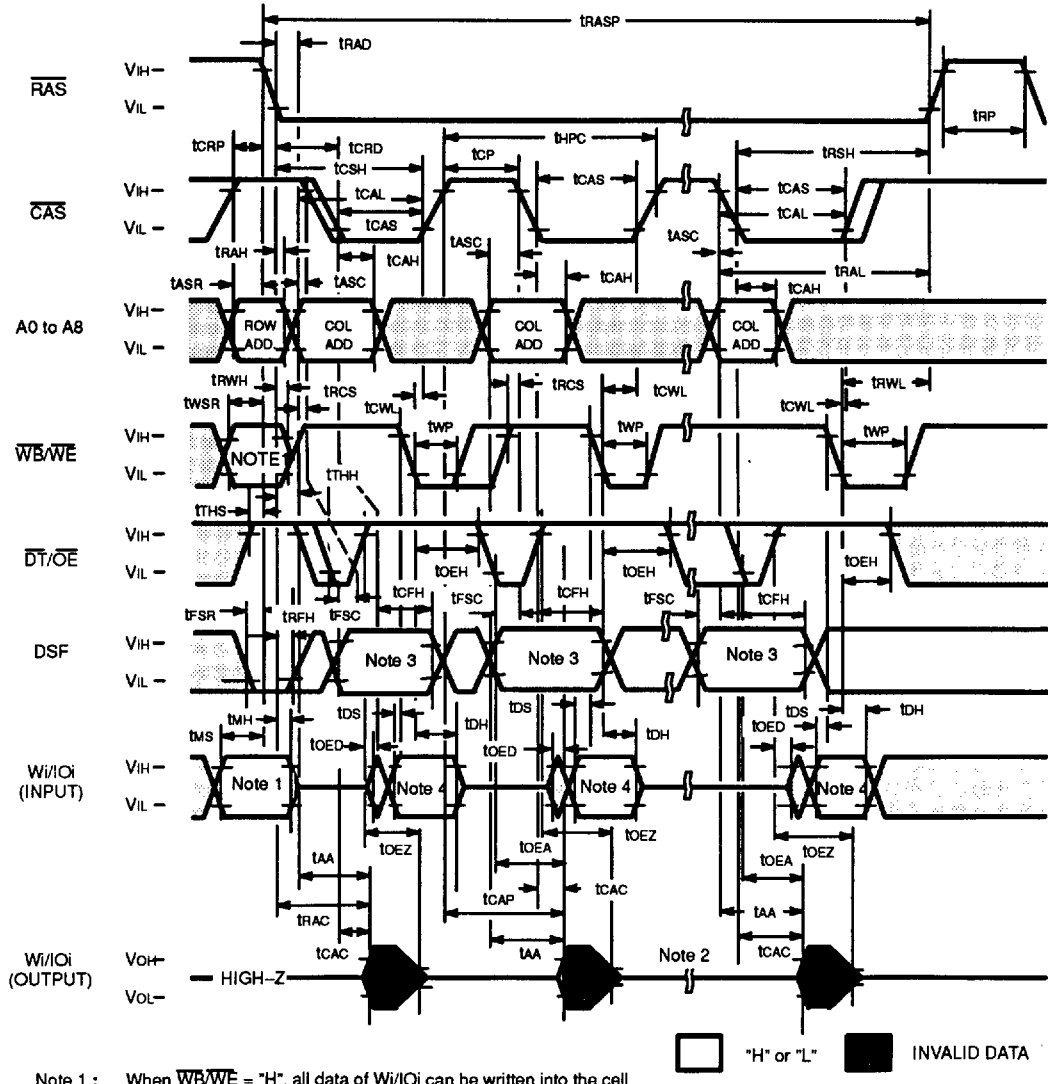
Fig. 14 – HYPER PAGE MODE WRITE CYCLE



Note 1 : When $\overline{WB/WE}$ = "H", all data of Wi/IOi can be written into the cell.
When $\overline{WB/WE}$ = "L", write-per-bit mode is entered and writes to memory cells can be inhibited by data of Wi/IOi in case of new mask mode and by data of mask register in case of old mask.

Note 2: When DSF = "H", block write mode is entered and the contents of the color register can be written into the cell.

Fig. 15 – HYPER PAGE MODE $\overline{OE}$ WRITE CYCLE



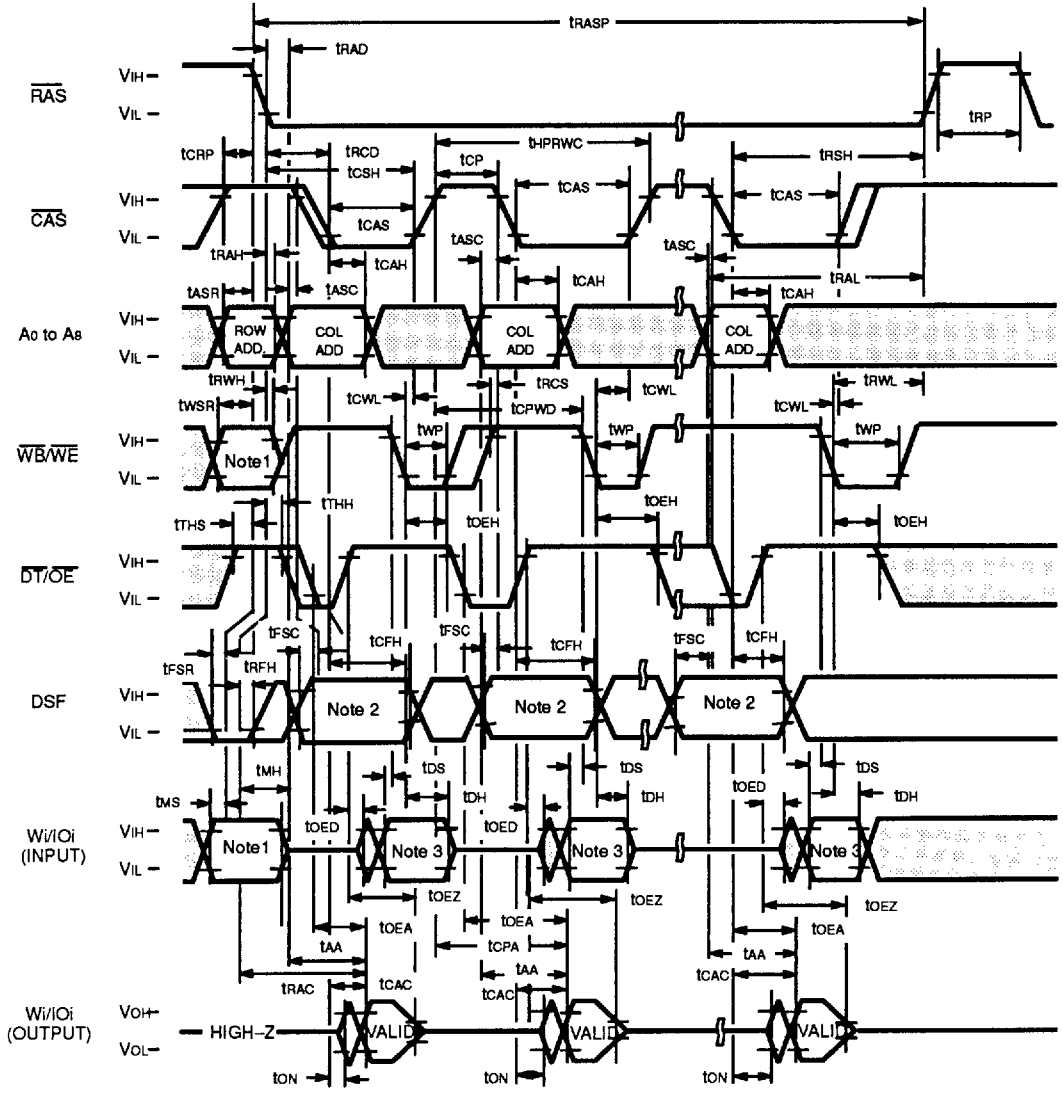
Note 1 : When $\overline{WB/WE}$ = "H", all data of Wi/IOi can be written into the cell.
When $\overline{WB/WE}$ = "L", write-per-bit mode is entered and writes to memory cells can be inhibited by data of Wi/IOi in case of new mask mode and by data of mask register in case of old mask mode.

Note 2: If $\overline{DT/OE}$ is kept "H" during the cycle, Wi/IOi are placed in the high-impedance state.

Note 3: When DSF = "H", block write mode is entered and the contents of the color register can be written into the cell.

Note 4: DATA IN / COLUMN ADD. SELECT

Fig. 16 – HYPER PAGE MODE READ-MODIFY-WRITE CYCLE



Note 1 : When $\overline{WB/WE}$ = "H", all data of Wi/IOi can be written into the cell.
When $\overline{WB/WE}$ = "L", write-per-bit mode is entered and writes to memory cells can be inhibited by data of Wi/IOi in case of new mask mode and by data of mask register in case of old mask mode.

Note 2: When DSF = "H", block write mode is entered and the contents of the color register can be written into the cell.

Note 3: DATA IN/ COLUMN ADD. SELECT

Fig. 17 – $\overline{RAS}$ ONLY REFRESH CYCLE

($\overline{WB}/\overline{WE}$ and W0/IO0 to W7/IO7 (input) = "H" or "L")

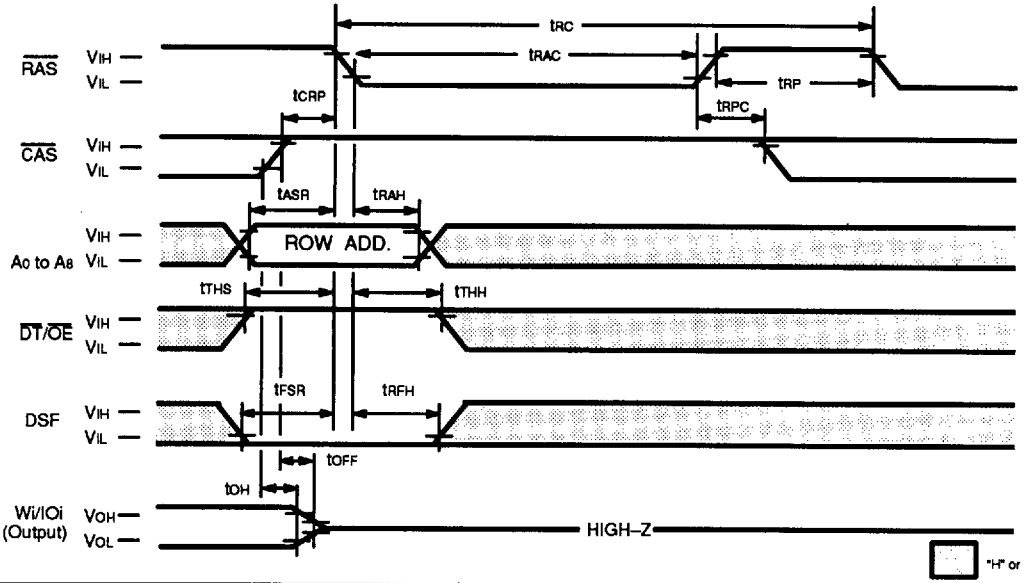
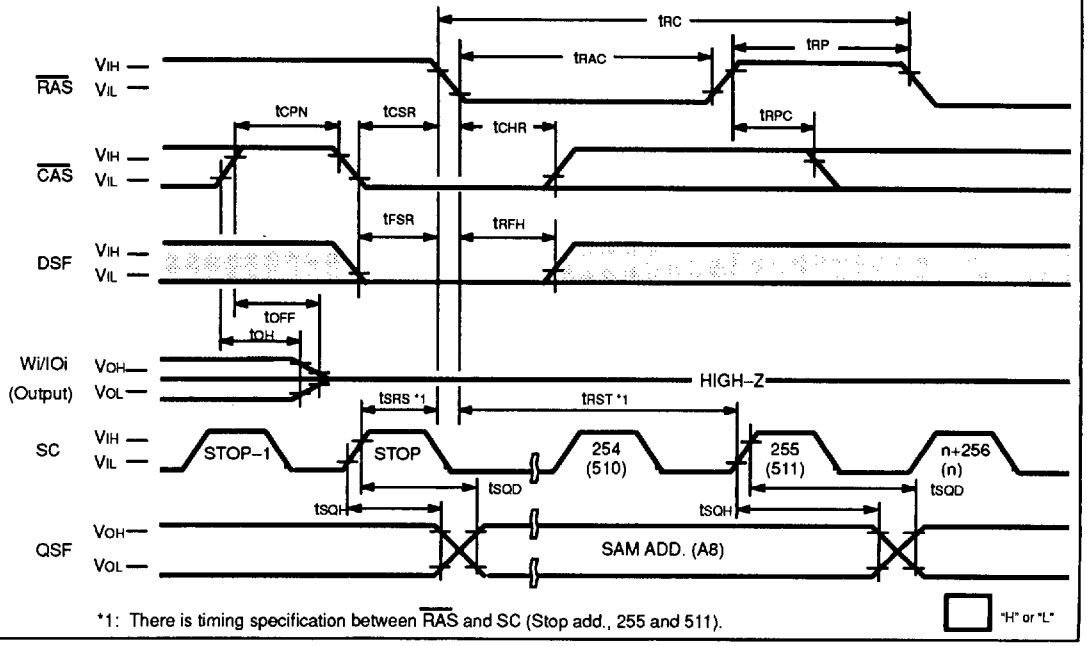


Fig. 18 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (OPTION RESET)

(A0 to A8, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and W0/IO0 to W7/IO7 (input) = "H" or "L")



*1: There is timing specification between $\overline{RAS}$ and SC (Stop add., 255 and 511).

Fig. 19 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (STOP REGISTER SET)

($\overline{DT}/\overline{OE}$ and W0/IO0 to W7/IO7 (input) = "H" or "L")

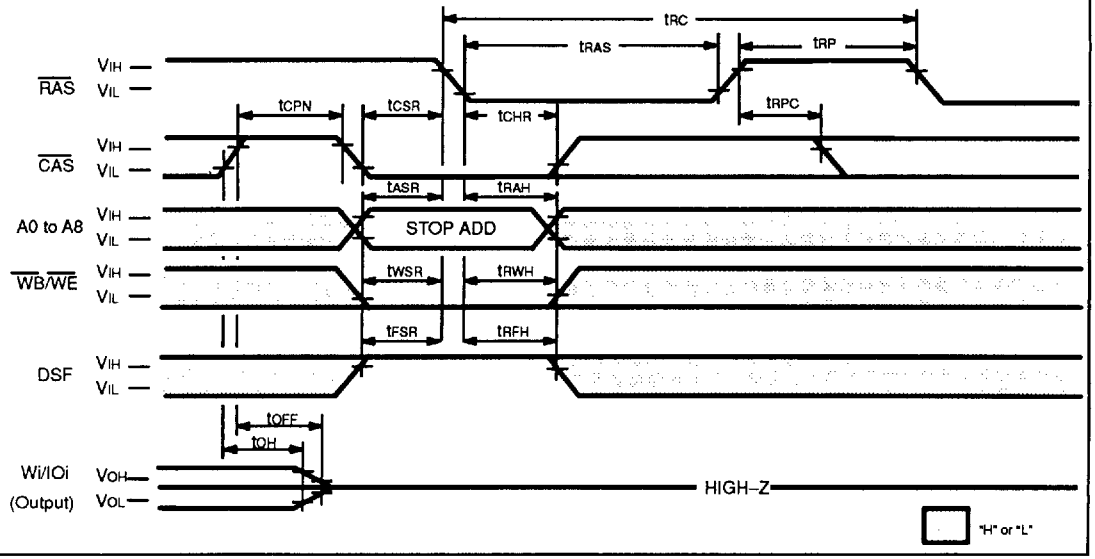


Fig. 20 – $\overline{CAS}$-$\overline{BEFORE}$-$\overline{RAS}$ $\overline{REFRESH}$ CYCLE (OPTION NO-RESET)

(A0 to A8, $\overline{DT}/\overline{OE}$ and W0/IO0 to W7/IO7 (input) = "H" or "L")

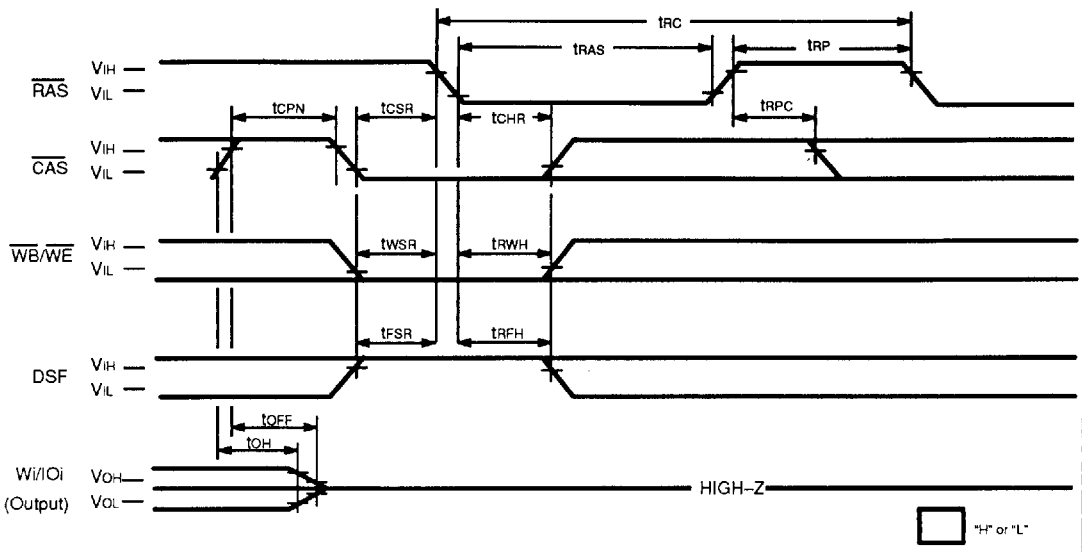
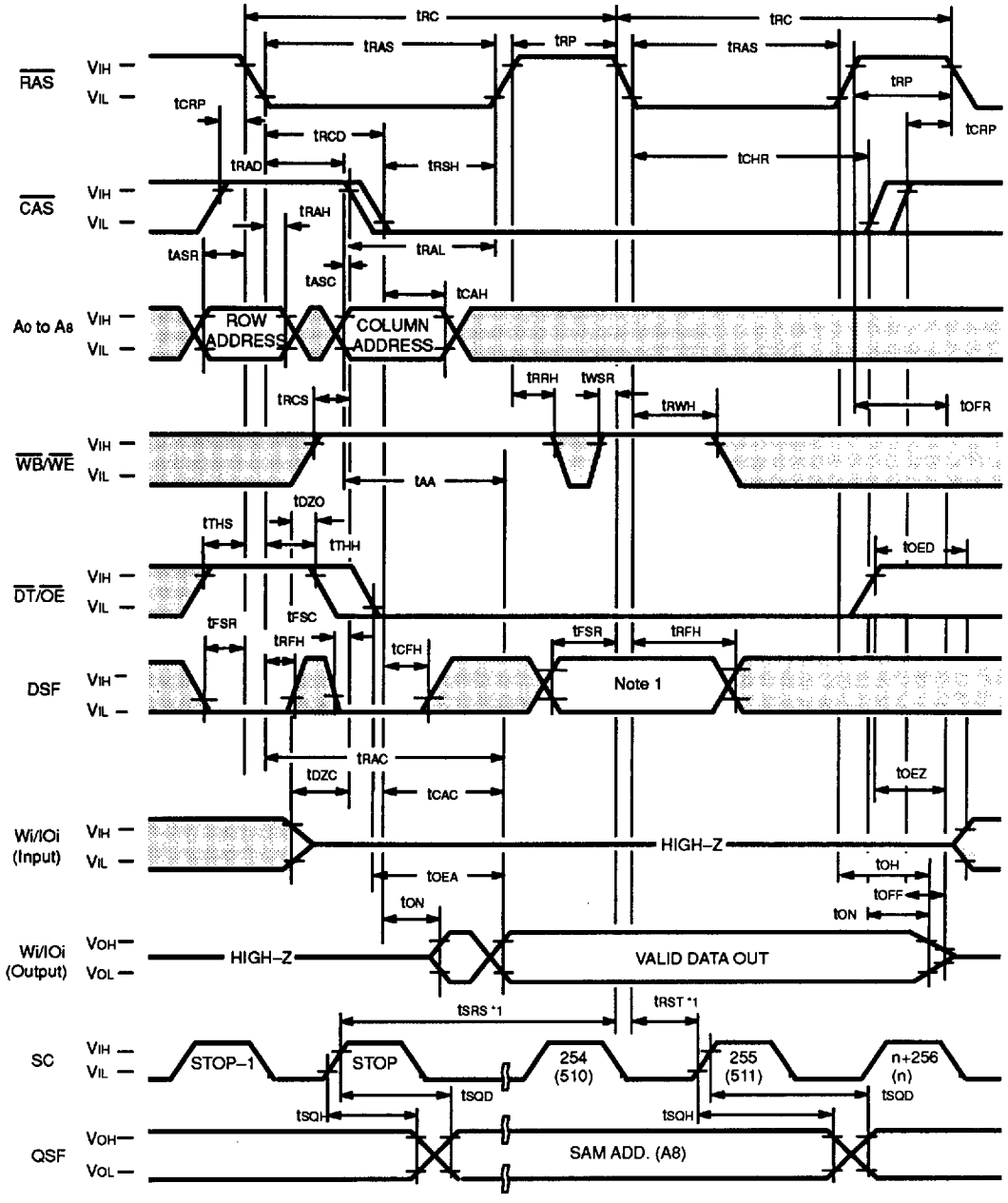


Fig. 21 – HIDDEN REFRESH CYCLE

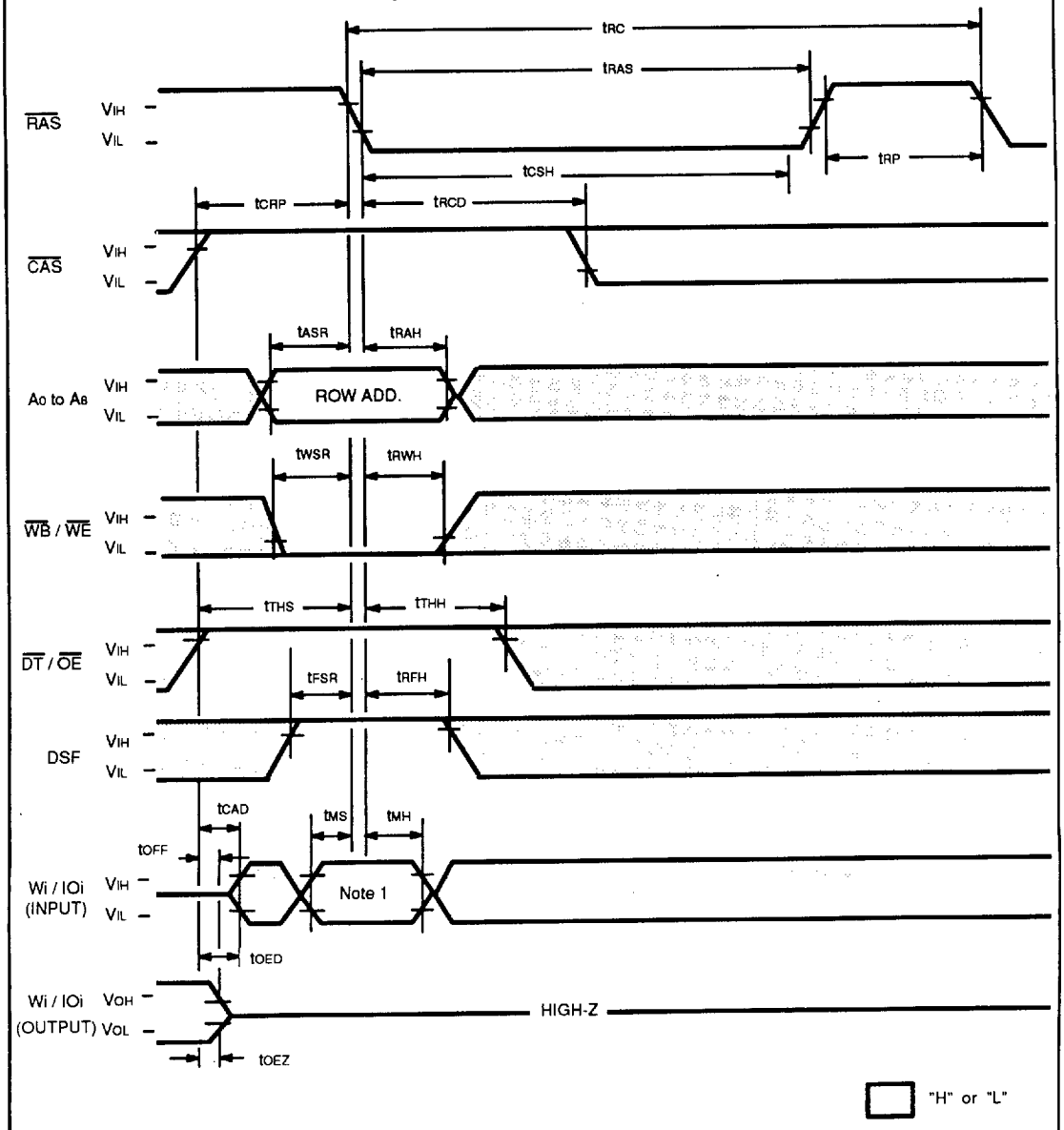


Note 1: When DSF = "H", there is option no-reset. When DSF = "L", there is option reset.

*1: In option reset mode, there is timing specification between $\overline{RAS}$ and SC (Stop add., 255 and 511).

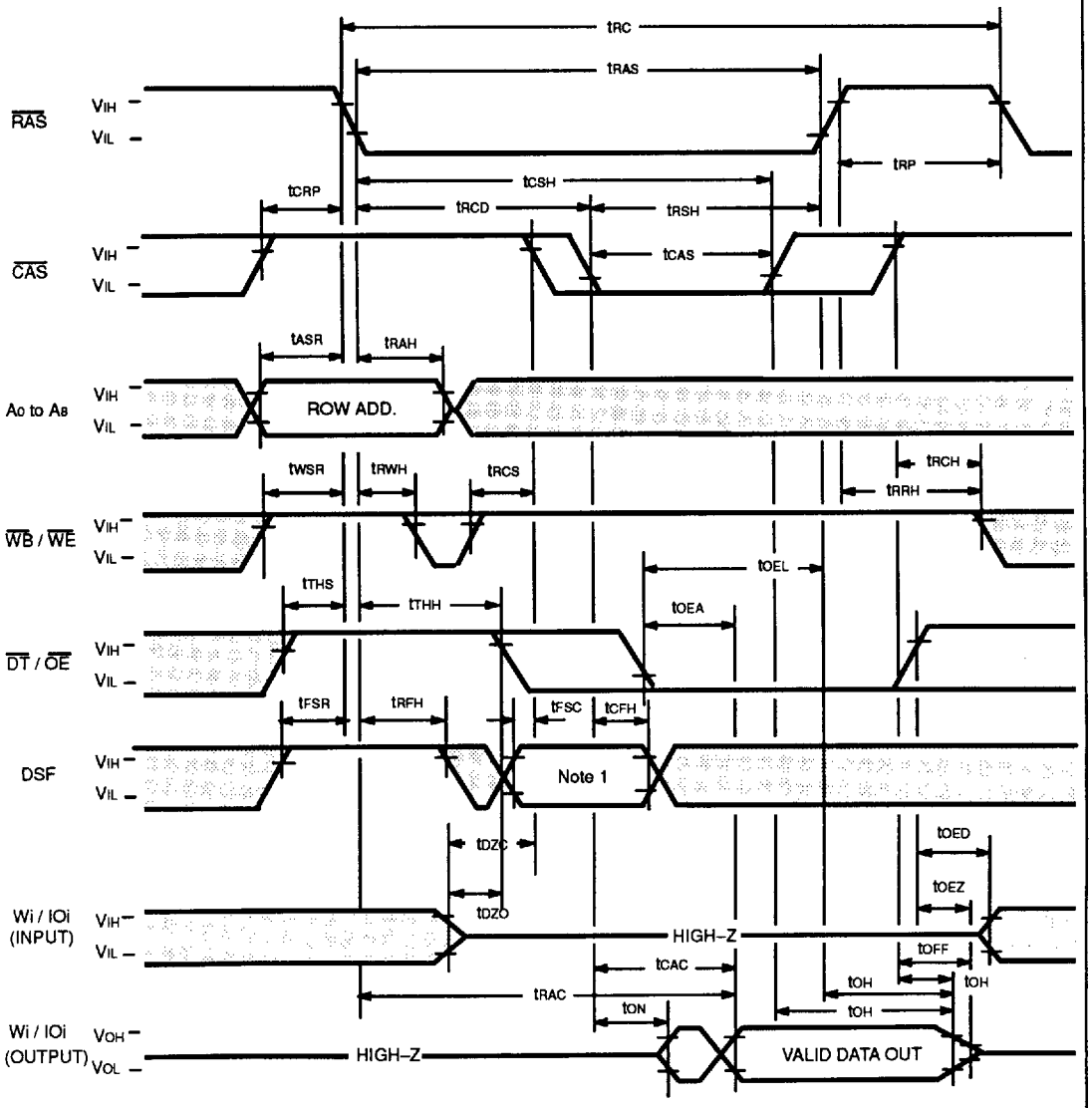
"H" or "L"

Fig. 22 – FLASH WRITE CYCLE



Note 1: When flash write cycle, write-per-bit mode is entered. And flash write operation can be inhibited by data of Wi/IOi in case of new mask mode and by data of mask register in case of old mask mode.

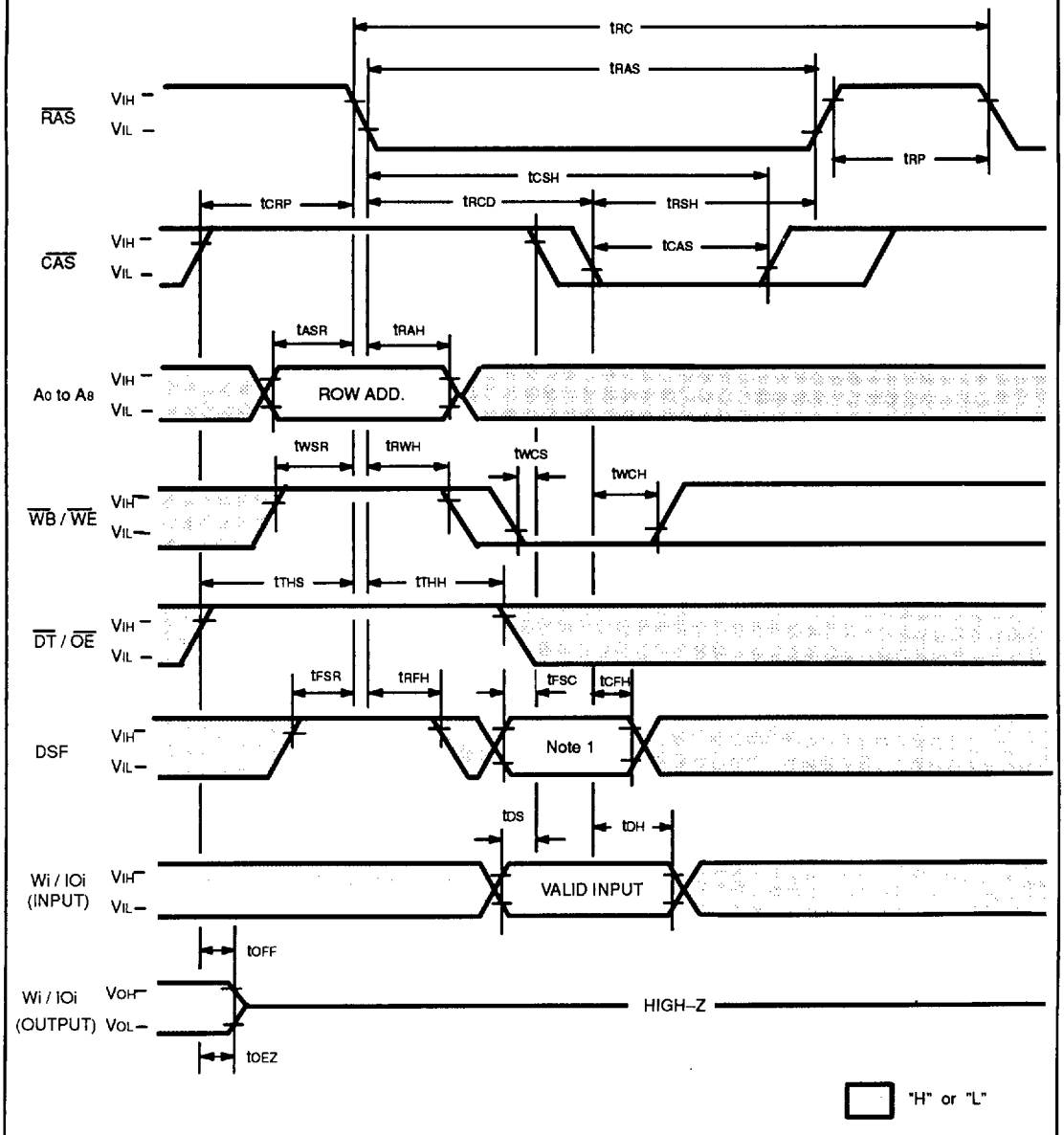
Fig. 23 – REGISTER READ CYCLE



Note 1: When DSF = "H", a state of color register is outputted.
When DSF = "L", a state of mask register is outputted.

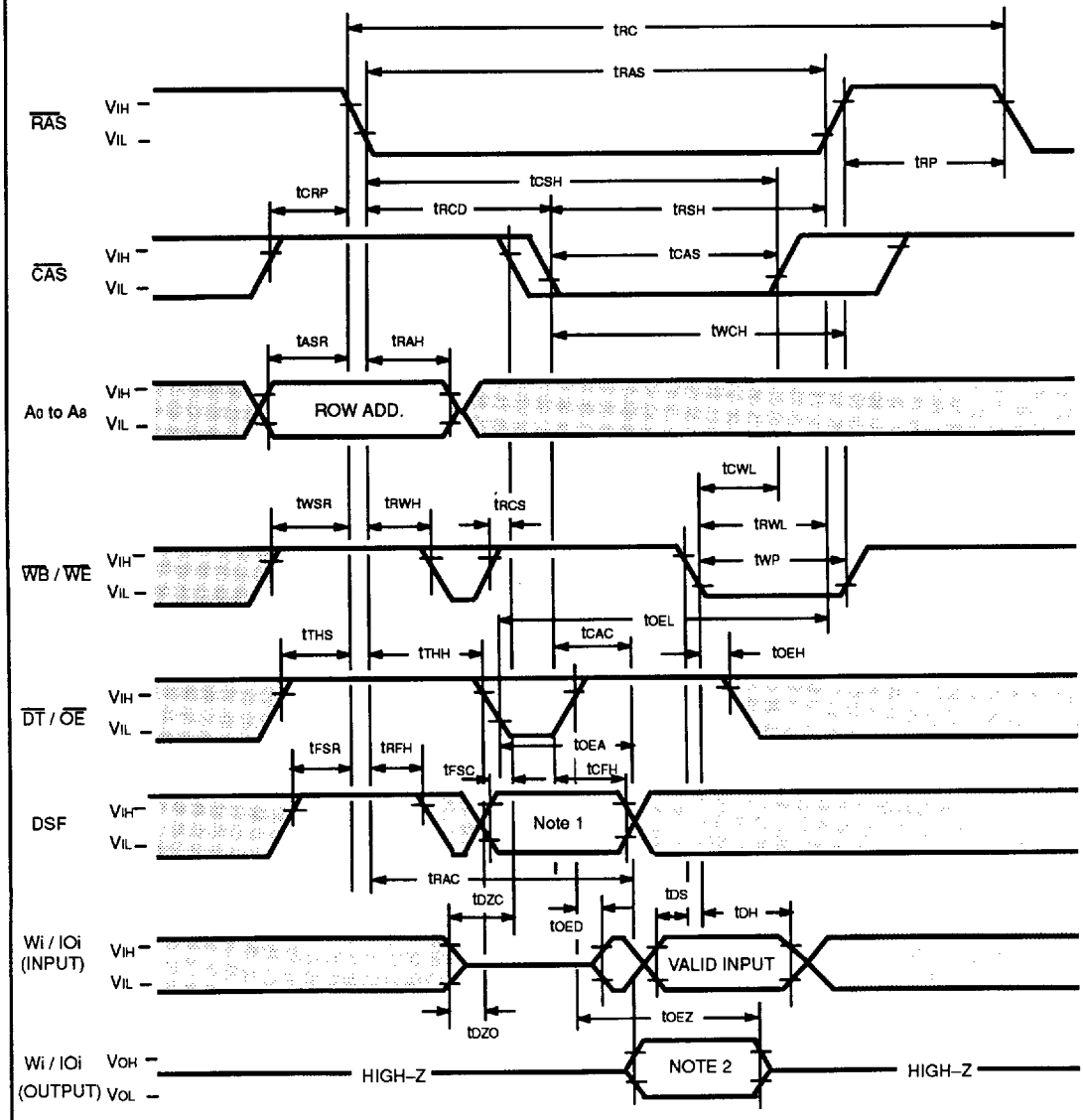
4

Fig. 24 – LOAD REGISTER CYCLE (EARLY WRITE)



Note 1: When DSF = "H", a data on Wi/IOi is written into the color register.
When DSF = "L", a data on Wi/IOi is written into the mask register.

Fig. 25 – LOAD REGISTER CYCLE ($\overline{OE}$ CONTROL)



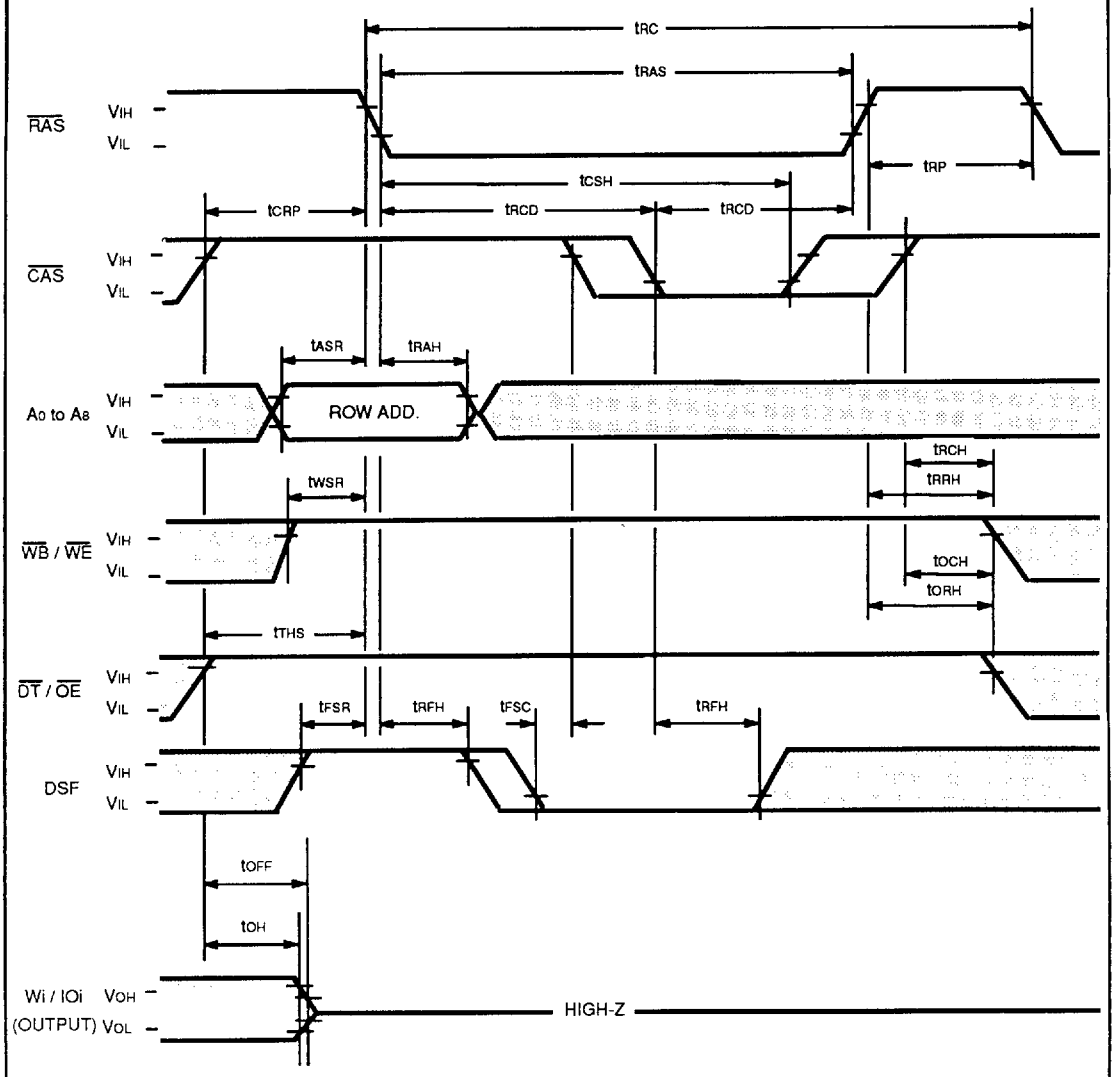
"H" or "L"

Note 1: When DSF = "H", a data on Wi/IOi is written into the color register.
When DSF = "L", a data on Wi/IOi is written into the mask register.

Note 2: If DT/OE is kept "H" during the cycle, WI/O is placed in the high-impedance state.

4

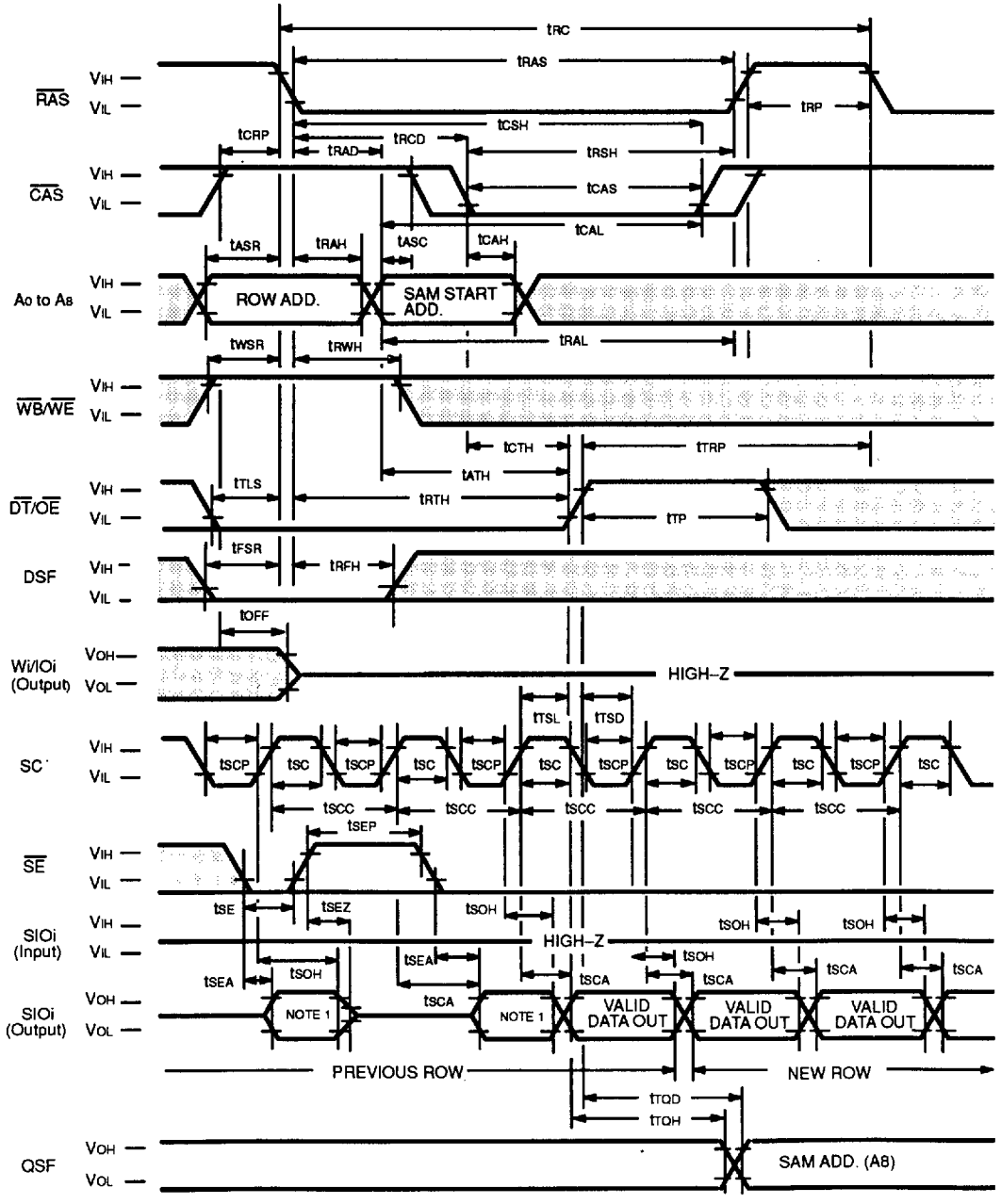
Fig. 26 – MASK MODE RESET CYCLE



Note: Mask mode is changed to new mask mode by execution of this cycle.

"H" or "L"

Fig. 27 – READ TRANSFER CYCLE (When the previous transfer was for read operation)

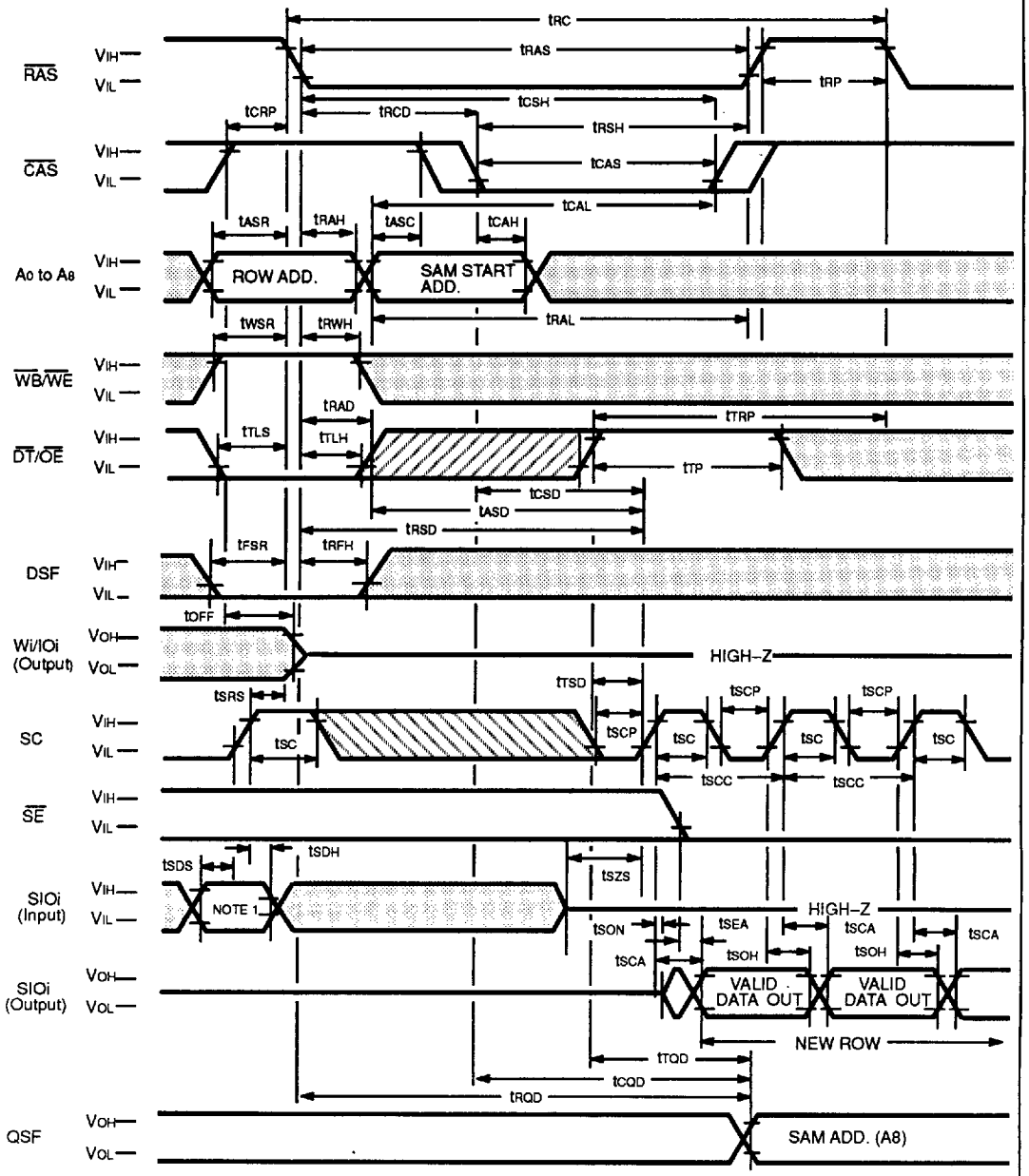


Note 1: If $\overline{SE}$ is low, the valid data is output when both tSCA and tSEA are met.

"H" or "L"

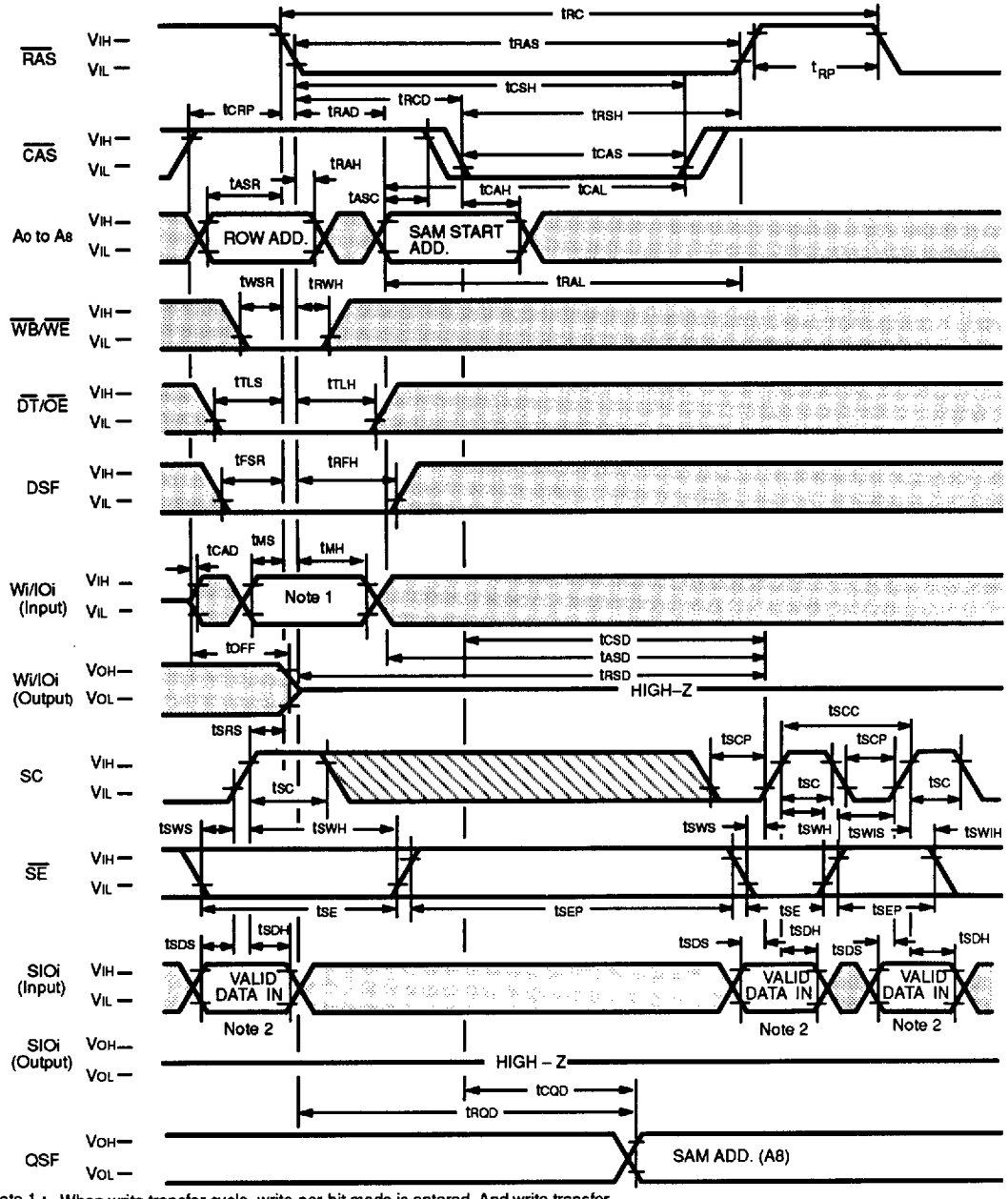
4

Fig. 28 – READ TRANSFER CYCLE (When the previous transfer was for write operation)



Note 1: If $\overline{SE}$ is low and the previous cycle was for serial write operation, the input data must be valid here.

Fig. 29 – WRITE TRANSFER CYCLE (When the previous transfer was for write operation)



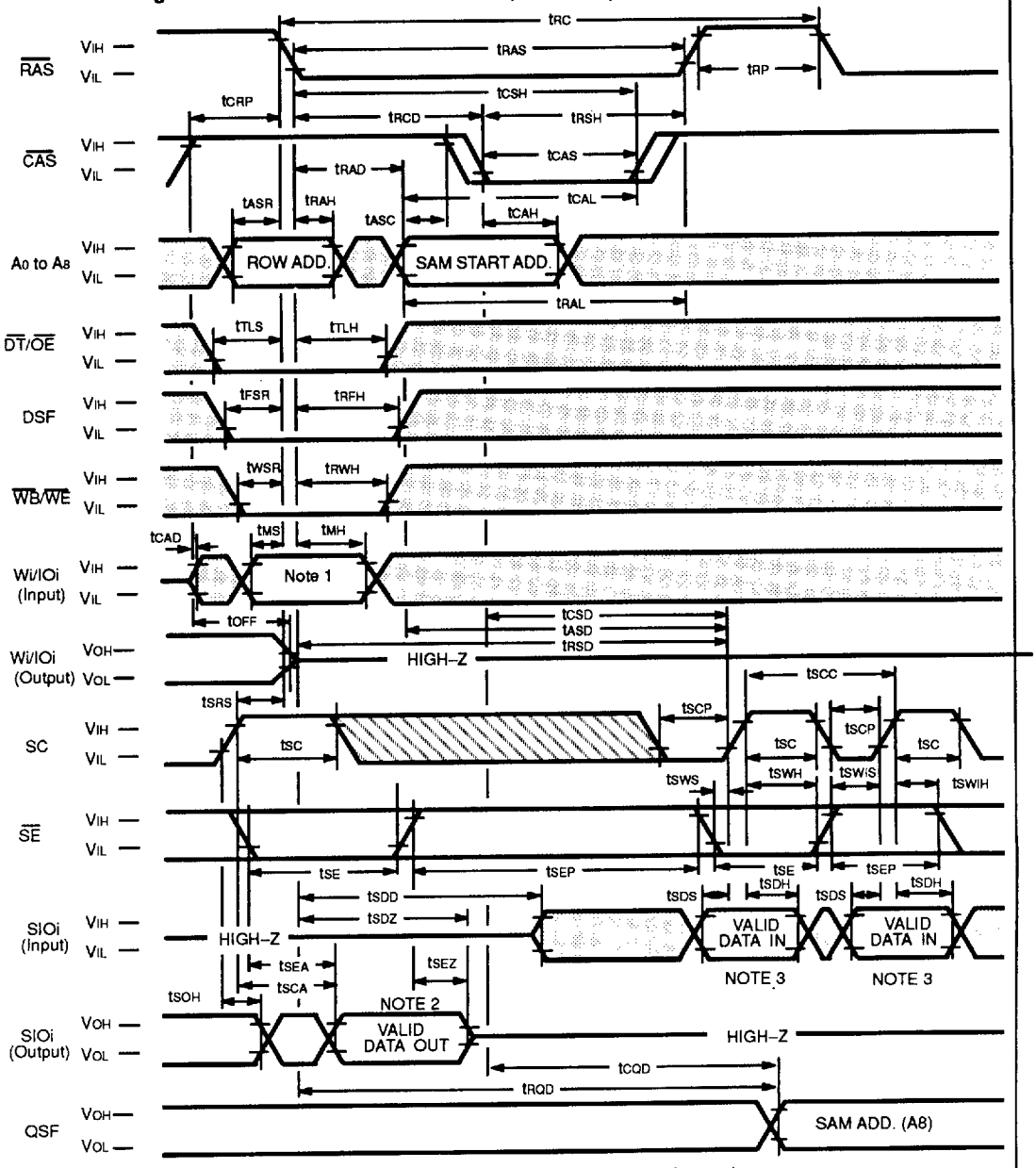
Note 1 : When write transfer cycle, write-per-bit mode is entered. And write transfer operation can be inhibited by data of Wi/IOi in case of new mask mode and by data of mask register in case of old mask mode.

Note 2 : If $\overline{SE}$ = "H", no data can be written to SAM.

Rising edges inhibited "H" or "L"

4

Fig. 30 – WRITE TRANSFER CYCLE (When the previous transfer was for read operation)



Note 1 : When write transfer cycle, write-per-bit mode is entered. And write transfer operation can be inhibited by data of Wi/IOi in case of new mask mode and by data of mask register in case of old mask mode.

Note 2 : If $\overline{SE}$ is "L", the valid data is output when both tSCA and tSEA are met.

Note 3 : If $\overline{SE}$ is "H", no data can be written to SAM.

Rising edges inhibited

"H" or "L"

Fig. 31 – SPLIT READ TRANSFER CYCLE

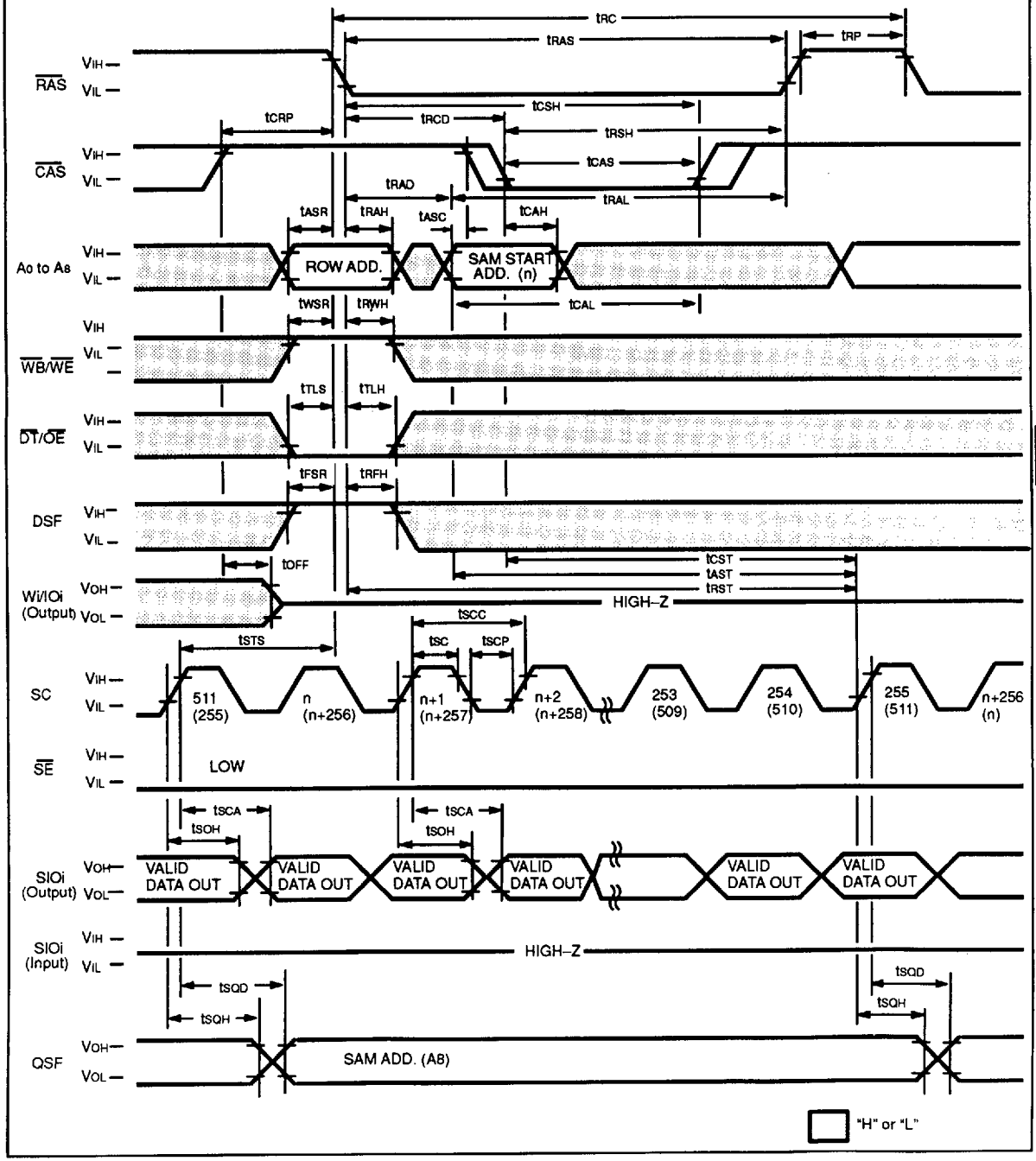
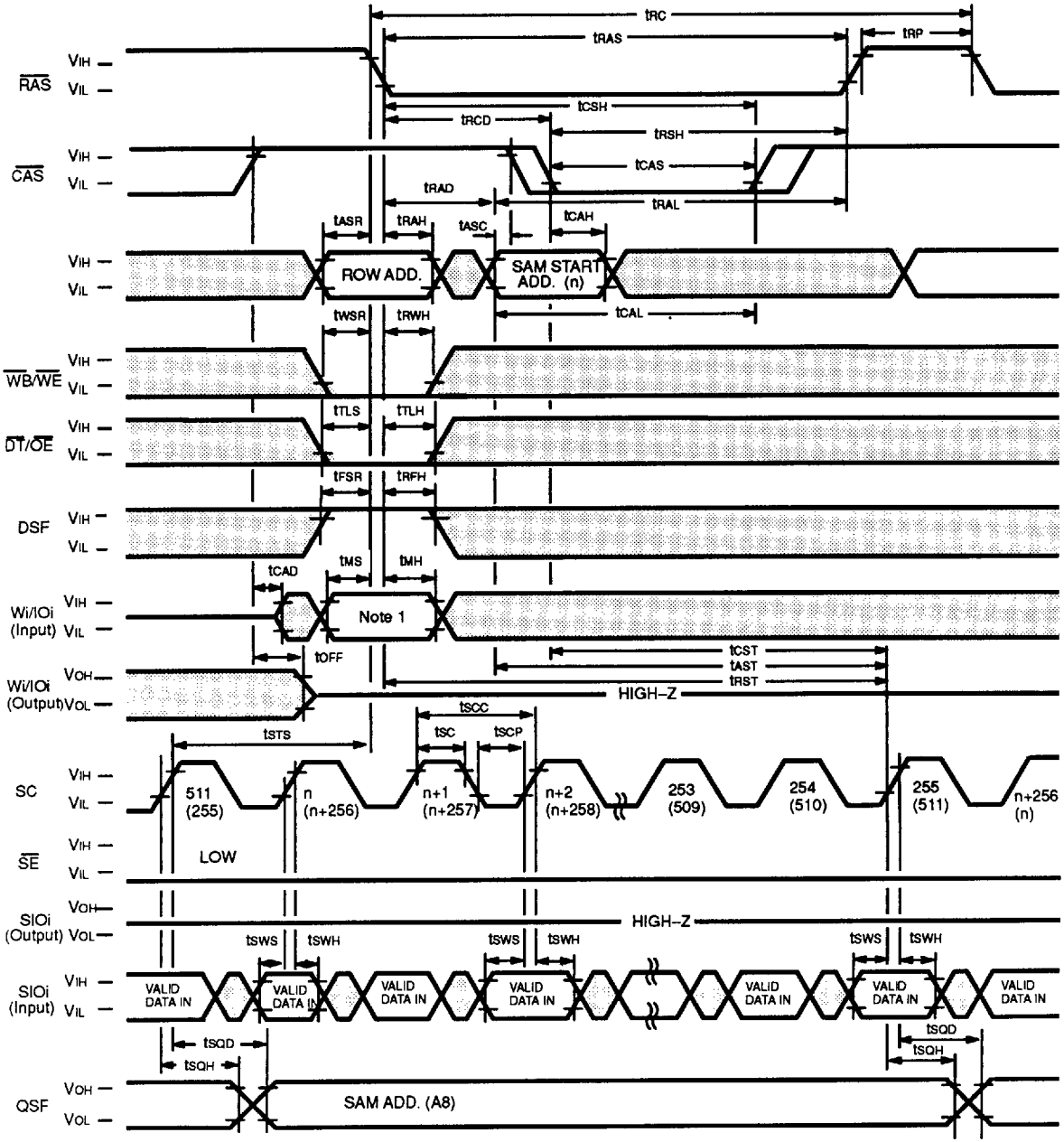


Fig. 32 – MASKED SPLIT WRITE TRANSFER CYCLE



Note 1: When split write transfer cycle, write-per-bit mode is entered. And split write transfer can be inhibited by data of Wi/IOi in case of new mask mode and by data of mask register in case of new mask mode.

"H" or "L"

Fig. 33 – SERIAL READ CYCLE

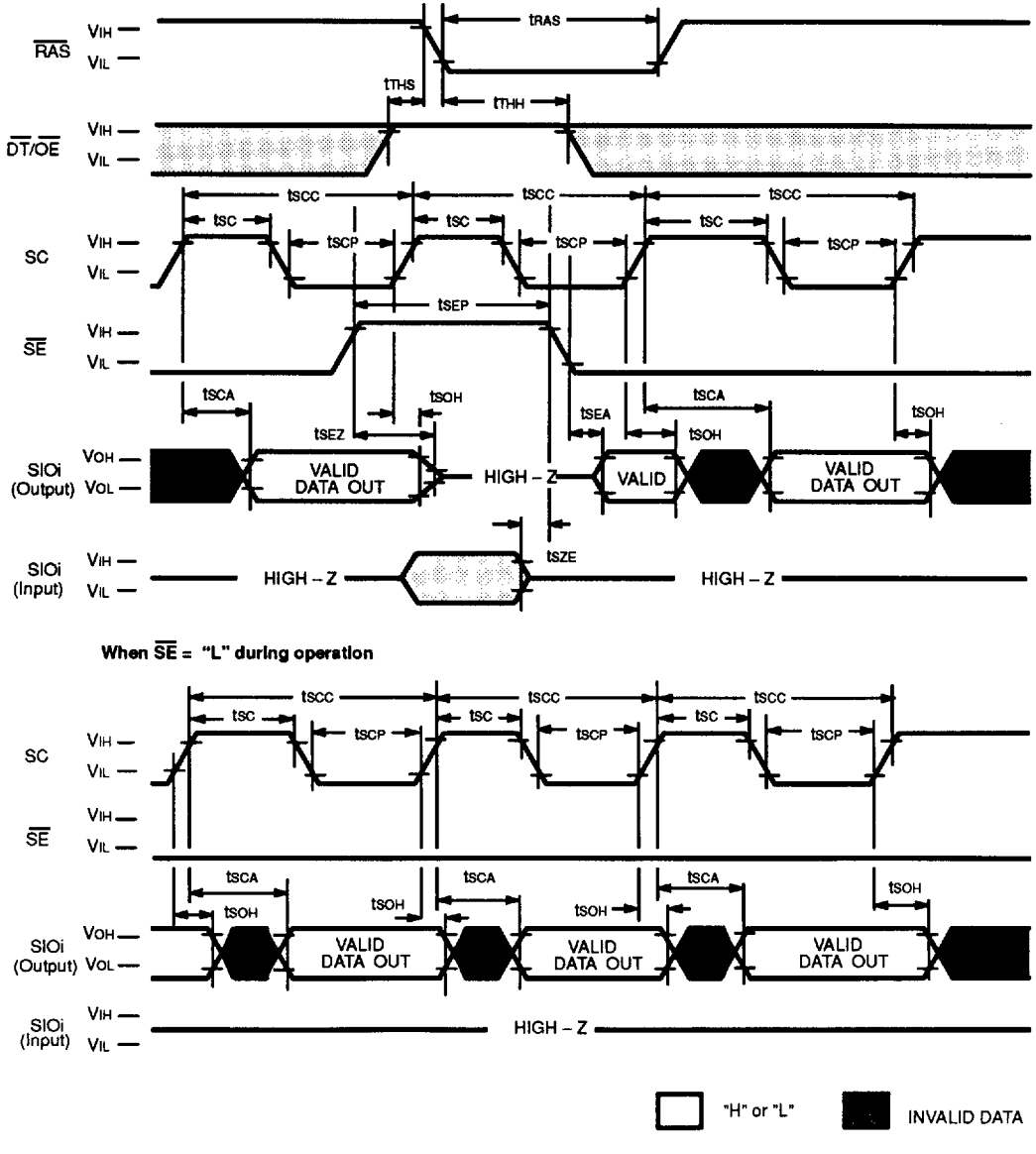
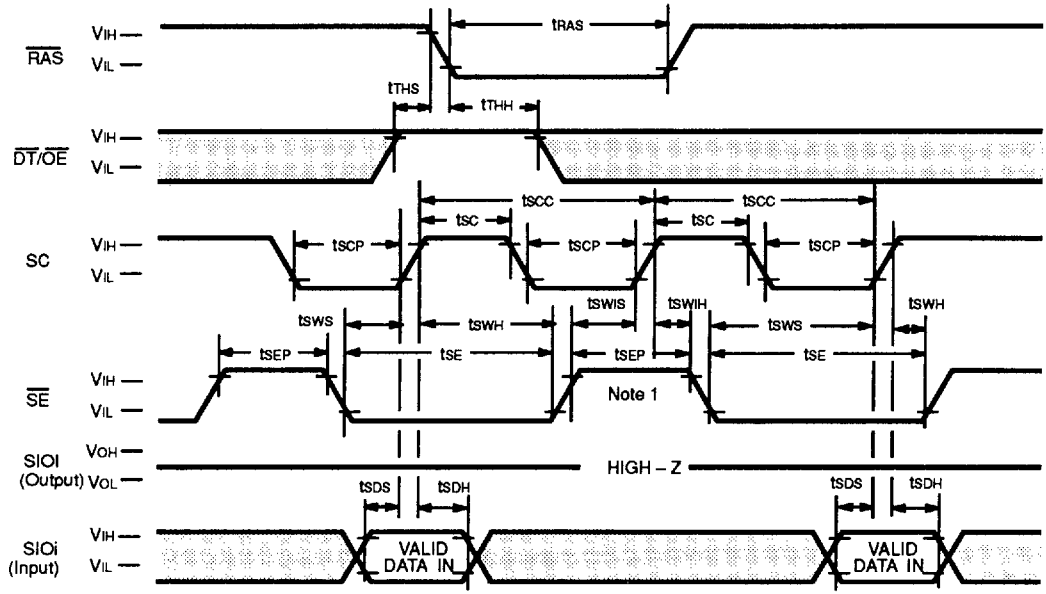
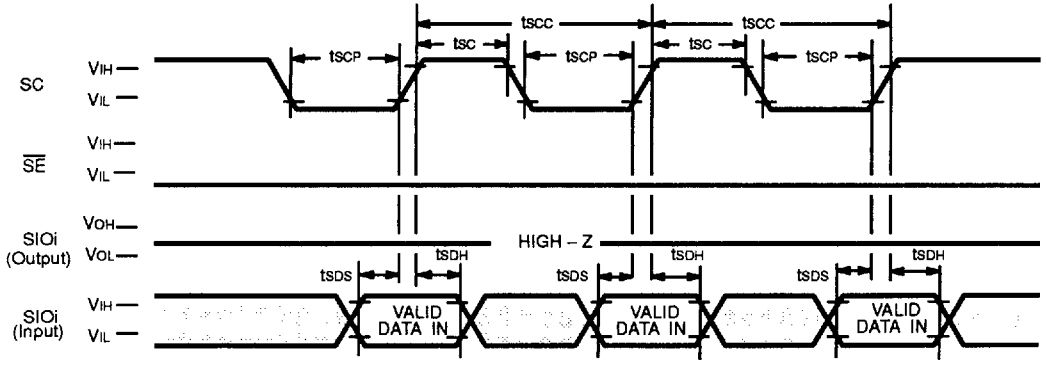


Fig. 34 – SERIAL WRITE CYCLE



When $\overline{SE}$ = "L" during operation

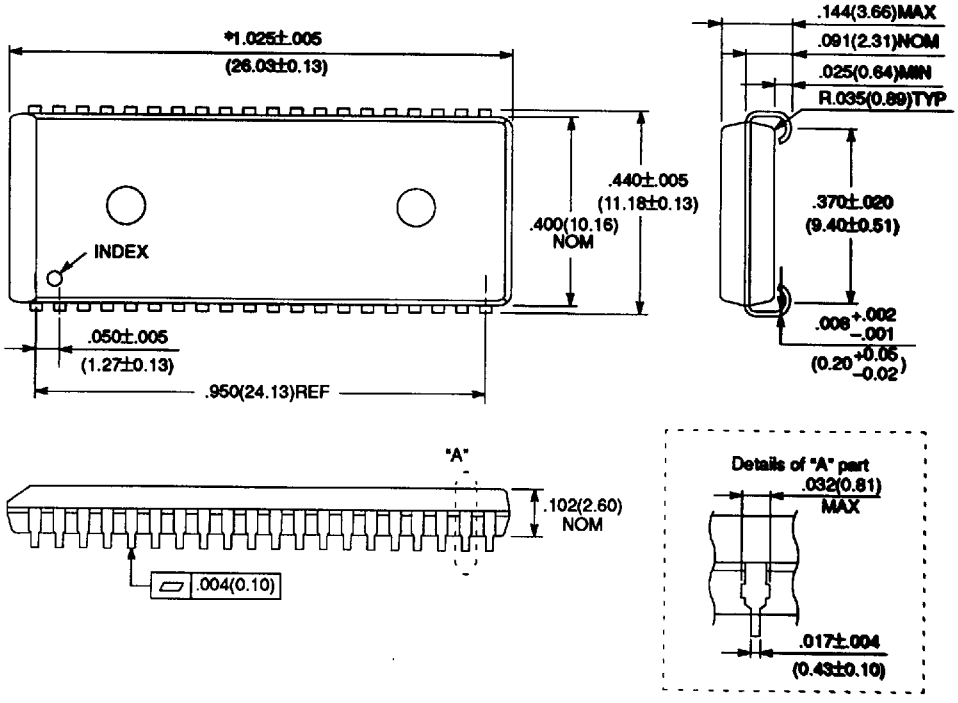


Note 1: When $\overline{SE}$ = "H" at rising edge of SC, writes to cells of SAM is inhibited.

"H" or "L"

PACKAGE DIMENSIONS

40-LEAD SOJ (PLASTIC LEADED CHIP CARRIER)
(CASE No.: LCC-40P-M01)



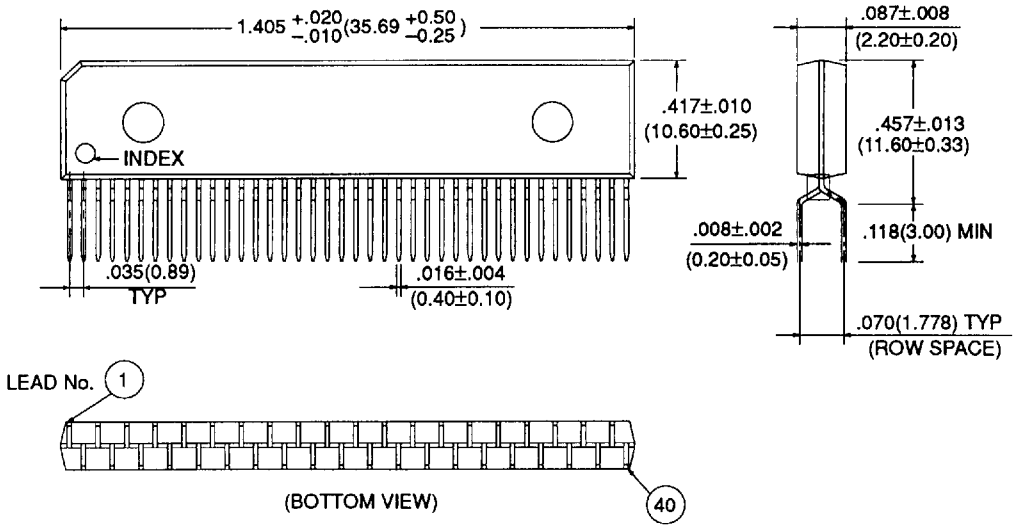
*Resin protrusion. (Each side:.006(0.15)MAX.)

Dimensions in inches (millimeters)

4

PACKAGE DIMENSIONS (Continued)

40-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE
(CASE No.: ZIP-40P-M02)

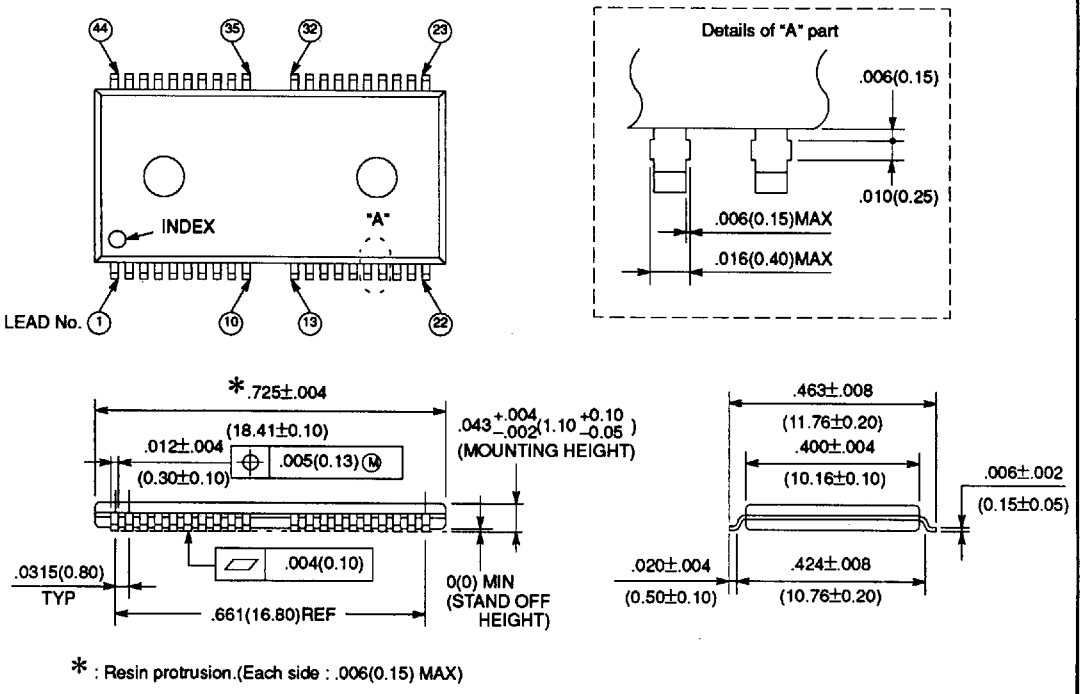


Dimensions in inches (millimeters)

4

PACKAGE DIMENSIONS (Continued)

44–LEAD PLASTIC SMALL OUTLINE PACKAGE
(CASE No.: FPT–44P–M07)



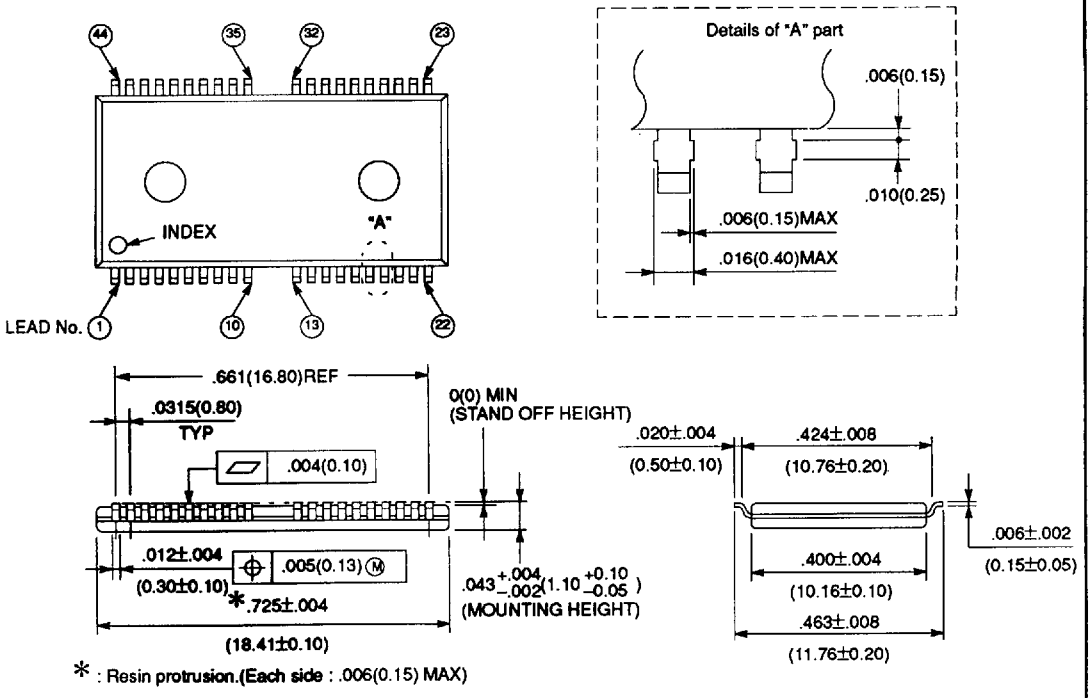
* : Resin protrusion.(Each side : .006(0.15) MAX)

Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS (Continued)

44-LEAD PLASTIC SMALL OUTLINE PACKAGE
(CASE No.: FPT-44P-M08)



Dimensions in inches (millimeters)