Signetics

FAST 74F595
Shift Register

FAST Products

8-Bit Shift Register with Output Latches (3-state)
Product Specification

FEATURES

- **Low noise, no switching feedthru current**
- **Controlled output edge rates**
- **High impedance PNP base inputs for reduced loading (20μA in High and Low states)**
- **8-bit serial-in, parallel-out shift register with storage**
- **3-state outputs**
- **Shift register has direct clear**
- **Guaranteed shift frequency-DC to 100MHz**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F595	130MHz	65mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F595N
16-Pin Plastic SO	N74F595D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_S	Serial data input	1.0/0.033	20μA/20μA
SHCP	Shift register clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
STCP	Storage register clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
$\overline{SHR}$	Shift register reset input (active Low)	1.0/0.033	20μA/20μA
$\overline{OE}$	Output enable input (active Low)	1.0/0.033	20μA/20μA
Q_S	Serial expansion output	50/33	1.0mA/20mA
Q_0 - Q_7	Data outputs	150/40	3.0mA/24mA

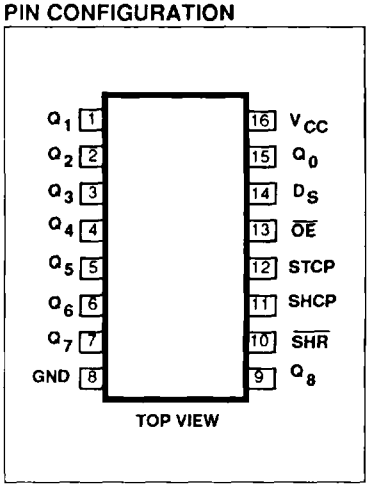
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F595 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct overriding clear, serial input and serial output pins for cascading. Both the shift register and storage register clocks are positive edge-triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

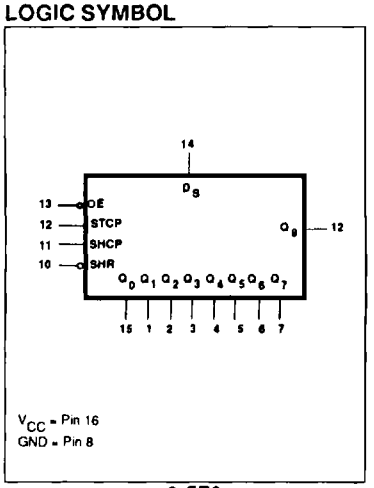
This device uses patented circuitry to control system noise and internal ground bounce. This is done by eliminating switching feedthru current and controlling both Low-to-High and High-to-Low slew rates.

PIN CONFIGURATION



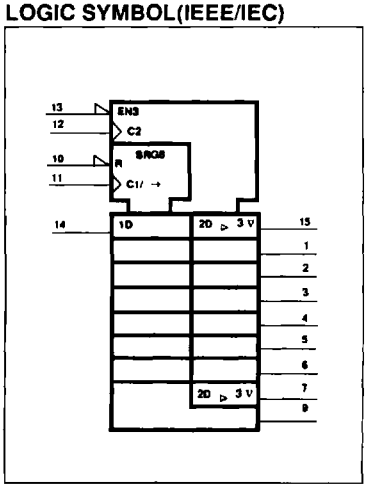
TOP VIEW

LOGIC SYMBOL

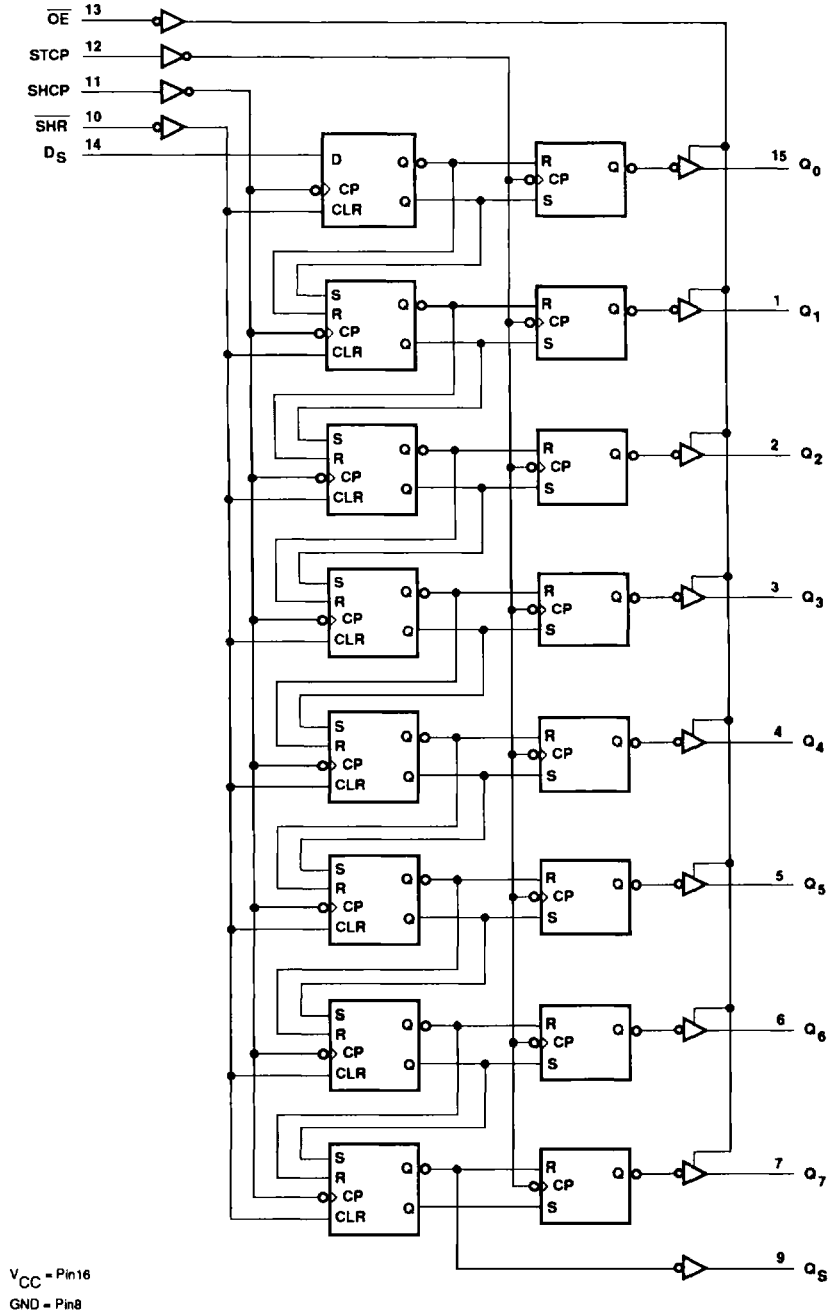


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT - FUNCTION TABLE

INPUTS					INTERNAL SHIFT REGISTERS		INTERNAL STORAGE REGISTER	OUTPUTS		OPERATING MODE
$\overline{OE}$	$\overline{SHR}$	SHCP	STCP	D_S	O_0	$O_1 - O_7$	$Q_0 - Q_7$	$Q_0 - Q_7$	Q_S	
H	H	↕	↕	X	O_0	$O_1 - O_7$	$Q_0 - Q_7$	Z	Q_7	No change
H	L	X	↕	X	L_0	L	$Q_0 - Q_7$	Z	L	Clear shift register, hold latch
L	L	X	↕	X	L_0	L	$Q_0 - Q_7$	$Q_0 - Q_7$	L	
H	H	↑	↕	d_s	D_s	$o_0 - o_6$	$Q_0 - Q_7$	Z	o_6	Shift
L	H	↑	↑	d_s	D_s	$o_0 - o_6$	$Q_0 - Q_7$	$Q_0 - Q_7$	o_6	
H	H	↕	↑	X	O_0	$O_1 - O_7$	$o_0 - o_7$	Z	Q_7	Store
L	H	↕	↑	X	O_0	$O_1 - O_7$	$o_0 - o_7$	$o_0 - o_7$	Q_7	
H	H	↑	↑	d_s	D_s	$o_0 - o_6$	$o_0 - o_7$*	Z	o_6	Store, then shift
L	H	↑	↑	d_s	D_s	$o_0 - o_6$	$o_0 - o_7$*	$o_0 - o$*	o_6	

H = High voltage level.
L = Low voltage level.
X = Don't care.
Z = High impedance.
$d_s(o_n)$ = Lower case letters indicate the state of the referenced input (or output) one set up time prior to the Low-to-High clock transition.
↑ = Low-to-High clock transition.
↕ = Not a Low-to-High clock transition.
* = When clocking both SHCP and STCP simultaneously the Shift Register state will always be one clock pulse ahead of the Storage Register.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	Q_S	40	mA
		$Q_0 - Q_7$	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_S			-1	mA
		$Q_0 - Q_7$			-3	mA
I_{OL}	Low-level output current	Q_S			20	mA
		$Q_0 - Q_7$			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Q_S	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		Q_0- Q_7		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	Q_S	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=20mA	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
		Q_0- Q_7		I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	mA
I_{OZH}	Off state output current, High-level voltage applied	Q_0- Q_7 only	V_{CC} =MAX, V_O=2.7V					50	µA
I_{OZL}	Off state output current, Low-level voltage applied	Q_0- Q_7 only	V_{CC} =MAX, V_O=0.5V					-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				55	85	mA
		I_{CCL}					70	105	mA
		I_{CCZ}					65	105	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

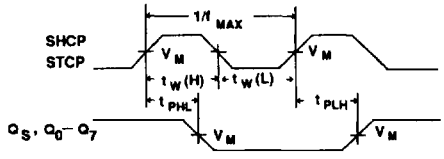
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	115	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Q_S	Waveform 1	6.0 2.5	8.0 4.5	10.5 7.5	5.0 2.5	12.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Q_0- Q_7	Waveform 1	5.5 3.0	8.0 5.0	11.0 8.0	4.5 3.0	13.0 8.5	ns
t_{PHL}	Propagation delay $\overline{SHR}$ to Q_S	Waveform 2	3.5	5.5	8.0	3.0	8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_0- Q_7	Waveform 5 Waveform 6	3.5 3.0	5.5 5.5	9.0 8.5	2.5 2.5	10.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_0- Q_7	Waveform 5 Waveform 6	2.0 4.0	4.0 6.0	7.0 9.0	1.5 3.0	8.5 10.0	ns

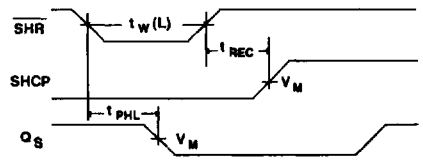
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_S to SHCP	Waveform 3	2.0 2.0			2.5 2.5		ns
t_h(H) t_h(L)	Hold time, High or Low D_S to SHCP	Waveform 3	0 0			0 0		ns
t_s(L)	Setup time, Low $\overline{SHR}$ to STCP	Waveform 3	4.5			5.0		ns
t_s(H)	Setup time, High SHCP to STCP	Waveform 4	4.5			5.0		ns
t_w(H) t_w(L)	SHCP Pulse width, High or Low	Waveform 1	3.5 4.0			4.0 4.0		ns
t_w(H) t_w(L)	STCP Pulse width, High or Low	Waveform 1	4.0 3.0			4.0 3.5		ns
t_w(L)	$\overline{SHR}$ Pulse width, Low	Waveform 2	3.0			3.0		ns
t_{REC}	Recovery time $\overline{SHR}$ to SHCP	Waveform 2	3.0			3.0		ns

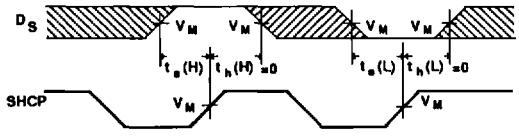
AC WAVEFORMS



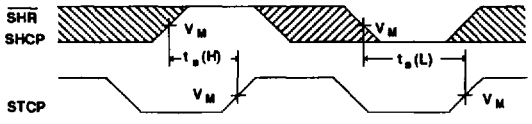
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



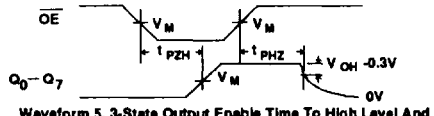
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



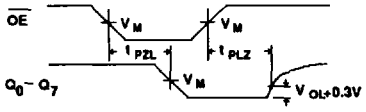
Waveform 3. Data Setup And Hold Times



Waveform 4. Setup And Hold Times



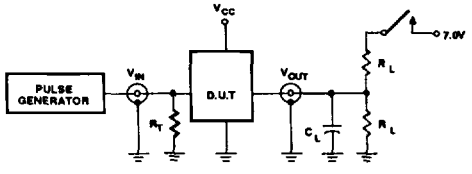
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

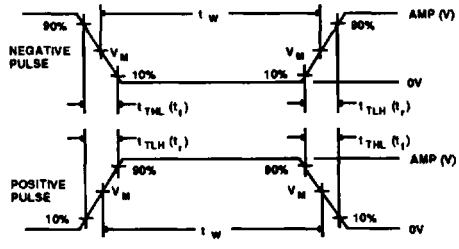
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns