

74AC/ACT11253
Dual 4-Input Multiplexer;
3-State

Product Specification

ACL Products

FEATURES

- 3-State outputs for bus interface and multiplex expansion
- Separate 3-State Output Enable Inputs
- Common Select Inputs
- Output capability: ± 24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50 Ω Incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11253 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11253 device provides two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common select inputs (S_0, S_1). When the individual output enable ($1OE, 2OE$) inputs of the 4-input multiplexers are High, the outputs are forced to a high impedance state.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS		TYPICAL		UNIT
		$T_A = 25^\circ\text{C}; \text{GND} = 0\text{V}; V_{CC} = 5.0\text{V}$		AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay $1I_n, 2I_n$ to nY	$C_L = 50\text{pF}$		4.7	6.5	ns
C_{PD}	Power dissipation capacitance per multiplexer ¹	$f = 1\text{MHz};$	Enabled	35	41	pF
		$C_L = 50\text{pF}$	Disabled	11	15	
C_{IN}	Input capacitance	$V_I = 0\text{V or } V_{CC}$		3.5	3.5	pF
C_{OUT}	Output capacitance	$V_I = 0\text{V or } V_{CC}; \text{Disabled}$		8	8	pF
I_{LATCH}	Latch-up current	Per Jeduc JC40.2 Standard 17		500	500	mA

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

f_I = input frequency in MHz, C_L = output load capacitance in pF,

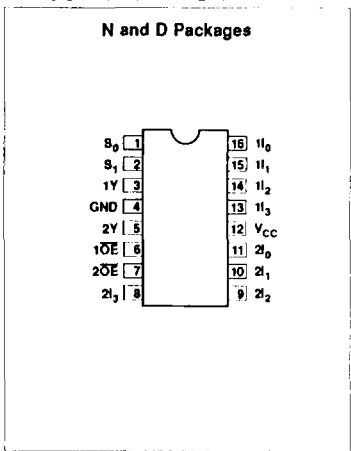
f_O = output frequency in MHz, V_{CC} = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

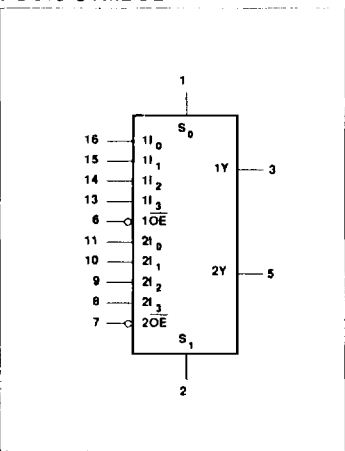
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11253N 74ACT11253N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11253D 74ACT11253D

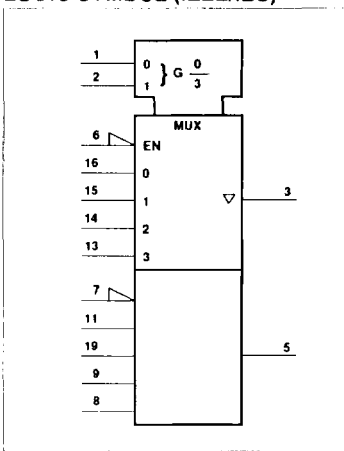
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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The 74AC/ACT11253 devices are the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two select inputs.

The '11253 is the non-inverting version of the '11353.

PIN DESCRIPTION

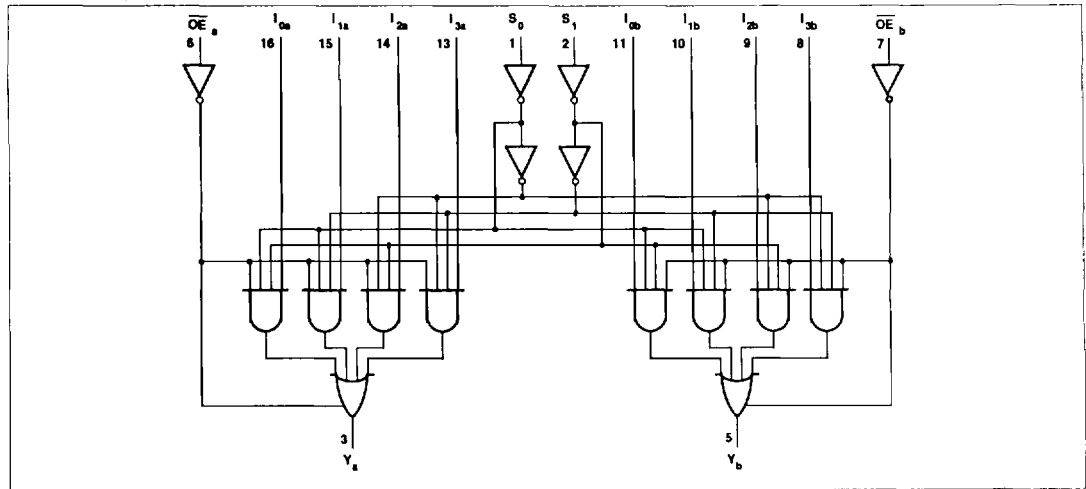
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2	S_0, S_1	Common select inputs
16, 15, 14, 13	$1I_0 - 1I_3$	Port A data inputs
11, 10, 9, 8	$2I_0 - 2I_3$	Port B data inputs
6	$1\overline{OE}$	Port A output enable input
7	$2\overline{OE}$	Port B output enable input
3, 5	$1Y, 2Y$	3-State data outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS							OUTPUT
$\overline{OE}_n$	s_1	s_0	I_{0n}	I_{1n}	I_{2n}	I_{3n}	Y_n
H	X	X	X	X	X	X	Z
L	L	L	X	X	X	X	L
L	L	L	H	X	X	X	H
L	L	H	X	L	X	X	L
L	L	H	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
L	H	H	X	X	X	L	L
L	H	H	X	X	X	H	H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
Z = High-impedance "OFF" state

LOGIC DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11253			74ACT11253			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0 ¹	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta V/\Delta t$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK} or V_I	DC input diode current ²	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
I_{OK} or V_O	DC output diode current ²	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current per output pin	$V_O = 0$ to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C: derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C: derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC} V	74AC11253				74ACT11253				UNIT	
				T _A = +25°C		T _A = -40°C to +85°C		T _A = +25°C		T _A = -40°C to +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V _{IH}	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V _{IL}	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V _{OH}	High-level output voltage	V _I = V _{IL} or V _{IH}	I _{OH} = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I _{OH} = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
			I _{OH} = -24mA	5.5	4.94		4.8		4.94		4.8		
				5.5			3.85				3.85		
V _{OL}	Low-level output voltage	V _I = V _{IL} or V _{IH}	I _{OL} = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
				5.5		0.1		0.1		0.1			0.1
			I _{OL} = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36			0.44
			I _{OL} = 24mA	5.5		0.36		0.44		0.36			0.44
				5.5				1.65					1.65
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I _{OZ}	3-State output off-state current	V _I = V _{IL} or V _{IH} , V _O = V _{CC} or GND	5.5		±0.5		±5.0		±0.5		±5.0	μA	
I _{CC}	Quiescent supply current	V _I = V _{CC} or GND, I _O = 0	5.5		8.0		80		8.0		80	μA	
ΔI _{CC}	Supply current, TTL inputs High ²	One input at 3.4V, other inputs at V _{CC} or GND	5.5						0.9		1.0	mA	

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
- This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

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AC ELECTRICAL CHARACTERISTICS AT 3.3V $\pm 0.3V$

SYMBOL	PARAMETER	WAVEFORM	74AC11253						UNIT
			T _A = +25°C			T _A = -40°C to +85°C			
			Min	Typ	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation delay I _n to nY	1	1.5 1.5	6.8 7.0	8.3 8.8	1.5 1.5	9.3 9.6	ns	
t _{PLH} t _{PHL}	Propagation delay nS to nY	1	1.5 1.5	7.1 7.5	9.7 10.1	1.5 1.5	11.0 11.4	ns	
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.5 1.5	4.8 5.8	6.2 7.4	1.5 1.5	6.8 8.2	ns	
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.5 1.5	5.0 5.2	6.3 6.5	1.5 1.5	6.7 6.9	ns	

AC ELECTRICAL CHARACTERISTICS AT 5.0V $\pm 0.5V$

SYMBOL	PARAMETER	WAVEFORM	74AC11253						UNIT
			T _A = +25°C			T _A = -40°C to +85°C			
			Min	Typ	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation delay I _n to nY	1	1.5 1.5	4.5 4.8	5.9 6.3	1.5 1.5	6.6 6.9	ns	
t _{PLH} t _{PHL}	Propagation delay nS to nY	1	1.5 1.5	4.9 5.2	7.0 7.3	1.5 1.5	7.9 8.2	ns	
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.5 1.5	3.4 4.0	4.6 5.3	1.5 1.5	5.1 5.8	ns	
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.5 1.5	4.7 4.6	6.0 5.9	1.5 1.5	6.3 6.2	ns	

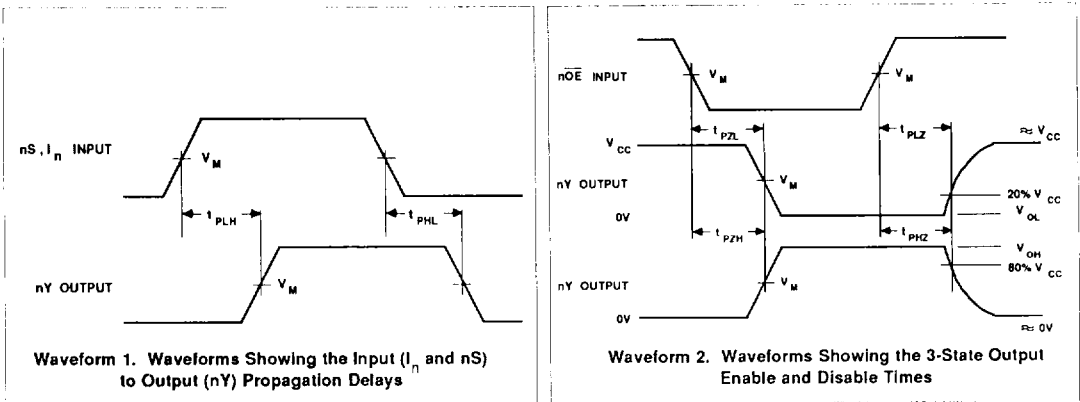
AC ELECTRICAL CHARACTERISTICS AT 5.0V $\pm 0.5V$

SYMBOL	PARAMETER	WAVEFORM	74ACT11253					UNIT
			T _A = +25°C			T _A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay I _n to nY	1	1.5 1.5	5.7 7.2	7.4 10.5	1.5 1.5	8.3 11.7	ns
t _{PLH} t _{PHL}	Propagation delay nS to nY	1	1.5 1.5	6.8 9.1	9.8 12.6	1.5 1.5	11.0 14.3	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.5 1.5	5.0 4.8	7.6 7.3	1.5 1.5	8.5 8.1	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.5 1.5	6.4 5.9	8.6 7.4	1.5 1.5	9.2 7.8	ns

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AC WAVEFORMS



WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC}$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0V$ $V_M = 1.5V$	$V_M = 50\% V_{CC}$

TEST CIRCUIT

