SN74ALS679
12-BIT ADDRESS COMPARATOR

- **12-Bit Address Comparator With Enable**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs**
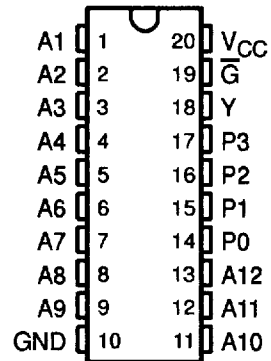
description

This 12-bit address comparator simplifies addressing of memory boards and/or other peripheral devices. The four P inputs are normally hardwired with a preprogrammed address. An internal decoder determines what input information applied to the A inputs must be low or high to cause a low state at the Y output. For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

This device features an enable ($\overline{G}$) input. When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high, regardless of the A and P inputs.

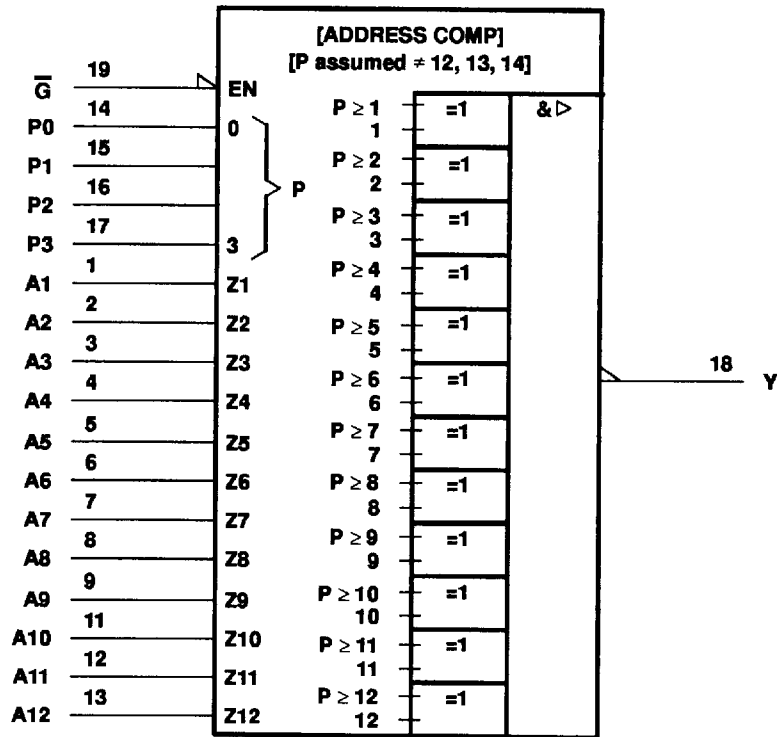The SN74ALS679 is characterized for operation from 0°C to 70°C.

DW OR N PACKAGE
(TOP VIEW)

```
         _____
A1  [ 1      20 ] V_CC
A2  [ 2      19 ] Ḡ
A3  [ 3      18 ] Y
A4  [ 4      17 ] P3
A5  [ 5      16 ] P2
A6  [ 6      15 ] P1
A7  [ 7      14 ] P0
A8  [ 8      13 ] A12
A9  [ 9      12 ] A11
GND [ 10     11 ] A10
```

FUNCTION TABLE

$\overline{G}$	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	OUTPUT Y
									INPUTS								
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	H	H	H	L	L†
L	H	H	L	H	L	L	L	L	L	L	L	L	L	H	H	L	L†
L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L†
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L									All other combinations								H
H									Any combination								H

† The three shaded rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for these combinations in which P = 12, 13, and 14. If symbols valid for all combinations are required, starting with the fourth exclusive-OR from the bottom, change P ≥ 9 to P = 9 . . . 11/13 . . . 15, P ≥ 10 to P = 10/11/14/15, and P ≥ 11 to P = 11/15.

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SN74ALS679
12-BIT ADDRESS COMPARATOR

logic symbol†

	[ADDRESS COMP] [P assumed ≠ 12, 13, 14]

Pin assignments shown in diagram:

$\overline{G}$ 19 → EN

P0 14 → 0 ⎫
P1 15 → ⎪
P2 16 → ⎬ P
P3 17 → 3 ⎭

A1 1 → Z1
A2 2 → Z2
A3 3 → Z3
A4 4 → Z4
A5 5 → Z5
A6 6 → Z6
A7 7 → Z7
A8 8 → Z8
A9 9 → Z9
A10 11 → Z10
A11 12 → Z11
A12 13 → Z12

Comparator blocks:

$P \geq 1$ — 1
$P \geq 2$ — 2
$P \geq 3$ — 3
$P \geq 4$ — 4
$P \geq 5$ — 5
$P \geq 6$ — 6
$P \geq 7$ — 7
$P \geq 8$ — 8
$P \geq 9$ — 9
$P \geq 10$ — 10
$P \geq 11$ — 11
$P \geq 12$ — 12

Each with =1, combined into & ▷ → 18 Y

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)

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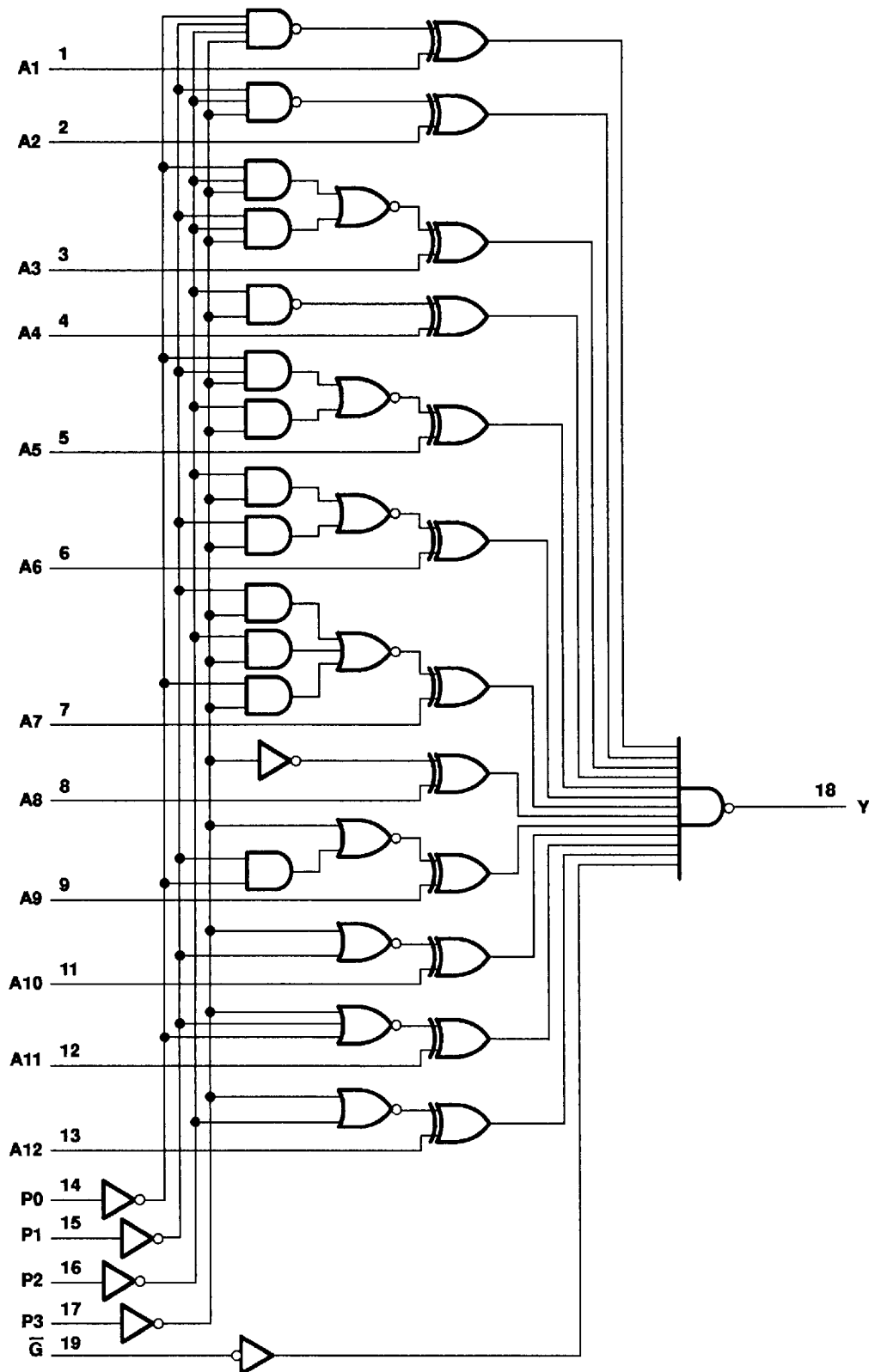
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			–1.5	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -0.4$ mA	$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V,	$I_{OH} = -2.6$ mA	2.4	3.2		
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA		0.25	0.4	V
		$I_{OL} = 24$ mA		0.35	0.5	
I_I	$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20	μA
I_{IL}	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			–0.1	mA
I_O§	$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	–30		–112	mA
I_{CC}	$V_{CC} = 5.5$ V			17	28	mA

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5$ V to 5.5 V, $C_L = 50$ pF, $R_L = 500$ Ω, T_A = MIN to MAX¶		UNIT
			MIN	MAX	
t_{PLH}	Any P	Y	4	25	ns
t_{PHL}			8	35	
t_{PLH}	Any A	Y	5	22	ns
t_{PHL}			5	30	
t_{PLH}	$\overline{G}$	Y	3	13	ns
t_{PHL}			5	25	

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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APPLICATION INFORMATION

The SN74ALS679 can be wired to recognize any one of 2^{12} addresses. The number of lows in the address determines the input pattern for the P inputs. The system address lines that are low in the address to be recognized are connected to the lowest-numbered A inputs of the address comparator. The system address lines that are high are connected to the highest-numbered A inputs.

For example, assume the comparator is to enable a device when the 12-bit system address is:
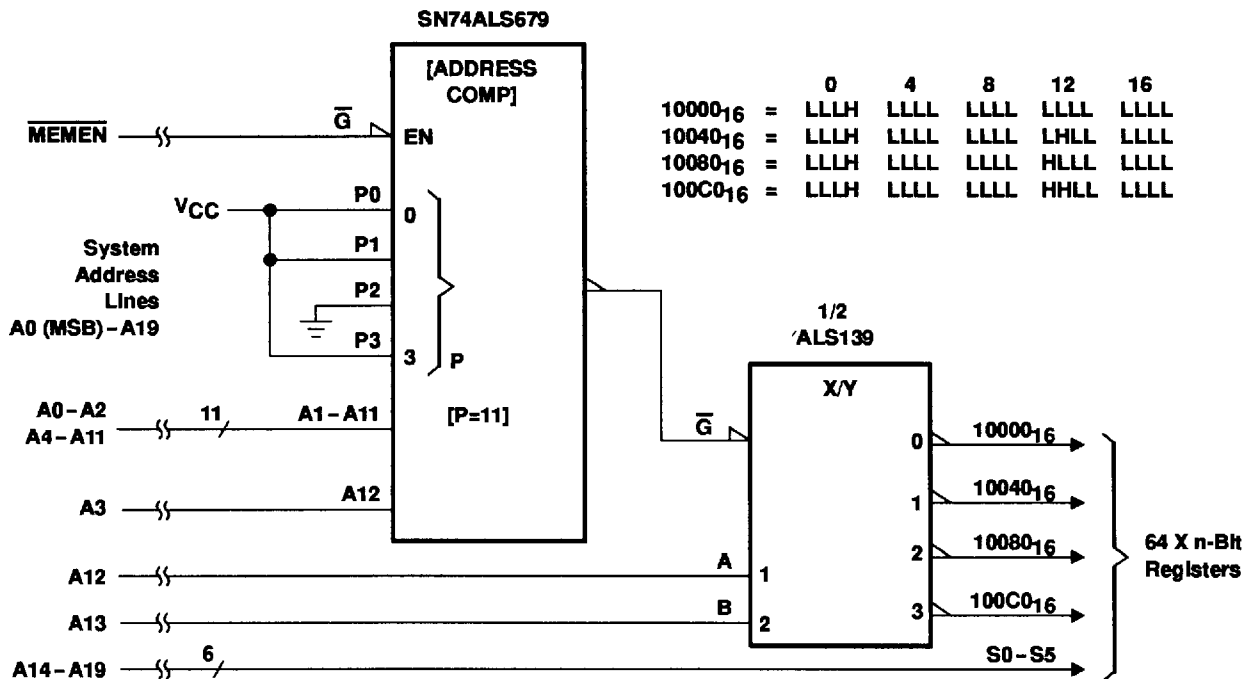
A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	H	H

Because the address contains four lows and eight highs, the following connections are made:

- P3 to 0 V, P2 to V_{CC}, P1 to 0 V, and P0 to 0 V
- System address lines A9, A8, A5, and A4 to comparator inputs A1 through A4 in any convenient order
- The remaining eight system address lines to comparator inputs A5 through A12 in any convenient order

The output provides an active-low enabling signal.

Figure 1 is a register-bank decoder that examines the 14 most significant bits (A0 through A13) of a 20-bit address to select banks corresponding to the hex addresses 10000, 10040, 10080, and 100C0.
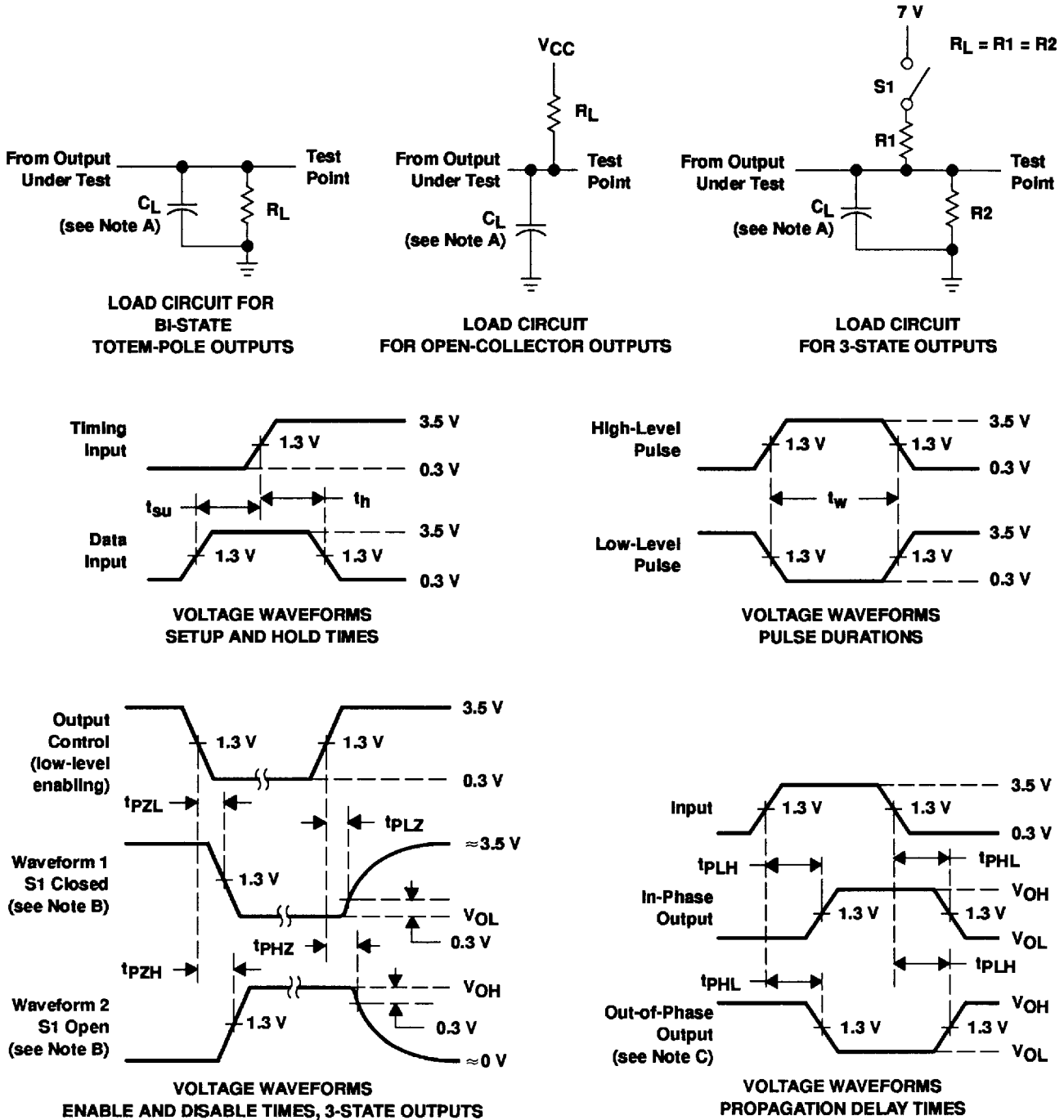

Figure 1. Register-Bank Decoder

PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES

LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

LOAD CIRCUIT FOR 3-STATE OUTPUTS

$R_L = R1 = R2$

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PULSE DURATIONS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
  B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
  Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
  D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
  E. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

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