Features

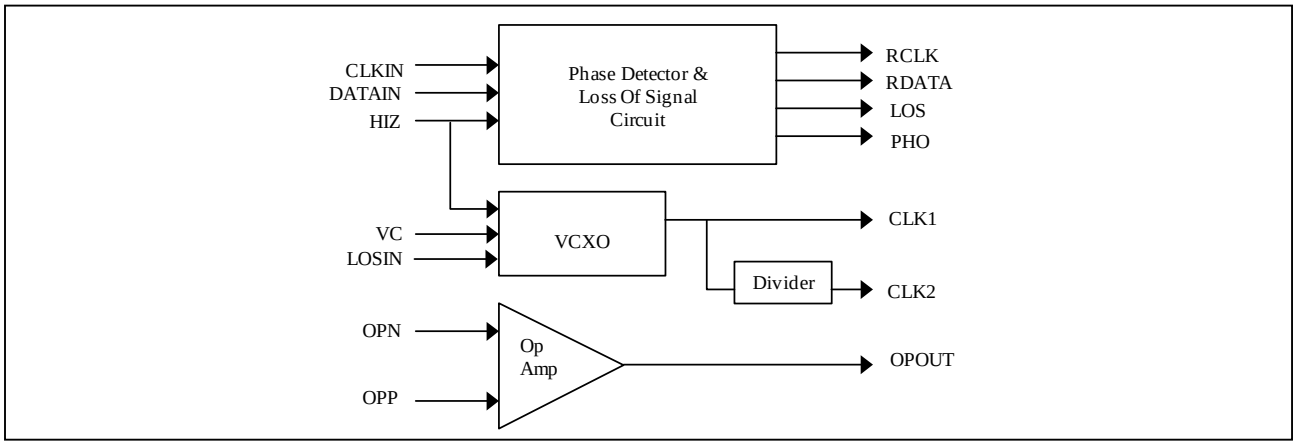
- PLL with quartz stabilized VCXO
- Loss of signals alarm
- Return to nominal clock upon LOS
- Input data rates from 8 kb/s to 65 Mb/s
- Tri-state output
- User defined PLL loop response
- NRZ data compatible
- Single +5.0V power supply

Description

The device is composed of a phase-lock loop with an integrated VCXO for use in clock recovery, data re-timing, frequency translation and clock smoothing applications in telecom and datacom systems.

Crystal Frequencies Supported: 12.000~50.000 MHz.

Block Diagram



Ordering Information

PT7V4050 T B C G A 49.408 / 12.352

Device Type
16-pin clock recovery module

Package Leads
T: Thru-Hole
G: Surface Mount

CLK2 Divider
A: Divide by 2 E: Divide by 32
B: Divide by 4 F: Divide by 64
C: Divide by 8 G: Divide by 128
D: Divide by 16 H: Divide by 256
K: Disable

Temperature Range
C: 0°C to 70°C
T: -40°C to 85°C

C: ±20ppm
F: ±32ppm
G: ±50ppm
H: ±100ppm

A: 5.0V supply voltage
B: 3.3V supply voltage

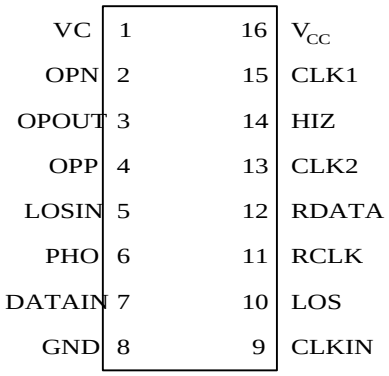
CLK1 Frequency

CLK2 Frequency

Frequencies using at CLK1 (MHz)				
12.000	*12.288*	*12.624*	*13.00*	*16.000*
16.128	*16.384*	*16.777*	*16.896*	*17.920*
18.432	*18.936*	*20.000*	*20.480*	*22.1184*
22.579	*24.576*	*24.704*	*25.000*	*27.000*
28.000	*30.720*	*32.000*	*32.768*	*33.330*
34.368	*38.880*	*40.000*	*41.2416*	*41.943*
44.736	*47.457*	*49.152*	*49.408*	*50.000*
		19.440	*35.328*	*40.960*

Note: CLK1 up to 40.960MHz for both 5V and 3.3V for temperature -40°C to 85 °C; CLK1 up to 50MHz for both 5V and 3.3V for temperature 0°C to 70°C.

Pin Configuration



Pin Description

Pin No	Pin Name	Type	Description
1	VC	I	Control voltage input to internal voltage controlled crystal oscillator (VCXO).
2	OPN	I	Negative input terminal to internal operational amplifier.
3	OPOUT	O	Output terminal of internal operational amplifier.
4	OPP	I	Positive input terminal to internal operational amplifier.
5	LOSIN	I	TTL input. When LOSIN is set to HIGH, VC disabled, and when set to LOW, VC to VCXO are enabled. (Internal pull-down resistor)
6	PHO	O	Output signal of phase detector.
7	DATAIN	I	TTL input. Input data stream to phase detector.
8	GND	G	Ground.
9	CLKIN	I	TTL input. Input clock to phase detector.
10	LOS	O	Signal loss indication for DATAIN, high active.
11	RCLK	O	Output recovered clock.
12	RDATA	O	Output recovered data stream.
13	CLK2	O	Output clock with divided function.
14	HIZ	I	TTL input. When HIZ is set to LOW, the device is in standby state and the outputs are set to high impedance. (Internal pull-up resistor)
15	CLK1	O	Output clock of internal VCXO frequency.
16	V_{CC}	P	5V power supply

Notes:

1. LOSIN input sets to HIGH, VC is disabled and the VCXO returns to its nominal center frequency. When sets to LOW, VC to VCXO is enabled.
2. LOS output sets to HIGH, if no transitions are detected at DATAIN after 256 clock cycles. LOS output sets to LOW as soon as a transition occurs at DATAIN.
3. HIZ input sets LOW, output pins CLK1, CLK2, RCLK, and RDATA buffers are set to high-impedance state. When set to logic high or no connection, the device functions and output pins CLK1, CLK2, RCLK, and RDATA etc. are active.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested)

Storage Temperature ..... -55°C to +125°C
Power Supply Voltage ..... -0.5 to +7V
Input High Voltage ..... +7V Max.
Input Low Voltage ..... -0.5V Min.

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

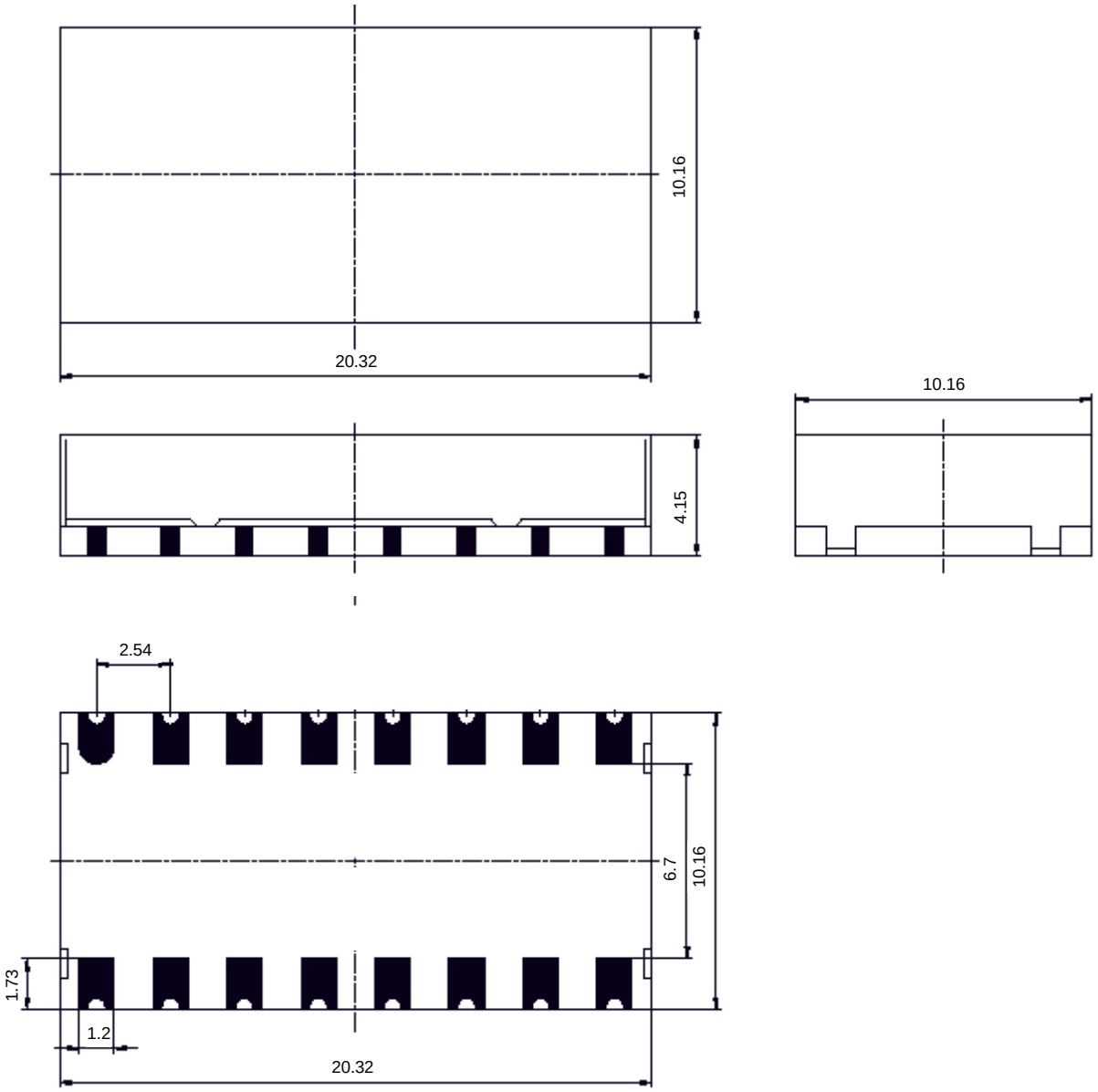
Symbol	Parameters	Conditions	Min		Max	Units
V_{CC}	Supply Voltage		4.5		5.5	V
I_{LEAK}	Input Leakage Current	0~V_{DD}	-10		10	μA
V_{TIH}	TTL Input High Voltage		2			V
V_{TIL}	TTL Input Low Voltage				0.8	V
V_{OH1}	Output High Voltage for CLK1 & 2, RCLK&RDATA	Ioh = -8mA	2.4			V
V_{OL1}	Output Low Voltage for CLK1 & 2, RCLK&RDATA	Iol = 8mA			0.4	V
V_{OH2}	Output High Voltage for LOS	Ioh = -3mA	2.4			V
V_{OL2}	Output Low Voltage for LOS	Iol = 3mA			0.4	V
I_{PULLUP}	Input Pull up Current for HIZ		-160			μA
$I_{PULLDOWN}$	Input Pull down Current for LOSIN				50	μA
I_{CC}	Maximum Supply Current	Full Active			60	mA
T_A	Ambient Temperature		-40		85	°C

AC Electrical Characteristics

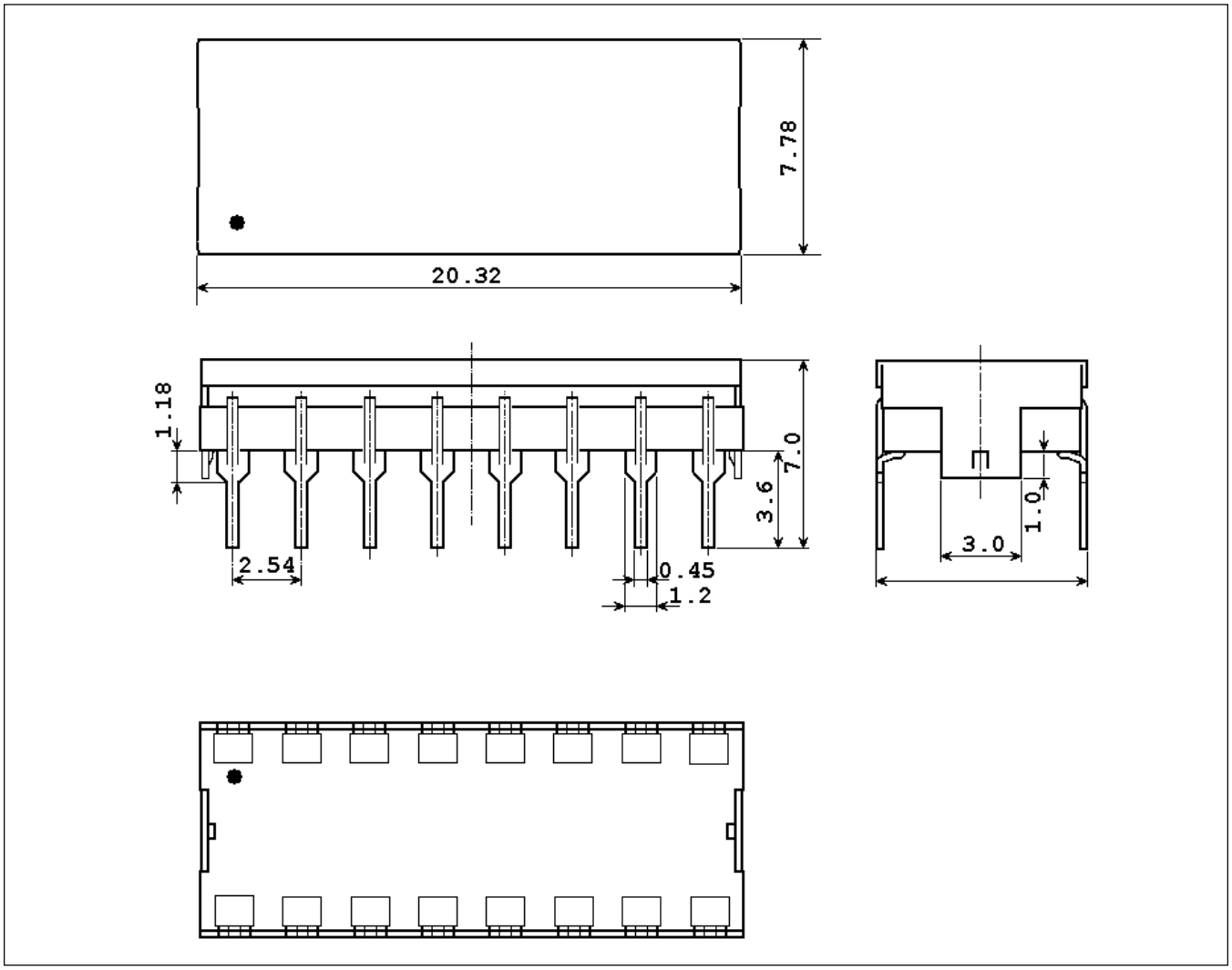
Parameter	Symbol	Min	Typical	Max	Unit
Input NRZ Data Rates	DATAIN	0.008		65.536	M b/s
Input RZ Data and Clock Rates	DATAIN	0.008		32.768	M b/s
Nominal Output Frequency Clock Output 1 Clock Output 2	 CLK1 CLK2	 12.00 CLK1 /256		 65.536 CLK1 /2	 MHz MHz
Transition Times: Rise Time (0.5V to 2.5V) Fall Time (2.5V to 0.5V)	 t_R t_F	 0.5 0.5		 5 5	 ns ns
Symmetry or Duty cycle (VS = 1.4V) CLK1 CLK2 RCLK	 SYM 1 SYM 2 RCLK	 40 45 40		 60 55 60	 % % %
Control Voltage Bandwidth (-3 dB,VC = $0.5V_{CC}$)	BW		20		kHz
Sensitivity @ VC = $V_{CC}/2$	ΔF/ΔVC		100		ppm/V
Nominal Output Frequency on Loss of Signal: Clock Output 1 & 2	CLK1 CLK2	-75 -75		75 75	ppm from fo 1 ppm from fo 2
Phase Detector Gain	K D		0.53 x Data Density		V/rad

Packaging Information

16-pin Surface Mount (G)



16-pin Thru-Hole (T)



Notes

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