AT45DB322F

Low-Power 32 Mbit, 1.65V - 3.6V SPI Serial DataFlash Memory with 256/264 Byte Page Size

PRELIMINARY DATASHEET

Features

- Single 1.65V - 3.6V supply
- Serial Peripheral Interface (SPI) compatible
  - 104 MHz dual and quad SPI I/O
  - Supports SPI modes 0 and 3 and RapidS™ operation
- Active interrupt Smart Intelligent Host Interface technology
- Continuous read capability through entire array
  - Up to 104 MHz
  - Low-power read option up to 20 MHz
  - Clock-to-output time (t_V) of 8ns maximum
- User configurable page size
  - 256 or 264 bytes per page
  - Page size can also be factory pre-configured
- Two fully independent SRAM data buffers
- Flexible programming options
  - Byte/Page Program: 1 to 256/264 bytes directly into main memory
  - Buffer Write: Buffer to Main Memory Page Program
- Flexible erase options
  - Page Erase: 256/264 bytes
  - Block Erase: 2KB for 256/264 byte page size
  - Sector Erase: 256KB for 256/264 byte page size
  - Chip Erase: 32-Mbits
- Program and Erase Suspend/Resume
- Advanced hardware and software data protection features
  - Individual sector protection and lockdown to make any sector read-only
  - Sector lockdown disable command to permanently disable a sector
- 128-byte, One-Time Programmable (OTP) Security Register
  - 64 bytes factory programmed with a unique identifier
  - 64 bytes user programmable
- JEDEC Standard Manufacturer and Device ID Read (5-byte sequence)
- Low-power dissipation
  - 200nA Ultra-Deep Power-Down current (typical)
  - 9µA Deep Power-Down current (typical @ 1.8V)
  - 20µA Standby current (typical @ 1.8V)
  - 5mA Active Read current (typical at 50MHz) — 7.5 mA @ 85 MHz
- Endurance / Data Retention: 100,000 program/erase cycles per page / 20 years
- Complies with full industrial temperature range (-40C to +85C) ROHS
- Green (Pb/Halide-free/RoHS compliant) packaging options
  - 8-lead SOIC (0.208" wide)
  - 8-pad Ultra-thin DFN (5 x 6 x 0.6mm)
  - DWF — Die Wafer Form

Description

This data sheet provides information on the AT45DB322F device. The AT45BD322F device allows users an upgrade path from the AT45DB041E / AT45DB081E devices and contains the same page sizes of 256 (binary device) or 264 bytes (standard device).

The AT45DB322F is a 1.65V minimum, serial-interface sequential access Flash memory ideally suited for a wide variety of digital voice, image, program code, and data storage applications. The AT45DB322F also supports Dual-I/O, Quad-I/O, and RapidS serial interface for applications requiring very high speed operation. For the AT45BD322F device, the memory is organized as 16,384 pages of 256 bytes or 264 bytes each.

In addition to the main memory, the AT45DB322F device contains two independent SRAM buffers of 256/264 bytes. Interleaving between both buffers can dramatically increases a system's ability to write a continuous data stream. In addition, the SRAM buffers can be used as additional system scratch pad memory, and E^2PROM emulation (bit or byte alterability) can be easily handled with a self-contained three step read-modify-write operation. One of the SRAM's can also be used to store critical data that can be written to the Flash memory in the event of a power failure.

Both devices implement the active status interrupt feature using the *Active Status Interrupt* command (25h). This command eliminates the need continuously read the status register to determine when the operation has finished. Rather, the microcontroller need only monitor the value of the MISO pin. Once the operation is finished, the DataFlash device toggles the MISO pin. Refer to Section 4.4.6, Active Status Interrupt for more information.

Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash® uses a serial interface to sequentially access its data. The simple sequential access dramatically reduces active pin count, facilitates simplified hardware layout, increases system reliability, minimizes switching noise, and reduces package size. The device is optimized for use in many commercial and industrial applications where high-density, low-pin count, low-voltage, and low-power are essential.

To allow for simple in-system re-programmability, the AT45DB322F does not require high input voltages for programming. The device operates from a single 1.65V to 3.6V power supply for the erase and program and read operations. The AT45DB322F is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 3-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK). All programming and erase cycles are self-timed.

1. Pinouts and Pin Descriptions

Figure 1-1 shows the pinouts for the 44-ball WLSCP package, the 8-lead SOIC package, and the 8-pad UDFN package. Note that the metal pad on the bottom of the UDFN package is not internally connected to a voltage potential. This pad can be a "no connect" or connected to GND. Care must be taken to avoid the Metal Pad shorting the PCB tracks.

Although the $\overline{WP}$ pin is internally pulled high in this device and therefore may be left floating, it is recommended that it also be externally connected to VCC via a 10 KΩ resistor in most applications.

If the application specifically requires that the device be set in a permanent protection mode, it is recommended that the $\overline{WP}$ pin be connected directly to system ground. Refer to Section 5., Sector Protection for more information.

Figure 1-1. Device Pinouts

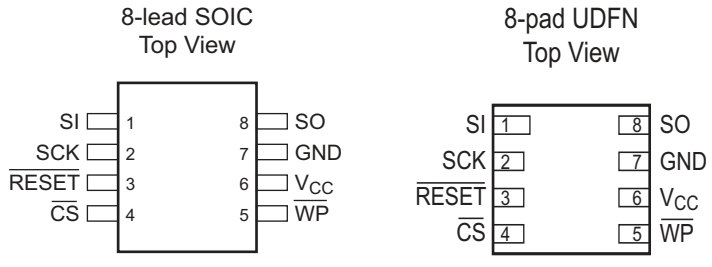


Table 1-1. Pin Descriptions

Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	Chip Select: Asserting the $\overline{CS}$ pin selects the device. When the $\overline{CS}$ pin is deasserted, the device is deselected and normally be placed in the standby mode (not Deep Power-Down mode) and the output pin (SO) is placed in a high-impedance state. When the device is deselected, data is not accepted on the input pin (SI). A high-to-low transition on the $\overline{CS}$ pin is required to start an operation and a low-to-high transition is required to end an operation. When ending an internally self-timed operation such as a program or erase cycle, the device does not enter standby mode until the completion of the operation.	Low	Input
SCK	Serial Clock: This pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command, address, and input data present on the SI pin is always latched on the rising edge of SCK, while output data on the SO pin is always clocked out on the falling edge of SCK.	—	Input
SI (I/O_0)	Serial Input (I/O_0): The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched on the rising edge of SCK. With the Dual-output and Quad-output Read Array commands, the SI pin becomes an output pin (I/O0) and, along with other pins, allows two bits (on I/O_{1-0}) or four bits (on I/O_{3-0}) of data to be clocked out on every falling edge of SCK. To maintain consistency with SPI nomenclature, the SI (I/O0) pin will be referenced as SI throughout the document with exception to sections dealing with the Dual-output and Quad-output Read Array commands in which it will be referenced as I/O_0. Data present on the SI pin will be ignored whenever the device is deselected ($\overline{CS}$ is deasserted).	—	Input/ Output
SO (I/O_1)	Serial Output (I/O_1): The SO pin is used to shift data out of the device. Data on the SO pin is always clocked out on the falling edge of SCK. With the Dual-output and Quad-output Read Array commands, the SO pin becomes an output pin (I/O_1) and, along with other pins, allows two bits (on I/O_{1-0}) or four bits (on I/O_{3-0}) of data to be clocked out on every falling edge of SCK. To maintain consistency with SPI nomenclature, the SO (I/O_1) pin will be referenced as SO throughout the document with exception to sections dealing with the Dual-output and Quad-output Read Array commands in which it is referenced as I/O_1. Hardware places the SO pin in the high-impedance state whenever the device is deselected ($\overline{CS}$ is deasserted).	—	Input/ Output

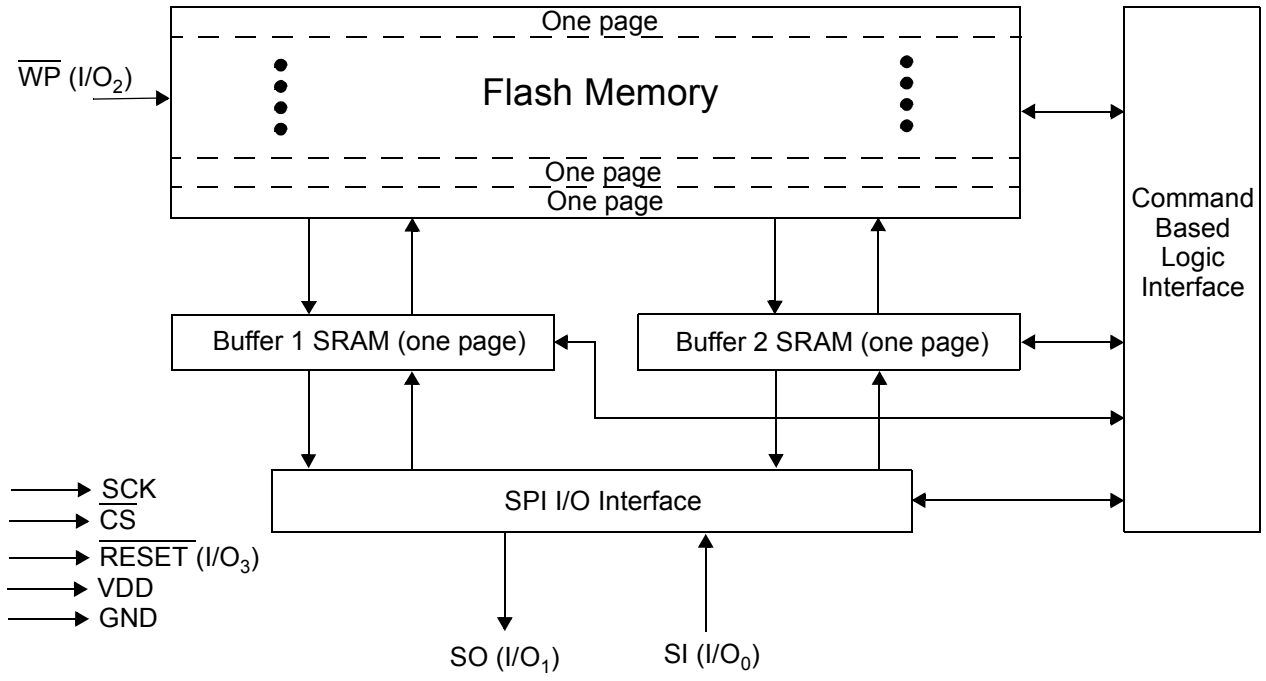
Table 1-1. Pin Descriptions *(continued)*

Symbol	Name and Function	Asserted State	Type
$\overline{WP}$ (I/O_2)	Write Protect (I/O_2): When the $\overline{WP}$ pin is asserted, all sectors specified for protection by the Sector Protection Register will be protected against program and erase operations regardless of whether the Enable Sector Protection command has been issued or not. The $\overline{WP}$ pin functions independently of the software controlled protection method. After the $\overline{WP}$ pin goes low, the contents of the Sector Protection Register cannot be modified. If a program or erase command is issued to the device while the $\overline{WP}$ pin is asserted, the device will simply ignore the command and perform no operation. The device will return to the idle state once the $\overline{CS}$ pin has been deasserted. The Enable Sector Protection command and the Sector Lockdown command, however, will be recognized by the device when the $\overline{WP}$ pin is asserted. The $\overline{WP}$ pin is internally pulled-high at power-up and may be left floating if hardware controlled protection will not be used. However, it is recommended that the $\overline{WP}$ pin also be externally connected to VCC whenever possible. With the Quad-output Read Array command, the $\overline{WP}$ pin becomes an output pin (I/O_2) and, when used with other pins, allows four bits (on I/O_{3-0}) of data to be clocked out on every falling edge of SCK. The QE bit in the Configuration Register must be set in order for the $\overline{WP}$ pin to be used as an I/O data pin.	Low	Input/ Output
$\overline{RESET}$ (I/O_3)	Reset (I/O_3): A low state on the reset pin ($\overline{RESET}$) terminates the operation in progress and resets the internal state machine to an idle state. The device remains in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level. With the Quad-output Read Array command, the $\overline{RESET}$ pin becomes an output pin (I/O_3) and, when used with other pins, allows four bits (on I/O_{3-0}) of data to be clocked out on every falling edge of SCK. The QE bit in the Configuration Register must be set in order for the $\overline{RESET}$ pin to be used as an I/O data pin. The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. If this pin and feature is not utilized, then it is recommended that the $\overline{RESET}$ pin be driven high externally.	Low	Input/ Output
V_{CC}	Device Power Supply: The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	—	Power
GND	Ground: The ground reference for the power supply. GND should be connected to the system ground.	—	Ground

2. Block Diagram

The following figure shows a block diagram of the AT45DB322F device.

Figure 2-1. Block Diagram of the AT45DB322F Device



As shown in the figure above, each entry in the Flash memory has a width of one page. The actual width of the page in bits and the number of pages in the memory depends on the product type. The Buffer 1 and Buffer 2 SRAM memories each contain a single page. The available memory sizes and corresponding page sizes are shown in Table 2-1.

Table 2-1. AT45DB322F Product Offerings

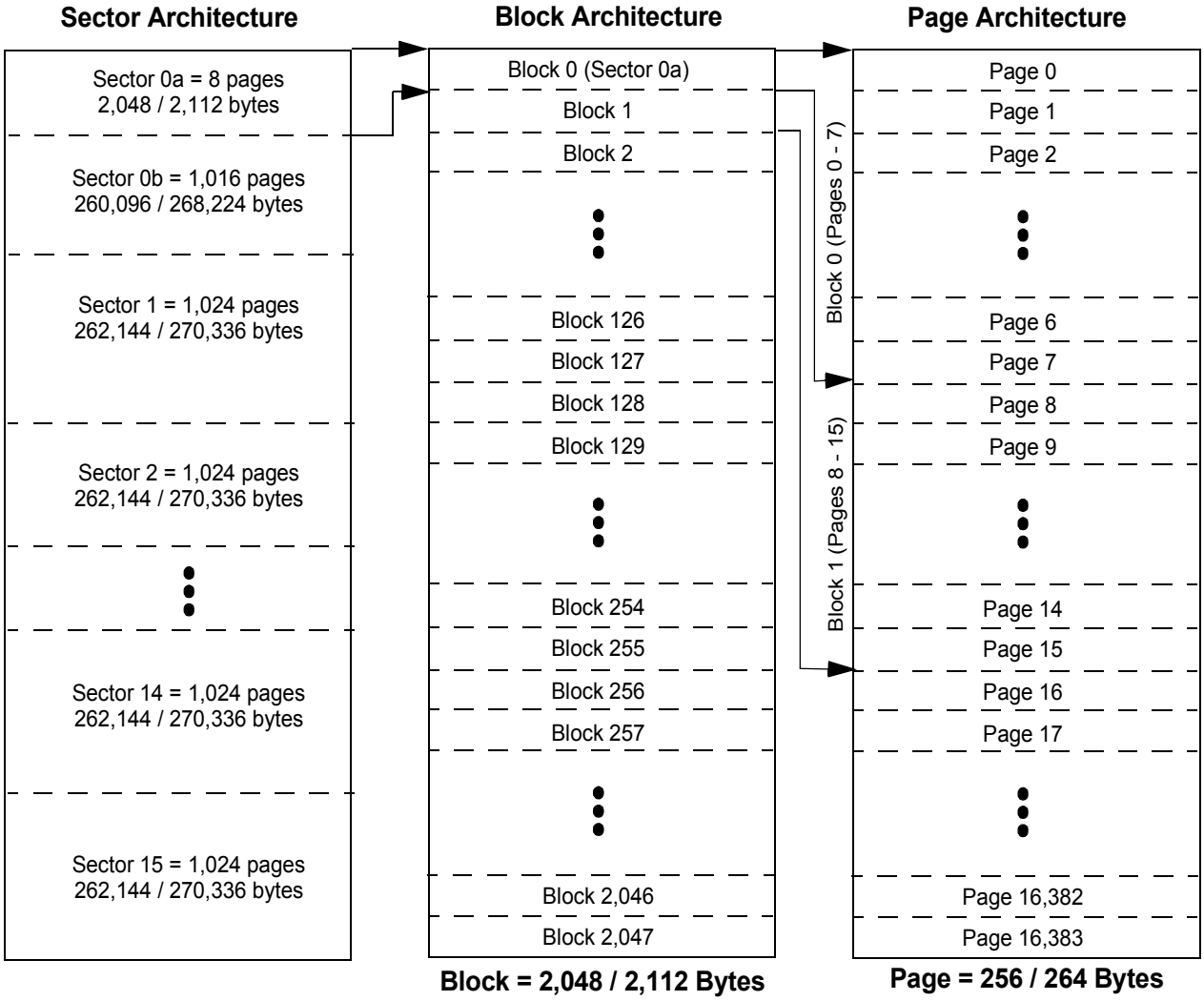
Product Number	Flash Memory Size (Bytes)	Page Size	Number of Pages	Product Type
AT45DB322F	32M	256-byte	16,384	Binary
AT45DB322F	32M	264-byte	16,384	Standard

The Binary product part ordering code includes the '2B' suffix in the part number. Refer to Section 24., Ordering Information for more information.

3. Memory Array

To provide optimal flexibility, the AT45DB322F memory array is divided into three levels of granularity comprising of sectors, blocks, and pages. Figure 3-1, AT45DB322F Memory Architecture Diagram illustrates the breakdown of each level and details the number of pages per sector and block for each device. Program operations to the DataFlash can be done at the full page level or at the byte level (a variable number of bytes). The erase operations can be performed at the chip, sector, block, or page level.

Figure 3-1. AT45DB322F Memory Architecture Diagram



4. Command Interface and Device Operation

The device operation is controlled by instructions from the host processor. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK pin controls the loading of the opcode and the desired buffer or main memory address location through the SI (Serial Input) pin. All instructions, addresses, and data are transferred with the Most Significant Bit (MSB) first.

Three address bytes are used to address memory locations in either the main memory array or in one of the SRAM buffers. The three address bytes are comprised of a number of dummy bits and a number of actual device address bits, with the number of dummy bits varying depending on the operation being performed and the selected device page size.

Buffer addressing for the standard DataFlash page size (264 bytes) is referenced in the datasheet using the terminology BFAx - BFA0 to denote the address bits required to designate a byte address within a buffer, where 'x' is the highest order address bit used to index the buffer. The main memory addressing is referenced using the terminology PA1y - PA0 and BAx - BA0, where 'y' denotes the highest order address bit used to index the memory and 'x' denotes the highest order bit used to access a given byte of a page within the memory. For example, if address ranges of PA[14:0] and BA[8:0] are used, this means that the upper 15 address bits are used to index a page within the memory, and BA[8:0] are used index a byte within the page. In this case, a total of 24 address bits are used.

For the "power of 2" binary page size (256 bytes), the buffer addressing is referenced in the datasheet using the conventional terminology Ax - A0 to denote the address bits required to designate a byte address within a buffer. Main memory addressing is referenced using the terminology A2y - A0, where 'y' denotes the highest order address bit used to index the memory. For example, A[22:8] denotes that 15 address bits are required to index a page within the memory, and A7 - A0 denotes the 8 address bits required to designate a byte address within a page. Therefore, a total of 23 address bits are used.

4.1 Dual-I/O and Quad I/O Operation

The AT45DB322F features a Dual-input Buffer Write mode and a Dual-output Read mode that allows two bits of data to be clocked into Buffer 1 or Buffer 2 or allows two bits of data to be read out of the device on every clock cycle to improve throughputs. To accomplish this, both the SI and SO pins are utilized as inputs/outputs for the transfer of data bytes. With the Dual-input Buffer Write command, the SO pin becomes an input along with the SI pin. Alternatively, with the Dual-output Read Array command, the SI pin becomes an output along with the SO pin. For both Dual-I/O commands, the SO pin is referred to as I/O_1 and the SI pin will be referred to as I/O_0.

The device also supports a Quad-input Buffer Write mode and a Quad-output Read mode in which the $\overline{WP}$ (I/O_2) and $\overline{RESET}$ (I/O_3) pins become data pins for even higher throughputs by allowing four bits of data to be clocked on every clock cycle into one of the buffers or by allowing four bits of data to be read out of the device on every clock cycle. For the Quad-input Buffer Write and Quad-output Read Array commands, the $\overline{RESET}$, $\overline{WP}$, SO and SI pins are referred to as I/O_{3-0} where $\overline{RESET}$ becomes I/O_3, $\overline{WP}$ becomes I/O_2, SO becomes I/O_1 and SI becomes I/O_0.

The QE bit in the Configuration Register must be set (via issuing the Quad Enable command) to enable the Quad-I/O operation and to enable the $\overline{RESET}$ and $\overline{WP}$ pins to be converted to I/O data pins.

4.2 Read Commands

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two SRAM data buffers. The DataFlash supports RapidS protocols for Mode 0 and Mode 3. Please see Section 22., Detailed Bit-level Read Waveforms: RapidS Mode 0/Mode 3 diagrams in this datasheet for details on the clock cycle sequences for each mode.

Table 4-1. Read Commands

Command	Opcode	Description
Continuous Array Read (Legacy)	E8h	The continuous array read command can be utilized to sequentially read a continuous stream of data from the device by simply providing a clock signal. The DataFlash incorporates an internal address counter that automatically increments on every clock cycle, allowing one continuous read from memory to be performed without the need for additional address sequences. The dummy bytes that follow the address types are needed to initiate the read operation. Following the dummy bytes, additional clock pulses on the SCK pin result in data being output onto the SO (serial out) pin. When the end of a page in the main memory is reached during a Continuous Array Read, the device continues reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit in the main memory array has been read, the device continues reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays are incurred when wrapping around from the end of the array to the beginning of the array. **Warning:** This command is not recommended for new designs.
Continuous Array Read (High Frequency Mode)	1Bh	This command can be used to read the main memory array sequentially at the highest possible operating clock frequency up to the maximum specified by f_{CAR4}.
Continuous Array Read (High Frequency Mode)	0Bh	This command can be used to read the main memory array sequentially at higher clock frequencies up to the maximum specified by f_{CAR1}.
Continuous Array Read (Low Frequency Mode)	03h	This command can be used to read the main memory array sequentially at lower clock frequencies up to maximum specified by f_{CAR2}. Unlike the previously described read commands, this Continuous Array Read command for the lower clock frequencies does not require the clocking in of dummy bytes after the address byte sequence. Following the address bytes, additional clock pulses on the SCK pin results in data being output on the SO pin.
Continuous Array Read (Low Power Mode)	01h	This command is ideal for applications that want to minimize power consumption and do not need to read the memory array at high frequencies. Like the 03h opcode, this Continuous Array Read command allows reading the main memory array sequentially without the need for dummy bytes to be clocked in after the address byte sequence. The memory can be read at clock frequencies up to maximum specified by f_{CAR3}.
Main Memory Page Read	D2h	A Main Memory Page Read allows the reading of data directly from a single page in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. The dummy bytes that follow the address bytes are sent to initialize the read operation. The maximum SCK frequency allowable for the Main Memory Page Read is defined by the f_{SCK} specification.
Buffer 1 Read	D1h (low-freq) D4h (high-freq)	The Buffer 1 SRAM data buffer can be accessed independently from the main memory array, and utilizing the Buffer Read command allows data to be sequentially read directly from either one of the buffers. The use of each opcode depends on the maximum SCK frequency that is used to read data from the buffers.
Buffer 2 Read	D3h (low-freq) D6h (high-freq)	The Buffer 2 SRAM data buffer can be accessed independently from the main memory array, and utilizing the Buffer Read command allows data to be sequentially read directly from either one of the buffers. The use of each opcode depends on the maximum SCK frequency that is used to read data from the buffers.

Table 4-1. Read Commands *(continued)*

Command	Opcode	Description
Dual-output Read Array	3Bh	The Dual-output Read Array command is similar to the Continuous Array Read command and can be used to sequentially read a continuous stream of data from the device by simply providing the clock signal once the initial starting address has been specified. Unlike the Continuous Array Read command however, the Dual-output Read Array command allows two bits of data to be clocked out of the device on every clock cycle rather than just one. After the three address bytes and the dummy byte have been clocked in, additional clock cycles results in data being output on both the I/O_1 and I/O_0 pins. The data is always output with the MSB of a byte first, and the MSB is always output on the I/O_1 pin. During the first clock cycle, bit seven of the first data byte is output on the I/O_1 pin while bit six of the same data byte is output on the I/O_0 pin. During the next clock cycle, bits five and four of the first data byte is output on the I/O_1 and I/O_0 pins, respectively. The sequence continues with each byte of data being output after every four clock cycles.
Quad-output Read Array	6Bh	The Quad-output Read Array command is similar to the Dual-output Read Array command and can be used to sequentially read a continuous stream of data from the device by simply providing the clock signal once the initial starting address has been specified. Unlike the Dual-output Read Array command however, the Quad-output Read Array command allows four bits of data to be clocked out of the device on every clock cycle rather than two. After the three address bytes and the dummy byte have been clocked in, additional clock cycles results in data being output on the I/O_{3-0} pins. The data is always output with the MSB of a byte first and the MSB is always output on the I/O_3 pin. During the first clock cycle, bit seven of the first data byte is output on the I/O_3 pin while bits six, five, and four of the same data byte is output on the I/O_2, I/O_1, and I/O_0 pins, respectively. During the next clock cycle, bits three, two, one, and zero of the first data byte is output on the I/O_3, I/O_2, I/O_1 and I/O_0 pins, respectively. The sequence continues with each byte of data being output after every two clock cycles.

For each of the read commands listed above, the $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the dummy bytes (if present), and the reading of data. When the end of a page in the main memory is reached during a Continuous Array Read, the device continues reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page).

When the last bit in the main memory array has been read, the device continues reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays are incurred when wrapping around from the end of the array to the beginning of the array. The only exception to this is the Main Memory Read. In this case, when the end of a page in main memory is reached, the device continues reading back at the beginning of the same page rather than the beginning of the next page.

A low-to-high transition on the $\overline{CS}$ pin terminates the read operation and tri-state the output pin (SO). The maximum SCK frequency allowable for the Continuous Array Read is defined by the corresponding f_{CARx} specification. The Continuous Array Read commands bypass both data buffers and leaves the contents of the buffers unchanged.

The following tables define the parameters of the various read commands. Table 4-2 shows the read operations for the AT45DB322F device. Each of these commands is defined in Table 4-1 above.

Table 4-2. AT45DB322F Standard and Binary Device Read Operations

Operation	Opcode	Maximum SCK Frequency	Page Size	Address			Number of Dummy Bytes
				Total Number of Address Bits	Page Address	Starting Byte within Page	
Continuous Array Read (Legacy)	E8h	f_{CAR1}	264	24	PA[14:0]	BA[8:0]	4
			256	23	A[22:8]	A[7:0]	4
Continuous Array Read (High Frequency Mode)	1Bh	f_{CAR4}	264	24	PA[14:0]	BA[8:0]	2
			256	23	A[22:8]	A[7:0]	2
Continuous Array Read (High Frequency Mode)	0Bh	f_{CAR1}	264	24	PA[14:0]	BA[8:0]	1
			256	23	A[22:8]	A[7:0]	1
Continuous Array Read (Low Frequency Mode)	03h	f_{CAR2}	264	24	PA[14:0]	BA[8:0]	0
			256	23	A[22:8]	A[7:0]	0
Continuous Array Read (Low Power Mode)	01h	f_{CAR3}	264	24	PA[14:0]	BA[8:0]	0
			256	23	A[22:8]	A[7:0]	0
Memory Page Read	D2h	f_{SCK}	264	24	PA[14:0]	BA[8:0]	4
			256	23	A[22:8]	A[7:0]	4
SRAM Buffer 1 Read	D4h	f_{CAR1}	264	24	PA[14:0] (dummy)	BFA[8:0]	1
			256	24	PA[15:0] (dummy)	BFA[7:0]	1
	D1h	f_{CAR2}	264	24	PA[14:0] (dummy)	BFA[8:0]	1
			256	24	PA[15:0] (dummy)	BFA[7:0]	1
SRAM Buffer 2 Read	D6h	f_{CAR1}	264	24	PA[14:0] (dummy)	BFA[8:0]	1
			256	24	PA[15:0] (dummy)	BFA[7:0]	1
Dual-output Read Array	3Bh	f_{CAR5}	264	23	PA[14:0]	BA[8:0]	1
			256	22	A22:0	--	1
Quad-output Read Array	6Bh	f_{CAR6}	264	23	PA[14:0]	BA[8:0]	1
			256	22	A22:0	--	1

4.3 Program and Erase Commands

Table 4-3 shows the commands used to program and/or erase part of all of the Flash memory. The table shows the command name, opcode, and description. Refer to Table 4-4 for more detailed information on each command type, including required address and data fields required based on product type.

During the transaction, the RDY/BUSY bit in the Status Register indicates that the device is busy. The device also incorporates an intelligent erase and program algorithm that can detect when a byte location fails to erase or program properly. If an erase or programming error arises, it is indicated by the EPE bit in the Status Register.

Table 4-3. Program and Erase Command Definitions

Command	Opcode	Description
Buffer Write	84h (Buffer 1) 87h (Buffer 2)	The write buffer commands allows data clocked in from the SI pin to be written directly into either one or the SRAM data buffers. After the last address byte has been clocked into the device, data can then be clocked in on subsequent clock cycles. If the end of the data buffer is reached, the device wraps around back to the beginning of the buffer. Data continues to be loaded into the buffer until a low-to-high transition is detected on the $\overline{CS}$ pin.
Dual-input Buffer Write	24h (Buffer 1) 27h (Buffer 2)	The Dual-input Buffer Write command is similar to the Buffer Write command and can be used to increase the data input into one of the SRAM buffers by allowing two bits of data to be clocked into the device on every clock cycle rather than just one.
Quad-input Buffer Write	44h (Buffer 1) 47h (Buffer 2)	The Quad-input Buffer Write command is similar to the Buffer Write command and can be used to significantly increase the data input into one of the SRAM buffers by allowing four bits of data to be clocked into the device on every clock cycle rather than just one.
Buffer to Main Memory Page Program with Built-in Erase	83h (Buffer 1) 86h (Buffer 2)	The Buffer to Main Memory Page Program with Built-In Erase command allows data that is stored in one of the SRAM buffers to be written into an erased or programmed page in the main memory array. It is not necessary to pre-erase the page in main memory to be written because this command automatically erases the selected page prior to the program cycle. When a low-to-high transition occurs on the $\overline{CS}$ pin, the device first erases the selected page in main memory (the erased state is a Logic 1) and then program the data stored in the appropriate buffer into that same page in main memory. Both the erasing and the programming of the page are internally self-timed and should take place in a maximum time of t_{EP}.
Buffer to Main Memory Page Program without Built-in Erase	88h (Buffer 1) 89h (Buffer 2)	The Buffer to Main Memory Page Program without Built-In Erase command allows data that is stored in one of the SRAM buffers to be written into a pre-erased page in the main memory array. It is necessary that the page in main memory to be written be previously erased in order to avoid programming errors. When a low-to-high transition occurs on the $\overline{CS}$ pin, the device programs the data stored in the appropriate buffer into the specified page in the main memory. The page in main memory that is being programmed must have been previously erased using one of the erase commands (Page Erase, Block Erase, Sector Erase, or Chip Erase). The programming of the page is internally self-timed and should take place in a maximum time of t_P.
Main Memory Page Program through Buffer with Built-in Erase	82h (Buffer 1) 85h (Buffer 2)	The Main Memory Page Program through Buffer with Built-In Erase command combines the Buffer Write and Buffer to Main Memory Page Program with Built-In Erase operations into a single operation to help simplify application firmware development. With the Main Memory Page Program through Buffer with Built-In Erase command, data is first clocked into either Buffer 1 or Buffer 2, the addressed page in memory is then automatically erased, and then the contents of the appropriate buffer are programmed into the just-erased main memory page. After all address bytes have been clocked in, the device takes data from the input pin (SI) and store it in the specified data buffer. If the end of the buffer is reached, the device wraps around back to the beginning of the buffer. When there is a low-to-high transition on the $\overline{CS}$ pin, the device first erases the selected page in main memory (the erased state is a Logic 1) and then program the data stored in the buffer into that main memory page. Both the erasing and the programming of the page are internally self-timed and should take place in a maximum time of t_{EP}.

Table 4-3. Program and Erase Command Definitions *(continued)*

Command	Opcode	Description
Main Memory Byte/Page Program through Buffer 1 without Built-in Erase	02h	The Main Memory Byte/Page Program through Buffer 1 without Built-In Erase command combines both the Buffer Write and Buffer to Main Memory Program without Built-In Erase operations to allow any number of bytes (1 to 256/264 bytes) to be programmed directly into previously erased locations in the main memory array. With the Main Memory Byte/Page Program through Buffer 1 without Built-In Erase command, data is first clocked into Buffer 1, and then only the bytes clocked into the buffer are programmed into the pre-erased byte locations in main memory. Multiple bytes up to the page size can be entered with one command sequence. After all address bytes are clocked in, the device takes data from the input pin (SI) and store it in Buffer 1. Any number of bytes (1 to 256) can be entered. If the end of the buffer is reached, then the device wraps around back to the beginning of the buffer. When using the binary page size, the page and buffer address bits correspond to a 23-bit logical address (A22-A0) in the main memory. After all data bytes have been clocked into the device, a low-to-high transition on the CS pin starts the program operation in which the device programs the data stored in Buffer 1 into the main memory array. Only the data bytes that were clocked into the device are programmed into the main memory. If only two data bytes were clocked into the device, then only two bytes are programmed into main memory and the remaining bytes in the memory page remain in their previous state. The $\overline{CS}$ pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, the operation is aborted and no data is programmed. The programming of the data bytes is internally self-timed and should take place in a maximum time of t_P (the program time is a multiple of the t_{BP} time depending on the number of bytes being programmed).

Table 4-3. Program and Erase Command Definitions *(continued)*

Command	Opcode	Description
Buffer Write (Read-Modify-Write)	58h (Buffer 1) 59h (Buffer 2)	The Buffer Write command uses the same opcode as the Read-Modify-Write command. A completely self-contained read-modify-write operation can be performed to reprogram any number of sequential bytes in a page in the main memory array without affecting the rest of the bytes in the same page. This command allows the device to easily emulate an EEPROM by providing a method to modify a single byte or more in the main memory in a single operation, without the need for pre-erasing the memory or the need for any external RAM buffers. The Read-Modify-Write command is essentially a combination of the Main Memory Page to Buffer Transfer, Buffer Write, and Buffer to Main Memory Page Program with Built-in Erase commands. After the address bytes have been clocked in, any number of sequential data bytes from one to 256/264 bytes can be clocked into the device. If the end of the buffer is reached when clocking in the data, then the device wraps around back to the beginning of the buffer. After all data bytes have been clocked into the device, a low-to-high transition on the CS pin starts the self-contained, internal read-modify-write operation. Only the data bytes that were clocked into the device are reprogrammed in the main memory. If only one data byte was clocked into the device, then only one byte in main memory are reprogrammed and the remaining bytes in the main memory page remain in their previous state. The CS pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, the operation is aborted and no data is programmed. The reprogramming of the data bytes is internally self-timed and should take place in a maximum time of t_P. The Read-Modify-Write command uses the same opcodes as the Auto Page Rewrite command. If no data bytes are clocked into the device, then the device performs an Auto Page Rewrite operation.
Page Erase	81h	The Page Erase command can be used to individually erase any page in the main memory array allowing the Buffer to Main Memory Page Program without Built-In Erase command or the Main Memory Byte/Page Program through Buffer 1 command to be utilized at a later time. When a low-to-high transition occurs on the $\overline{CS}$ pin, the device erases the selected page (the erased state is a Logic 1). The erase operation is internally self-timed and should take place in a maximum time of t_{PE}.
Block Erase	50h	The Block Erase command can be used to erase a block of eight pages at one time. This command is useful when needing to pre-erase larger amounts of memory and is more efficient than issuing eight separate Page Erase commands. Refer to Table 4-5 for more information on Block erase.
Sector Erase	7Ch	The Sector Erase command can be used to individually erase any sector in the main memory. Refer to Table 4-6 for more information on Block erase.
Chip Erase	C7h, 94h, 80h, 9Ah	The Chip Erase command allows the entire main memory array to be erased can be erased at one time. Refer to Table 4-7 for more information on Chip erase.

Table 4-3. Program and Erase Command Definitions *(continued)*

Command	Opcode	Description
Program Erase/Suspend	B0h	In some code and data storage applications, it may not be possible for the system to wait the milliseconds required for the Flash memory to complete a program or erase cycle. The Program/Erase Suspend command allows a program or erase operation in progress to a particular 256KB sector of the main memory array to be suspended so that other device operations can be performed. By suspending an erase operation to a particular sector, the system can perform functions such as a program or read operation within a different 256KB sector. Other device operations, such as Read Status Register, can also be performed while a program or erase operation is suspended. No address bytes need to be clocked into the device, and any data clocked in after the opcode is ignored. Refer to Section 4.3.4 for more information on Program Erase/Suspend.
Program Erase/Resume	D0h	The Program/Erase Resume command allows a suspended program or erase operation to be resumed and continue where it left off. No address bytes need to be clocked into the device, and any data clocked in after the opcode is ignored. Refer to Section 4.3.5 for more information on Program Erase/Suspend.

Table 4-4. AT45DB322F Standard and Binary Device Program and Erase Operations

Operation	Opcode	Page Size	Address			Number of Dummy Bytes
			Total Number of Address Bits	Page Address	Starting Byte within Page	
SRAM Buffer 1 Write	84h	264	24	PA[14:0] (dummy)	BFA[8:0]	0
	84h	256	23	PA[15:0] (dummy)	BFA[7:0]	0
SRAM Buffer 2 Write	87h	264	24	PA[14:0] (dummy)	BFA[8:0]	0
	87h	256	23	PA[15:0] (dummy)	BFA[7:0]	0
Dual-input Buffer 1 Write	24h	264	24	PA[14:0] (dummy)	BFA[8:0]	0
	24h	256	24	PA[15:0] (dummy)	BFA[7:0]	0
Dual-input Buffer 2 Write	27h	264	24	PA[14:0] (dummy)	BFA[8:0]	0
	27h	256	24	PA[15:0] (dummy)	BFA[7:0]	0
Quad-input Buffer 1 Write	44h	264	24	PA[14:0] (dummy)	BFA[8:0]	0
	44h	256	24	PA[15:0] (dummy)	BFA[7:0]	0
Quad-input Buffer 2 Write	47h	264	24	PA[14:0] (dummy)	BFA[8:0]	0
	47h	256	24	PA[15:0] (dummy)	BFA[7:0]	0

Table 4-4. AT45DB322F Standard and Binary Device Program and Erase Operations *(continued)*

Operation	Opcode	Page Size	Address			Number of Dummy Bytes
			Total Number of Address Bits	Page Address	Starting Byte within Page	
Buffer 1 to Main Memory Page Program with Built-in Erase	83h	264	24	PA[14:0]	BFA[8:0] (dummy)	0
	83h	256	23	A[22:8]	BFA[7:0] (dummy)	0
Buffer 2 to Main Memory Page Program with Built-in Erase	86h	264	24	PA[14:0]	BFA[8:0] (dummy)	0
	86h	256	23	A[22:8]	BFA[7:0] (dummy)	0
Buffer 1 to Main Memory Page Program without Built-in Erase	88h	264	24	PA[14:0]	BFA[8:0] (dummy)	0
	88h	256	23	A[22:8]	BFA[7:0] (dummy)	0
Buffer 2 to Main Memory Page Program without Built-in Erase	89h	264	24	PA[14:0]	BFA[8:0] (dummy)	0
	89h	256	23	A[22:8]	BFA[7:0] (dummy)	0
Main Memory Byte/Page Program through Buffer 1 with Built-in Erase	82h	264	24	PA[14:0]	BFA[8:0]	0
	82h	256	23	A[22:8]	BFA[7:0]	0
Main Memory Byte/Page Program through Buffer 2 with Built-in Erase	85h	264	24	PA[14:0]	BFA[8:0]	0
	85h	256	23	A[22:8]	BFA[7:0]	0
Main Memory Byte/Page Program through Buffer 1 without Built-in Erase	02h	264	24	PA[14:0]	BFA[8:0]	0
	02h	256	23	A[22:8]	BFA[7:0]	0
Byte Write Buffer 1 (Read-Modify-Write)	58h	264	24	PA[14:0]	BFA[8:0]	0
	58h	256	23	A[22:8]	BFA[7:0]	0
Byte Write Buffer 2 (Read-Modify-Write)	59h	264	24	PA[14:0]	BFA[8:0]	0
	59h	256	23	A[22:8]	BFA[7:0]	0
Page Erase	81h	264	24	PA[14:0]	BFA[8:0] (dummy)	0
	81h	256	23	A[22:8]	BFA[7:0] (dummy)	0
Block Erase	50h	264	24	PA[14:3]	BFA[11:0] (dummy)	0
	50h	256	23	A[22:11]	BFA[10:0] (dummy)	0
Sector Erase (0a or 0b)	7Ch	264	24	PA[14:3]	BFA[11:0] (dummy)	0
	7Ch	256	23	A[22:11]	BFA[10:0] (dummy)	0
Sector Erase (1 - 31)	7Ch	264	24	PA[14:10]	BFA[18:0] (dummy)	0
	7Ch	256	23	A[22:18]	BFA[17:0] (dummy)	0

Table 4-4. AT45DB322F Standard and Binary Device Program and Erase Operations *(continued)*

Operation	Opcode	Page Size	Address			Number of Dummy Bytes
			Total Number of Address Bits	Page Address	Starting Byte within Page	
Chip Erase	C7h (byte 1) 94h (byte 2) 80h (byte 3) 9Ah (byte 4)	264 or 256	—	—	—	—
Program/Erase Suspend	B0h	264 or 256	—	—	—	—
Program/Erase Resume	D0h	264 or 256	—	—	—	—

4.3.1 Block Erase

Table 4-5 shows the address bit setting for erasing each one of the memory blocks.

Table 4-5. Block Erase Addressing

PA14/ A22	PA13/ A21	PA12/ A20	PA11/ A19	PA10/ A18	PA9/ A17	PA8/ A16	PA7/ A15	PA6/ A14	PA5/ A13	PA4/ A12	PA3/ A11	PA2/ A10	PA1/ A9	PA0/ A8	Block
0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	1
0	0	0	0	0	0	0	0	0	0	1	0	X	X	X	2
0	0	0	0	0	0	0	0	0	0	1	1	X	X	X	3
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	1	0	0	X	X	X	4092
1	1	1	1	1	1	1	1	1	1	0	1	X	X	X	4093
1	1	1	1	1	1	1	1	1	1	1	0	X	X	X	4094
1	1	1	1	1	1	1	1	1	1	1	1	X	X	X	4095

4.3.2 Sector Erase

Table 4-6 shows the address bit setting for the sector erase operation.

Table 4-6. Sector Erase Addressing

PA14/ A22	PA13/ A21	PA12/ A20	PA11/ A19	PA10/ A18	PA9/ A17	PA8/ A16	PA7/ A15	PA6/ A14	PA5/ A13	PA4/ A12	PA3/ A11	PA2/ A10	PA1/A9	PA0/A8	Sector
0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	0a
0	0	0	0	0	0	0	0	0	0	0	1	X	X	X	0b
0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	2
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	28
1	1	1	0	1	X	X	X	X	X	X	X	X	X	X	29
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	30

Table 4-6. Sector Erase Addressing *(continued)*

PA14/ A22	PA13/ A21	PA12/ A20	PA11/ A19	PA10/ A18	PA9/ A17	PA8/ A16	PA7/ A15	PA6/ A14	PA5/ A13	PA4/ A12	PA3/ A11	PA2/ A10	PA1/A9	PA0/A8	Sector
1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	31

4.3.3 Chip Erase

To execute the Chip Erase command, a 4-byte command sequence of C7h, 94h, 80h, and 9Ah must be clocked into the device. Since the entire memory array is to be erased, no address bytes need to be clocked into the device, and any data clocked in after the opcode is ignored. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to start the erase process. The erase operation is internally self-timed and should take place in a time of t_{CE}.

The Chip Erase command does not affect sectors that are protected or locked down; the contents of those sectors remain unchanged. Only those sectors that are not protected or locked down are erased.

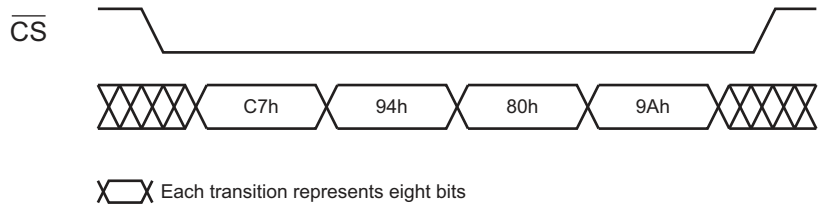
The $\overline{WP}$ pin can be asserted while the device is erasing, but protection is not activated until the internal erase cycle completes.

The device also incorporates an intelligent algorithm that can detect when a byte location fails to erase properly. If an erase error arises, it is indicated by the EPE bit in the Status Register.

Table 4-7. Chip Erase Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Chip Erase	C7h	94h	80h	9Ah

Figure 4-1. Chip Erase



4.3.4 Program/Erase Suspend

When the $\overline{CS}$ pin is deasserted, the program or erase operation currently in progress is suspended within a time of t_{SUSP}. One of the Program Suspend bits ($\overline{PS1}$ or $\overline{PS2}$) or the Erase Suspend bit (ES) in the Status Register is then be set to the Logic 1 state. In addition, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is ready for another operation.

Read operations are not allowed to a 256KB sector that has had its program or erase operation suspended. If a read is attempted to a suspended sector, then the device outputs undefined data. Therefore, when performing a Continuous Array Read operation and the device's internal address counter increments and crosses the sector boundary to a suspended sector, the device then starts outputting undefined data continuously until the address counter increments and crosses a sector boundary to an un-suspended sector.

A program operation is not allowed to a sector that has been erase suspended. If a program operation is attempted to an erase suspended sector, then the program operation aborts.

During an Erase Suspend, a program operation to a different 256KB sector can be started and subsequently suspended. This results in a simultaneous Erase Suspend/Program Suspend condition and is indicated by the states of both the ES and PS1 or PS2 bits in the Status Register being set to a Logic 1.

If a Reset command is performed, or if the $\overline{RESET}$ pin is asserted while a sector is erase suspended, then the suspend operation is aborted and the contents of the sector is left in an undefined state. However, if a reset is performed while a

page is program or erase suspended, the suspend operation aborts but only the contents of the page that was being programmed or erased are undefined; the remaining pages in the 256KB sector retain their previous contents.

Table 4-8. Operations Allowed and Not Allowed During Suspend

Command	Operation During Program Suspend in Buffer 1 (PS1)	Operation During Program Suspend in Buffer 2 (PS2)	Operation During Erase Suspend (ES)
Read Commands			
Read Array (All Opcodes)	Allowed	Allowed	Allowed
Read Buffer 1 (All Opcodes)	Allowed	Allowed	Allowed
Read Buffer 2 (All Opcodes)	Allowed	Allowed	Allowed
Dual-output Read Array	Allowed	Allowed	Allowed
Quad-output Read Array	Allowed	Allowed	Allowed
Program and Erase Commands			
Buffer 1 Write	Not Allowed	Allowed	Allowed
Buffer 2 Write	Allowed	Not Allowed	Allowed
Dual-input Buffer 1 Write	Not Allowed	Allowed	Allowed
Dual-input Buffer 2 Write	Allowed	Not Allowed	Allowed
Quad-input Buffer 1 Write	Not Allowed	Allowed	Allowed
Quad-input Buffer 2 Write	Allowed	Not Allowed	Allowed
Buffer 1 to Memory Program w/ Erase	Not Allowed	Not Allowed	Not Allowed
Buffer 2 to Memory Program w/ Erase	Not Allowed	Not Allowed	Not Allowed
Buffer 1 to Memory Program w/o Erase	Not Allowed	Not Allowed	Allowed
Buffer 2 to Memory Program w/o Erase	Not Allowed	Not Allowed	Allowed
Memory Program through Buffer 1 w/ Erase	Not Allowed	Not Allowed	Not Allowed
Memory Program through Buffer 2 w/ Erase	Not Allowed	Not Allowed	Not Allowed
Memory Program through Buffer 1 w/o Erase	Not Allowed	Not Allowed	Allowed
Auto Page Rewrite through Buffer 1	Not Allowed	Not Allowed	Not Allowed
Auto Page Rewrite through Buffer 2	Not Allowed	Not Allowed	Not Allowed
Read-Modify-Write through Buffer 1	Not Allowed	Not Allowed	Not Allowed
Read-Modify-Write through Buffer 2	Not Allowed	Not Allowed	Not Allowed
Page Erase	Not Allowed	Not Allowed	Not Allowed
Block Erase	Not Allowed	Not Allowed	Not Allowed
Sector Erase	Not Allowed	Not Allowed	Not Allowed
Chip Erase	Not Allowed	Not Allowed	Not Allowed
Protection and Security Commands			
Enable Sector Protection	Not Allowed	Not Allowed	Not Allowed
Disable Sector Protection	Not Allowed	Not Allowed	Not Allowed
Erase Sector Protection Register	Not Allowed	Not Allowed	Not Allowed
Program Sector Protection Register	Not Allowed	Not Allowed	Not Allowed
Read Sector Protection Register	Allowed	Allowed	Allowed
Sector Lockdown	Not Allowed	Not Allowed	Not Allowed
Read Sector Lockdown	Allowed	Allowed	Allowed
Freeze Sector Lockdown State	Not Allowed	Not Allowed	Not Allowed
Program Security Register	Not Allowed	Not Allowed	Not Allowed

Table 4-8. Operations Allowed and Not Allowed During Suspend *(continued)*

Command	Operation During Program Suspend in Buffer 1 (PS1)	Operation During Program Suspend in Buffer 2 (PS2)	Operation During Erase Suspend (ES)
Read Security Register	Allowed	Allowed	Allowed
Additional Commands			
Main Memory to Buffer 1 Transfer	Not Allowed	Allowed	Allowed
Main Memory to Buffer 2 Transfer	Allowed	Not Allowed	Allowed
Main Memory to Buffer 1 Compare	Not Allowed	Allowed	Allowed
Main Memory to Buffer 2 Compare	Allowed	Not Allowed	Allowed
Enter Deep Power-Down	Not Allowed	Not Allowed	Not Allowed
Resume from Deep Power-Down	Not Allowed	Not Allowed	Not Allowed
Enter Ultra-Deep Power-Down mode	Not Allowed	Not Allowed	Not Allowed
Read Configuration Register	Allowed	Allowed	Allowed
Read Status Register	Allowed	Allowed	Allowed
Read Manufacturer and Device ID	Allowed	Allowed	Allowed
Reset (via Hardware or Software)	Allowed	Allowed	Allowed

4.3.5 Program/Erase Resume

When the $\overline{CS}$ pin is deasserted, the currently suspended program or erase operation resumes within a time of t_{RES}. The PS1 bit, PS2 bit, or ES bit in the Status Register is then reset back to a Logic 0 state to indicate that the program or erase operation is no longer suspended. In addition, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy performing a program or erase operation.

During a simultaneous Erase Suspend/Program Suspend condition, issuing the Program/Erase Resume command results in the program operation resuming first. After the program operation has been completed, the Program/Erase Resume command must be issued again in order for the erase operation to be resumed.

While the device is busy resuming a program or erase operation, any attempts at issuing the Program/Erase Suspend command is ignored. Therefore, if a resumed program or erase operation needs to be subsequently suspended again, the system must either wait the entire t_{RES} time before issuing the Program/Erase Suspend command, or it must check the status of the RDY/$\overline{BUSY}$ bit or the appropriate PS1, PS2, or ES bit in the Status Register to determine if the previously suspended program or erase operation has resumed.

4.4 Additional Commands

This section describes the following additional commands:

— Main Memory Page to Buffer Transfer

— Main Memory Page to Buffer Compare

— Auto-page Rewrite

— Status Register Read

— Configuration Register Read

— Configuration Register Write

These commands are defined in Table 4-11 below.

Table 4-9. Additional Commands

Command	Opcode	Description
Main Memory Page to Buffer 1 Transfer	53h	Transfer a page of data from the main memory to Buffer 1 or Buffer 2. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode and the three address bytes from the input pin (SI). The transfer of the page of data from the main memory to the buffer begins when the CS pin transitions from a low to a high state. During the page transfer time (t_{XFR}), the RDY/BUSY bit in the Status Register can be read to determine whether or not the transfer has been completed.
Main Memory Page to Buffer 2 Transfer	55h	
Main Memory Page to Buffer 1 Compare	60h	A page of data in main memory can be compared to the data in Buffer 1 or Buffer 2 as a method to ensure that data was successfully programmed after a Buffer to Main Memory Page Program command. The $\overline{CS}$ pin must be low while toggling the SCK pin to load the opcode and the address bytes from the input pin (SI). On the low-to-high transition of the $\overline{CS}$ pin, the data bytes in the selected Main Memory Page are compared with the data bytes in Buffer 1 or Buffer 2. During the compare time (t_{COMP}), the RDY/BUSY bit in the Status Register indicates that the part is busy. On completion of the compare operation, hardware updates bit 6 of the Status Register with the result of the compare.
Main Memory Page to Buffer 2 Compare	61h	

Table 4-9. Additional Commands *(continued)*

Command	Opcode	Description
Byte Write Read-Modify-Write Auto-page Rewrite	58h (Buffer 1) 59h (Buffer 2)	The Auto Page Rewrite command contains the same hex value as the Byte Write and Read-Modify-Write commands and can be used in multiple ways. The Auto Page Rewrite command is a combination of the Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-In Erase commands. With the Auto Page Rewrite command, a page of data is first transferred from the main memory to Buffer 1 or Buffer 2. The same data (from Buffer 1 or Buffer 2) is then programmed back into the same page of main memory, essentially “refreshing” the contents of that page. This command only needs to be used if the possibility exists that static (non-changing) data may be stored in a page or pages of a sector and the other pages of the same sector are erased and programmed a large number of times. Applications that modify data in a random fashion within a sector may fall into this category. To preserve data integrity of a sector, each page within a sector must be updated/rewritten at least once within every 50,000 cumulative page erase/program operations within that sector. The Auto Page Rewrite command provides a simple and efficient method to “refresh” a page in the main memory array in a single operation. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part first transfers data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the RDY/BUSY Status Register indicates that the part is busy. If a sector is programmed or reprogrammed sequentially page by page and the possibility does not exist that there is a page(s) of static data, then the programming algorithm shown in Figure 23-1 is recommended. Otherwise, if there is a chance that there may be a page or pages of a sector that contains static data, then the programming algorithm shown in Figure 23-2 is recommended. Please contact Adesto for availability of devices that are specified to exceed the 50,000 cycle cumulative limit. Note that the Auto Page Rewrite command uses the same opcodes as the Read-Modify-Write command. If data bytes are clocked into the device, then the device performs a Read-Modify-Write operation. See the Read-Modify-Write command description for more details.
Status Register Read	D7h	The 2-byte Status Register can be used to determine the device's ready/busy status, page size, a Main Memory Page to Buffer Compare operation result, the sector protection status, Freeze Sector Lockdown status, erase/program error status, Program/Erase Suspend status, and the device density. The Status Register can be read at any time, including during an internally self-timed program or erase operation. Refer to Section 4.4.1 for more information.
Configuration Register Read	3Fh	The non-volatile Configuration Register can be used to determine if the Quad-input Buffer 1 or 2 Write and Quad-output Read Array commands have been enabled. Unlike the Status Register, the Configuration Register can only be read when the device is in an idle state (when the RDY/ BUSY bit of the Status Register indicates that the device is in a ready state). Refer to Section 4.4.2 for more information.

Table 4-9. Additional Commands *(continued)*

Command	Opcode	Description
Configuration Register Write	3Fh	The Write Configuration Register commands are used to modify the QE bit of the non-volatile Configuration Register. There are two commands that are utilized to enable and disable the Quad I/O functionality of the device and they are the Quad Enable and Quad Disable commands, respectively. Refer to Section 4.4.3 for more information.
Quad Enable	3Dh, 2Ah, 81h, 66h	The Quad Enable command is used to program the QE bit of the non-volatile Configuration Register to a Logical 1 to enable the Quad I/O functionality of the device. Refer to Section 4.4.4 for more information.
Quad Disable	3Dh, 2Ah, 81h, 67h	The Quad Disable command is used to program the QE bit of the non-volatile Configuration Register to a Logical 0 to disable the Quad I/O functionality of the device. Refer to Section 4.4.5 for more information.
Active Status Interrupt	25h	The Active Status Interrupt command eliminates the need continuously read the Status register to determine when the operation has finished. With the active status interrupt, the microcontroller need only monitor the value of the MISO pin. If the MISO pin is connected to an interrupt line on the host controller, the host controller may be in sleep mode until the SO pin indicates that the device is ready for the next command. Refer to Section 4.4.6 for more information.
Software Reset	F0h, 00h, 00h, 00h	To perform a Software Reset, the CS pin must be asserted and a 4-byte command sequence of F0h, 00h, 00h, and 00h. For more information, refer to Section 10.

Table 4-10. AT45DB322F Standard and Binary Device Additional Operations

Operation	Opcode	Page Size	Address			Number of Dummy Bytes
			Total Number of Address Bits	Page Address	Starting Byte within Page	
Main Memory Page to Buffer 1 Transfer	53h	264	24	PA[14:0]	BFA[8:0] (dummy)	0
	53h	256	23	A[22:8]	BFA[7:0] (dummy)	0
Main Memory Page to Buffer 2 Transfer	55h	264	24	PA[14:0]	BFA[8:0] (dummy)	0
	55h	256	23	A[22:8]	BFA[7:0] (dummy)	0
Main Memory Page to Buffer 1 Compare	60h	264	24	PA[14:0]	BFA[8:0] (dummy)	0
	60h	256	23	A[22:8]	BFA[7:0] (dummy)	0
Main Memory Page to Buffer 2 Compare	61h	264	24	PA[14:0]	BFA[8:0] (dummy)	0
	61h	256	23	A[22:8]	BFA[7:0] (dummy)	0
Byte Write/Read-Modify-Write/Auto Page Rewrite to Buffer 1	58h	264	24	PA[14:0]	BFA[8:0] (dummy)	0
	58h	256	23	A[22:8]	BFA[7:0] (dummy)	0

Table 4-10. AT45DB322F Standard and Binary Device Additional Operations *(continued)*

Operation	Opcode	Page Size	Address			Number of Dummy Bytes
			Total Number of Address Bits	Page Address	Starting Byte within Page	
Byte Write/Read-Modify-Write/Auto Page Rewrite to Buffer 2	59h	264	24	PA[14:0]	BFA[8:0] (dummy)	0
	59h	256	23	A[22:8]	BFA[7:0] (dummy)	0
Status Register Read	D7h	264	--	--	--	--
	D7h	256	--	--	--	--
Configuration Register Read	3Fh	264	--	--	--	--
	3Fh	256	--	--	--	--

4.4.1 Status Register Read

To read the Status Register, the $\overline{CS}$ pin must first be asserted and then the opcode D7h must be clocked into the device. After the opcode has been clocked in, the device begins outputting Status Register data on the SO pin during every subsequent clock cycle. After the second byte of the Status Register has been clocked out, the sequence repeats itself, starting again with the first byte of the Status Register, as long as the $\overline{CS}$ pin remains asserted and the clock pin is being pulsed. The data in the Status Register is constantly being updated, so each repeating sequence may output new data. The RDY/$\overline{BUSY}$ status is available for both bytes of the Status Register and is updated for each byte.

Deasserting the $\overline{CS}$ pin terminates the Status Register Read operation and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

Table 4-11. Status Register Format — Byte 1

Bit	Name		Type[1]	Description	
7	RDY/$\overline{BUSY}$	Ready/Busy Status	R	0	Device is busy with an internal operation.
				1	Device is ready.
6	COMP	Compare Result	R	0	Main memory page data matches buffer data.
				1	Main memory page data does not match buffer data.
5:2	DENSITY	Density Code	R	1101	32-Mbit
1	PROTECT	Sector Protection Status	R	0	Sector protection is disabled.
				1	Sector protection is enabled.
0	PAGE SIZE	Page Size Configuration	R	0	Device is configured for standard DataFlash page size (264 bytes).
				1	Device is configured for “power of 2” binary page size (256 bytes).

Note: 1. R = Readable only

Table 4-12. Status Register Format – Byte 2

Bit	Name		Type[1]	Description	
7	RDY/$\overline{\text{BUSY}}$	Ready/Busy Status	R	0	Device is busy with an internal operation.
				1	Device is ready.
6	RES	*Reserved for Future Use*	R	0	*Reserved for future use.*
5	EPE	Erase/Program Error	R	0	Erase or program operation was successful.
				1	Erase or program error detected.
4	RES	*Reserved for Future Use*	R	0	*Reserved for future use.*
3	SLE	Sector Lockdown Enabled	R	0	Sector Lockdown command is disabled.
				1	Sector Lockdown command is enabled.
2	PS2	Program Suspend Status (Buffer 2)	R	0	No program operation has been suspended while using Buffer 2.
				1	A sector is program suspended while using Buffer 2.
1	PS1	Program Suspend Status (Buffer 1)	R	0	No program operation has been suspended while using Buffer 1.
				1	A sector is program suspended while using Buffer 1.
0	ES	Erase Suspend	R	0	No sectors are erase suspended.
				1	A sector is erase suspended.

Note: 1. R = Readable only

4.4.1.1 RDY/$\overline{\text{BUSY}}$ Bit

The RDY/$\overline{\text{BUSY}}$ bit is used to determine whether or not an internal operation, such as a program or erase, is in progress. To poll the RDY/$\overline{\text{BUSY}}$ bit to detect the completion of an internally timed operation, new Status Register data must be continually clocked out of the device until the state of the RDY/$\overline{\text{BUSY}}$ bit changes from a Logic 0 to a Logic 1.

4.4.1.2 COMP Bit

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using the COMP bit. If the COMP bit is a Logic 1, then at least one bit of the data in the Main Memory Page does not match the data in the buffer.

4.4.1.3 DENSITY Bits

The device density is indicated using the DENSITY bits. For the AT45DB322F, the four bit binary value is 1101. The decimal value of these four binary bits does not actually equate to the device density; the four bits represent a combinational code relating to differing densities of DataFlash devices. The DENSITY bits are not the same as the density code indicated in the JEDEC Device ID information. The DENSITY bits are provided only for backward compatibility to older generation DataFlash devices.

4.4.1.4 PROTECT Bit

The PROTECT bit provides information to the user on whether or not the sector protection has been enabled or disabled, either by the software-controlled method or the hardware-controlled method.

4.4.1.5 PAGE SIZE Bit

The PAGE SIZE bit indicates whether the buffer size and the page size of the main memory array is configured for the “power of 2” binary page size (256 bytes) or the standard DataFlash page size (264 bytes).

4.4.1.6 EPE Bit

The EPE bit indicates whether the last erase or program operation completed successfully or not. If at least one byte during the erase or program operation did not erase or program properly, then the EPE bit is set to the Logic 1 state. The EPE bit is not set if an erase or program operation aborts for any reason, such as an attempt to erase or program a protected region or a locked down sector or an attempt to erase or program a suspended sector. The EPE bit is updated after every erase and program operation.

4.4.1.7 SLE Bit

The SLE bit indicates whether or not the Sector Lockdown command is enabled or disabled. If the SLE bit is a Logic 1, then the Sector Lockdown command is still enabled and sectors can be locked down. If the SLE bit is a Logic 0, then the Sector Lockdown command has been disabled and no further sectors can be locked down.

4.4.1.8 PS2 Bit

The PS2 bit indicates if a program operation has been suspended while using Buffer 2. If the PS2 bit is a Logic 1, then a program operation has been suspended while Buffer 2 was being used, and any command attempts that would modify the contents of Buffer 2 is ignored.

4.4.1.9 PS1 Bit

The PS1 bit indicates if a program operation has been suspended while using Buffer 1. If the PS1 bit is a Logic 1, then a program operation has been suspended while Buffer 1 was being used, and any command attempts that would modify the contents of Buffer 1 is ignored.

4.4.1.10 The ES bit

The ES bit indicates whether or not an erase has been suspended. If the ES bit is a Logic 1, then an erase operation (page, block, sector, or chip) has been suspended.

4.4.2 Read Configuration Register

To read the Configuration Register, the $\overline{CS}$ pin must first be asserted and the opcode of 3Fh must be clocked into the device. After the opcode has been clocked in, the device begins outputting one byte of Configuration Register data on the SO pin during subsequent clock cycles. The data being output is a repeating byte as long as the $\overline{CS}$ pin remains asserted and the clock pin is being pulsed.

At clock frequencies above f_{SCK}, the first byte of data output is not valid. Therefore, if operating at clock frequencies above f_{SCK}, at least two bytes of data must be clocked out from the device in order to determine the correct value of the Configuration Register.

Deasserting the $\overline{CS}$ pin will terminate the Read Configuration Register operation and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

The Configuration Register is a non-volatile register; therefore, the contents of the Configuration Register are not affected by power cycles or power-on reset operations.

Table 4-13. Configuration Register Format

Bit	Name		Type	Description	
7	QE	Quad Enable	R/W	0	Quad-input/output commands and operation disabled.
				1	Quad-input/output commands and operation enabled. ($\overline{WP}$ and $\overline{RESET}$ disabled)
6:4	*RES*	*Reserved for Future Use*	R	0	Reserved for future use.
3	*RES*	*Reserved for Future Use*	R	1	Reserved for future use.
2:0	*RES*	*Reserved for Future Use*	R	0	Reserved for future use.

Note: 1. Only bit seven of the Configuration Register will be modified when using the Quad Enable/Disable commands.

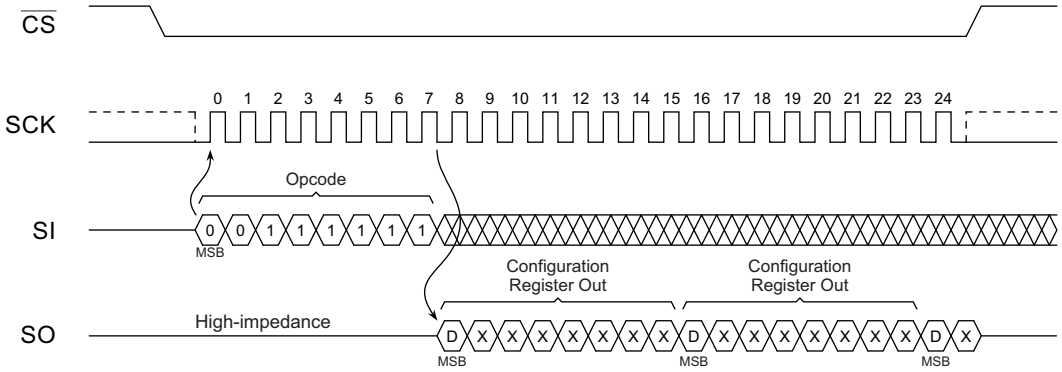
4.4.2.1 QE Bit

The QE bit is used to control whether the Quad-input Buffer 1 Write or Buffer 2 Write and the Quad-output Read Array commands are enabled or disabled. When the QE bit is in the Logical 1 state, the Quad-input Buffer Write and Quad-output Read Array commands are enabled and will be recognized by the device. In addition, the $\overline{WP}$ and $\overline{RESET}$ functions are disabled and the $\overline{WP}$ and $\overline{RESET}$ pins themselves operate as a bidirectional input/output pins ($\overline{WP}$ is I/O_2 and $\overline{RESET}$ is I/O_3).

When the QE bit is in the Logical 0 state, the Quad-Input Buffer Write and Quad-output Read Array commands are disabled and will not be recognized by the device as valid commands and the $\overline{WP}$ and $\overline{RESET}$ pins function as normal control pins. The $\overline{WP}$ and $\overline{RESET}$ pins should be externally pulled-high to avoid erroneous or unwanted device operation.

The Reset command has no effect on the QE bit. The QE bit defaults to the Logical 0 state when devices are initially shipped from Adesto.

Figure 4-2. Read Configuration Register



4.4.3 Write Configuration Register

The Configuration Register is a non-volatile register and is subject to the same program/erase endurance characteristics of the Main Memory Array. The programming of the Configuration Register is internally self-timed and should take place in a time of $t_{WRCR.}$ While the Configuration Register is being updated, the Status Register can be read and will indicate that the device is busy. For faster throughput, it is recommended that the Status Register be polled rather than waiting the t_{WRCR} time to determine if the Configuration Register has completed the programming cycle.

The Write Configuration Register (Quad Enable and Quad Disable) is subject to a limit of 10,000 cycles. Users are encouraged to carefully evaluate the number of times the Write Configuration Register will be modified during the course of the application's life cycle.

4.4.4 Quad Enable Command

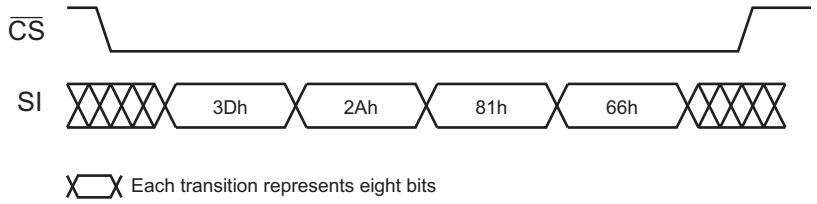
The Quad Enable command is used to program the QE bit of the non-volatile Configuration Register to a Logical 1 to enable the Quad I/O functionality of the device. To issue the Quad Enable command, the $\overline{CS}$ pin must first be asserted followed by a four byte opcode of 3Dh, 2Ah, 81h, and 66h.

After the last bit of the four byte opcode has been clocked in, the $\overline{CS}$ pin must be deasserted allowing the QE bit of the Configuration Register to be modified within the time of t_{WRCR}.

Table 4-14. Quad Enable Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Quad Enable	3Dh	2Ah	81h	66h

Figure 4-3. Quad Enable



4.4.5 Quad Disable Command

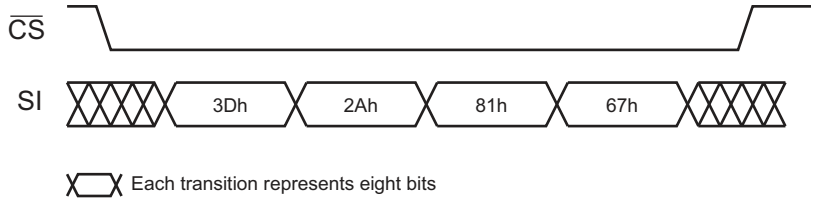
The Quad Disable command is used to program the QE bit of the non-volatile Configuration Register to a Logical 0 to disable the Quad I/O functionality of the device. To issue the Quad Disable command, the $\overline{CS}$ pin must first be asserted followed by a four byte opcode of 3Dh, 2Ah, 81h and 67h.

After the last bit of the four byte opcode has been clocked in, the $\overline{CS}$ pin must be deasserted allowing the QE bit of the Configuration Register to be modified within the time of t_{WRCR}.

Table 4-15. Quad Disable Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Quad Disable	3Dh	2Ah	81h	67h

Figure 4-4. Quad Disable



4.4.6 Active Status Interrupt

To simplify the readout of the RDY/BSY bit, the Active Status Interrupt command (25h) may be used. This command eliminates the need continuously read the status register to determine when the operation has finished. With the active status interrupt, the microcontroller need only monitor the value of the MISO pin. If the SO pin is connected to an interrupt line on the host controller, the host controller may be in sleep mode until the SO pin indicates that the AT45DB322F is ready for the next command.

The RDY/BSY bit can be read at any time, including during an internally self-timed program or erase operation.

To enable the Active Status Interrupt command, the active-low $\overline{CS}$ pin must first be asserted (driven low) and the opcode of 25h must be clocked into the device. For SPI Mode3, at least one dummy bit has to be clocked into the device after the last bit of the opcode has been clocked in. In most cases, this is most easily done by sending a dummy byte to the device. The value of the SI line after the opcode is clocked in is of no significance to the operation. For SPI Mode 0, this dummy bit (dummy byte) is not required.

The value of RDY/BSY is then output on the SO line, and is continuously updated by the device for as long as the $\overline{CS}$ pin remains asserted. Additional clocks on the SCK pin are not required. If the RDY/BSY bit changes from 1 to 0 while the $\overline{CS}$ pin is asserted, the MISO line changes from 1 to 0. (The RDY/BSY bit cannot change from 0 to 1 during an operation, so if the SO line already is 0, it will not change.)

Driving the $\overline{CS}$ pin high terminates the Active Status Interrupt operation and places the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

5. Sector Protection

Two protection methods, hardware and software controlled, are provided for protection against inadvertent or erroneous program and erase cycles. The software controlled method relies on the use of software commands to enable and disable sector protection while the hardware controlled method employs the use of the Write Protect ($\overline{WP}$) pin. The selection of which sectors that are to be protected or unprotected against program and erase operations is specified in the Nonvolatile Sector Protection Register. The status of whether or not sector protection has been enabled or disabled by either the software or the hardware controlled methods can be determined by checking the Status Register.

5.1 Software Sector Protection

Software controlled protection is useful in applications in which the $\overline{WP}$ pin is not or cannot be controlled by a host processor. In such instances, the $\overline{WP}$ pin may be left floating (the $\overline{WP}$ pin is internally pulled high) and sector protection can be controlled using the Enable Sector Protection and Disable Sector Protection commands.

If the device is power cycled, then the software controlled protection is disabled. Once the device is powered up, the Enable Sector Protection command should be reissued if sector protection is desired and if the $\overline{WP}$ pin is not used.

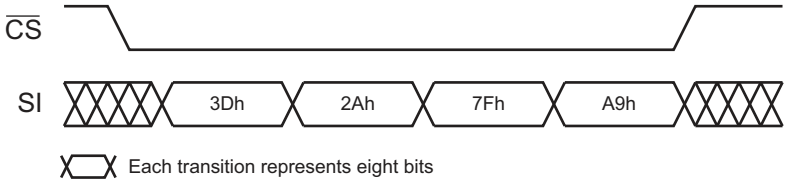
5.1.1 Enable Sector Protection

Sectors specified for protection in the Sector Protection Register can be protected from program and erase operations by issuing the Enable Sector Protection command. To enable the sector protection, a 4-byte command sequence of 3Dh, 2Ah, 7Fh, and A9h must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to enable the Sector Protection.

Table 5-1. Enable Sector Protection Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Enable Sector Protection	3Dh	2Ah	7Fh	A9h

Figure 5-1. Enable Sector Protection



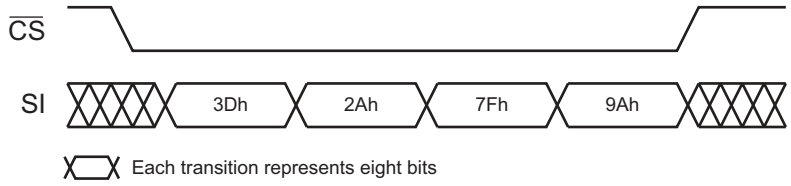
5.1.2 Disable Sector Protection

To disable the sector protection, a 4-byte command sequence of 3Dh, 2Ah, 7Fh, and 9Ah must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to disable the sector protection.

Table 5-2. Disable Sector Protection Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Disable Sector Protection	3Dh	2Ah	7Fh	9Ah

Figure 5-2. Disable Sector Protection



5.2 Hardware Controlled Protection

Sectors specified for protection in the Sector Protection Register and the Sector Protection Register itself can be protected from program and erase operations by asserting the $\overline{WP}$ pin and keeping the pin in its asserted state. The Sector Protection Register and any sector specified for protection cannot be erased or programmed as long as the $\overline{WP}$ pin is asserted. In order to modify the Sector Protection Register, the $\overline{WP}$ pin must be deasserted. If the $\overline{WP}$ pin is permanently connected to GND, then the contents of the Sector Protection Register cannot be changed. If the $\overline{WP}$ pin is deasserted or permanently connected to V_{CC}, then the contents of the Sector Protection Register can be modified.

The $\overline{WP}$ pin overrides the software controlled protection method but only for protecting the sectors.

Example: If the sectors were not previously protected by the Enable Sector Protection command, then simply asserting the $\overline{WP}$ pin would enable the sector protection within the maximum specified t_{WPE} time. When the $\overline{WP}$ pin is deasserted, however, the sector protection would no longer be enabled (after the maximum specified t_{WPD} time) as long as the Enable Sector Protection command was not issued while the $\overline{WP}$ pin was asserted. If the Enable Sector Protection command was issued before or while the $\overline{WP}$ pin was asserted, then simply deasserting the $\overline{WP}$ pin would not disable the sector protection. In this case, the Disable Sector Protection command would need to be issued while the $\overline{WP}$ pin is deasserted to disable the sector protection. The Disable Sector Protection command is also ignored whenever the $\overline{WP}$ pin is asserted.

A noise filter is incorporated to help protect against spurious noise that may inadvertently assert or deassert the $\overline{WP}$ pin.

Figure 5-3 and Table 5-3 detail the sector protection status for various scenarios of the $\overline{WP}$ pin, the Enable Sector Protection command, and the Disable Sector Protection command.

Figure 5-3. $\overline{WP}$ Pin and Protection Status

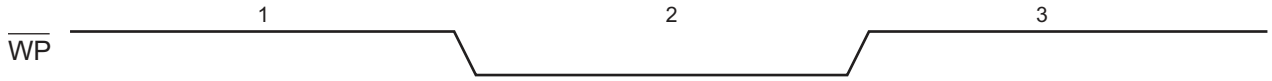


Table 5-3. $\overline{WP}$ Pin and Protection Status

Time Period	$\overline{WP}$ Pin	Enable Sector Protection Command	Disable Sector Protection Command	Sector Protection Status	Sector Protection Register
1	High	Command Not Issued Previously	X	Disabled	Read/Write
		—	Issue Command	Disabled	Read/Write
		Issue Command	—	Enabled	Read/Write
2	Low	X	X	Enabled	Read
3	High	Command Issued During Period 1 or 2	Not Issued Yet	Enabled	Read/Write
		—	Issue Command	Disabled	Read/Write
		Issue Command	—	Enabled	Read/Write

5.3 Sector Protection Register

The nonvolatile Sector Protection Register specifies which sectors are to be protected or unprotected with either the software or hardware controlled protection methods. The Sector Protection Register contains thirty two bytes of data, of which byte locations zero through thirty one contain values that specify whether Sectors 0 through 31 is protected or unprotected. The Sector Protection Register is user modifiable and must be erased before it can be reprogrammed. Table 5-4 illustrates the format of the Sector Protection Register.

Table 5-4. Sector Protection Register

Sector Number	0 (0a, 0b)	1 to 31
Protected	See Table 5-5	FFh
Unprotected		00h

Note: 1. The default values for bytes 0 through 31 are 00h when shipped from Adesto.

Table 5-5. Sector 0 (0a, 0b) Sector Protection Register Byte Value

	Bit 7:6	Bit 5:4	Bit 3:2	Bit 1:0	
	Sector 0a (Page 0-7)	Sector 0b (Page 8-1023)	N/A	N/A	Data Value
Sectors 0a and 0b Unprotected	00	00	XX	XX	0xh
Protect Sector 0a	11	00	XX	XX	Cxh
Protect Sector 0b	00	11	XX	XX	3xh
Protect Sectors 0a and 0b	11	11	XX	XX	Fxh

Note: 1. x = Don't care

5.3.1 Erase Sector Protection Register

In order to modify and change the values of the Sector Protection Register, it must first be erased using the Erase Sector Protection Register command.

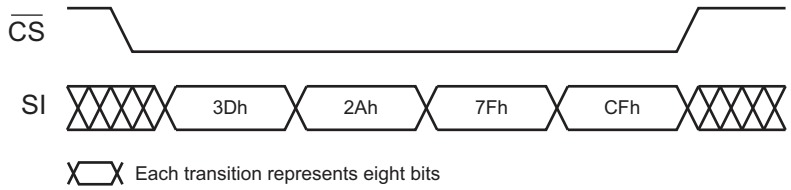
To erase the Sector Protection Register, a 4-byte command sequence of 3Dh, 2Ah, 7Fh, and CFh must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed erase cycle. The erasing of the Sector Protection Register should take place in a maximum time of t_{PE}. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy. If the device is powered-down before the completion of the erase cycle, then the contents of the Sector Protection Register cannot be guaranteed.

The Sector Protection Register can be erased with sector protection enabled or disabled. Since the erased state (FFh) of each byte in the Sector Protection Register is used to indicate that a sector is specified for protection, leaving the sector protection enabled during the erasing of the register allows the protection scheme to be more effective in the prevention of accidental programming or erasing of the device. If for some reason an erroneous program or erase command is sent to the device immediately after erasing the Sector Protection Register and before the register can be reprogrammed, then the erroneous program or erase command is not processed because all sectors would be protected.

Table 5-6. Erase Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Erase Sector Protection Register	3Dh	2Ah	7Fh	CFh

Figure 5-4. Erase Sector Protection Register



5.3.2 Program Sector Protection Register

Once the Sector Protection Register has been erased, it can be reprogrammed using the Program Sector Protection Register command.

To program the Sector Protection Register, a 4-byte command sequence of 3Dh, 2Ah, 7Fh, and FCh must be clocked into the device followed by thirty two bytes of data corresponding to Sectors 0 through 31. After the last bit of the opcode sequence and data have been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed program cycle. The programming of the Sector Protection Register should take place in a maximum time of t_P. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy. If the device is powered-down before the completion of the erase cycle, then the contents of the Sector Protection Register cannot be guaranteed.

If the proper number of data bytes is not clocked in before the $\overline{CS}$ pin is deasserted, then the protection status of the sectors corresponding to the bytes not clocked in cannot be guaranteed.

Example: If only the first two bytes are clocked in instead of the complete thirty two bytes, then the protection status of the last thirty sectors cannot be guaranteed. Furthermore, if more than thirty two bytes of data is clocked into the device, then the data wraps back around to the beginning of the register. For instance, if thirty three bytes of data are clocked in, then the thirty third byte is stored at byte location 0 of the Sector Protection Register.

The data bytes clocked into the Sector Protection Register need to be valid values (0xh, 3xh, Cxh, and Fxh for Sector 0a or Sector 0b, and 00h or FFh for other sectors) in order for the protection to function correctly. If a non-valid value is clocked into a byte location of the Sector Protection Register, then the protection status of the sector corresponding to that byte location cannot be guaranteed.

Example: If a value of 17h is clocked into byte location 2 of the Sector Protection Register, then the protection status of Sector 2 cannot be guaranteed.

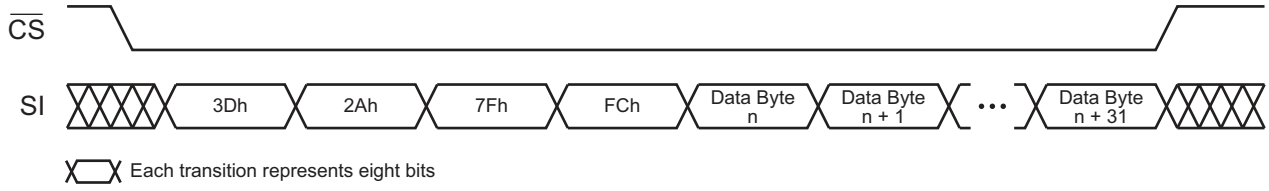
The Sector Protection Register can be reprogrammed while the sector protection is enabled or disabled. Being able to reprogram the Sector Protection Register with the sector protection enabled allows the user to temporarily disable the sector protection to an individual sector rather than disabling sector protection completely.

The Program Sector Protection Register command utilizes Buffer 1 for processing. Therefore, the contents of Buffer 1 is altered from its previous state when this command is issued.

Table 5-7. Program Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Program Sector Protection Register	3Dh	2Ah	7Fh	FCh

Figure 5-5. Program Sector Protection Register



5.3.3 Read Sector Protection Register

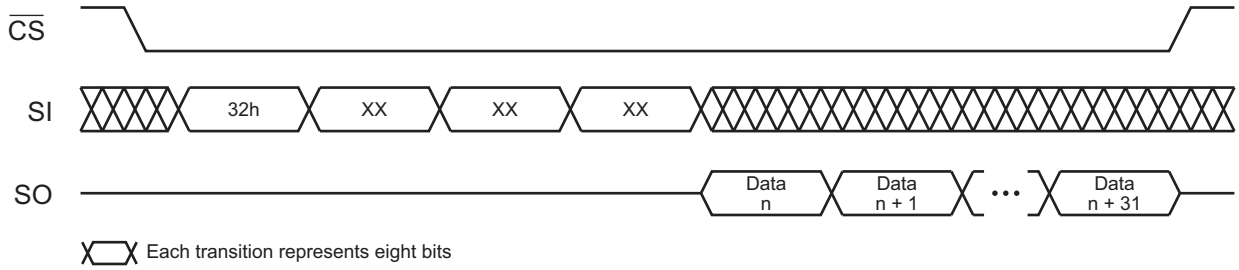
To read the Sector Protection Register, an opcode of 32h and three dummy bytes must be clocked into the device. After the last bit of the opcode and dummy bytes have been clocked in, any additional clock pulses on the SCK pin results in the Sector Protection Register contents being output on the SO pin. The first byte (byte location 0) corresponds to Sector 0 (0a and 0b), the second byte corresponds to Sector 1, and the last byte (byte location 31) corresponds to Sector 31. Once the last byte of the Sector Protection Register has been clocked out, any additional clock pulses result in undefined data being output on the SO pin. The $\overline{CS}$ pin must be deasserted to terminate the Read Sector Protection Register operation and put the output into a high-impedance state.

Table 5-8. Read Sector Protection Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Read Sector Protection Register	32h	XXh	XXh	XXh

Note: 1. XX = Dummy byte

Figure 5-6. Read Sector Protection Register



5.3.4 About the Sector Protection Register

The Sector Protection Register is subject to a limit of 10,000 erase/program cycles. Users are encouraged to carefully evaluate the number of times the Sector Protection Register is modified during the course of the application's life cycle. If the application requires that the Security Protection Register be modified more than the specified limit of 10,000 cycles because the application needs to temporarily unprotect individual sectors (sector protection remains enabled while the Sector Protection Register is reprogrammed), then the application must limit this practice. Instead, a combination of temporarily unprotecting individual sectors along with disabling sector protection completely must be implemented by the application to ensure that the limit of 10,000 cycles is not exceeded.

6. Security Features

6.1 Sector Lockdown

The device incorporates a sector lockdown mechanism that allows each individual sector to be permanently locked so that it becomes read-only (ROM). This is useful for applications that require the ability to permanently protect a number of sectors against malicious attempts at altering program code or security information.

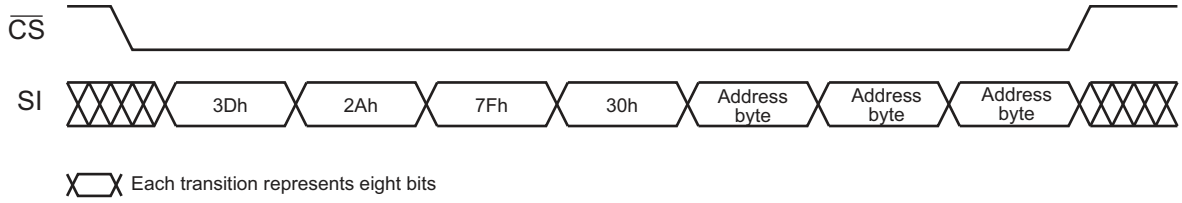
Warning: Once a sector is locked down, it can never be erased or programmed, and it can never be unlocked.

To issue the sector lockdown command, a 4-byte command sequence of 3Dh, 2Ah, 7Fh, and 30h must be clocked into the device followed by three address bytes specifying any address within the sector to be locked down. After the last address bit has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed lockdown sequence. The lockdown sequence should take place in a maximum time of t_P. During this time, the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy. If the device is powered-down before the completion of the lockdown sequence, then the lockdown status of the sector cannot be guaranteed. In this case, it is recommended that the user read the Sector Lockdown Register to determine the status of the appropriate sector lockdown bits or bytes and re-issue the Sector Lockdown command if necessary.

Table 6-1. Sector Lockdown Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Sector Lockdown	3Dh	2Ah	7Fh	30h

Figure 6-1. Sector Lockdown



6.1.1 Read Sector Lockdown Register

The nonvolatile Sector Lockdown Register specifies which sectors in the main memory are currently unlocked or have been permanently locked down. The Sector Lockdown Register is a read-only register and contains thirty two bytes of data which correspond to Sectors 0 through 31. To read the Sector Lockdown Register, an opcode of 35h must be clocked into the device followed by three dummy bytes. After the last bit of the opcode and dummy bytes have been clocked in, the data for the contents of the Sector Lockdown Register is clocked out on the SO pin. The first byte (byte location 0) corresponds to Sector 0 (0a and 0b), the second byte corresponds to Sector 1, and the last byte (byte location 31) corresponds to Sector 31. After the last byte of the Sector Lockdown Register has been read, additional pulses on the SCK pin results in undefined data being output on the SO pin.

Deasserting the $\overline{CS}$ pin terminates the Read Sector Lockdown Register operation and put the SO pin into a high-impedance state. Table 6-2 details the format the Sector Lockdown Register.

Table 6-2. Sector Lockdown Register

Sector Number	0 (0a, 0b)	1 to 31
Locked	See Table	FFh
Unlocked		00h

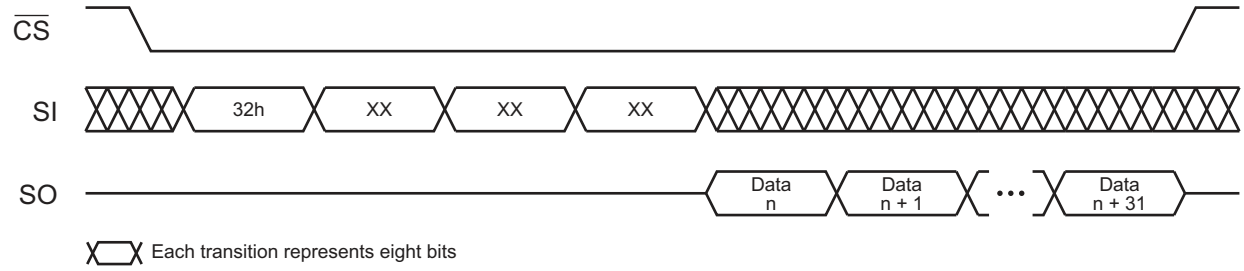
Table 6-3. Sector 0 (0a and 0b) Sector Lockdown Register Byte Value

	Bit 7:6	Bit 5:4	Bit 3:2	Bit 1:0	Data Value
	Sector 0a (Page 0-7)	Sector 0b (Page 8-1023)	N/A	N/A	
Sectors 0a and 0b Unlocked	00	00	00	00	00h
Sector 0a Locked	11	00	00	00	C0h
Sector 0b Locked	00	11	00	00	30h
Sectors 0a and 0b Locked	11	11	00	00	F0h

Table 6-4. Read Sector Lockdown Register Command

Command	Byte 1	Byte 2	Byte 3	Byte 4
Read Sector Lockdown Register	35h	XXh	XXh	XXh

Figure 6-2. Read Sector Lockdown Register



6.1.2 Freeze Sector Lockdown

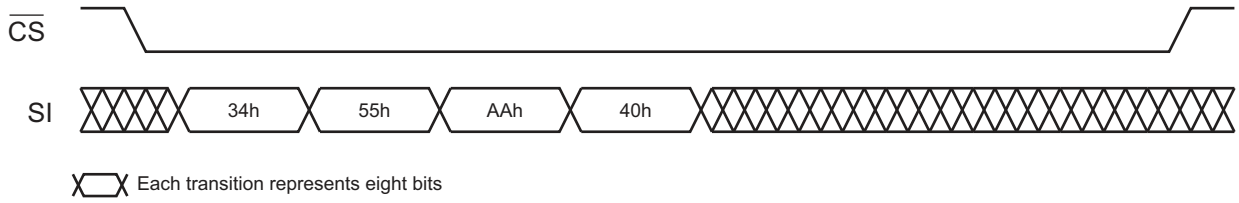
The Sector Lockdown command can be permanently disabled, and the current sector lockdown state can be permanently frozen so that no additional sectors can be locked down aside from those already locked down. Any attempt to issue the Sector Lockdown command after the Sector Lockdown State has been frozen is ignored.

To issue the Freeze Sector Lockdown command, the $\overline{CS}$ pin must be asserted and the opcode sequence of 34h, 55h, AAh, and 40h must be clocked into the device. Any additional data clocked into the device is ignored. When the $\overline{CS}$ pin is deasserted, the current sector lockdown state is permanently frozen within a time of t_{LOCK}. In addition, the SLE bit in the Status Register is permanently reset to a Logic 0 to indicate that the Sector Lockdown command is permanently disabled.

Table 6-5. Freeze Sector Lockdown

Command	Byte 1	Byte 2	Byte 3	Byte 4
Freeze Sector Lockdown	34h	55h	AAh	40h

Figure 6-3. Freeze Sector Lockdown



6.2 Security Register

The device contains a specialized Security Register that can be used for purposes such as unique device serialization or locked key storage. The register is comprised of a total of 128 bytes that is divided into two portions. The first 64 bytes (byte locations 0 through 63) of the Security Register are allocated as a One-Time Programmable space. Once these 64 bytes have been programmed, they cannot be erased or reprogrammed. The remaining 64 bytes of the register (byte locations 64 through 127) are factory programmed by Adesto and contain a unique value for each device. The factory programmed data is fixed and cannot be changed.

Table 6-6. Security Register

	Security Register Byte Number							
	0	1	· · ·	63	64	65	· · ·	127
Data Type	One-Time User Programmable				Factory Programmed by Adesto			

6.2.1 Programming the Security Register

The user programmable portion of the Security Register does not need to be erased before it is programmed.

To program the Security Register, a 4-byte opcode sequence of 9Bh, 00h, 00h, and 00h must be clocked into the device. After the last bit of the opcode sequence has been clocked into the device, the data for the contents of the 64-byte user programmable portion of the Security Register must be clocked in.

After the last data byte has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed program cycle. The programming of the Security Register should take place in a time of t_P, during which time the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy. If the device is powered-down during the program cycle, then the contents of the 64-byte user programmable portion of the Security Register cannot be guaranteed.

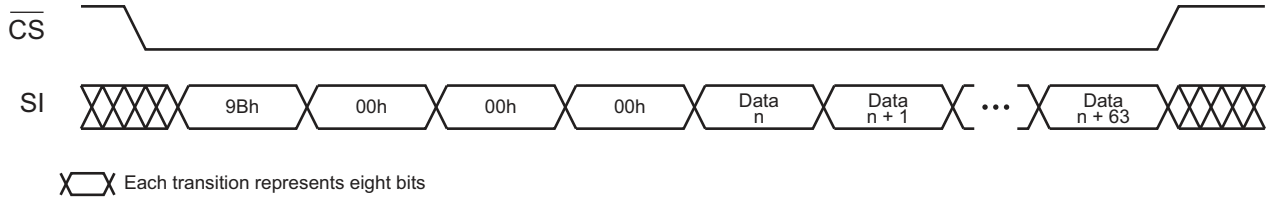
If the full 64 bytes of data are not clocked in before the $\overline{CS}$ pin is deasserted, then the values of the byte locations not clocked in cannot be guaranteed.

Example: If only the first two bytes are clocked in instead of the complete 64 bytes, then the remaining 62 bytes of the user programmable portion of the Security Register cannot be guaranteed. Furthermore, if more than 64 bytes of data is clocked into the device, then the data wraps around to the beginning of the register. For example, if 65 bytes of data are clocked in, then the 65th byte is stored at byte location 0 of the Security Register.

Warning: **The user programmable portion of the Security Register can only be programmed one time.** Therefore, it is not possible, for example, to only program the first two bytes of the register and then program the remaining 62 bytes at a later time.

The Program Security Register command utilizes Buffer 1 for processing. Therefore, the contents of Buffer 1 are altered from its previous state when this command is issued.

Figure 6-4. Program Security Register

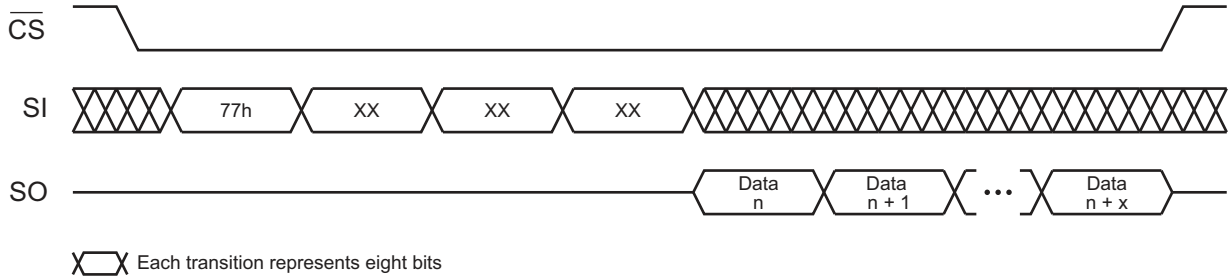


6.2.2 Reading the Security Register

To read the Security Register, an opcode of 77h and three dummy bytes must be clocked into the device. After the last dummy bit has been clocked in, the contents of the Security Register can be clocked out on the SO pin. After the last byte of the Security Register has been read, additional pulses on the SCK pin results in undefined data being output on the SO pin.

Deasserting the $\overline{CS}$ pin terminates the Read Security Register operation and put the SO pin into a high-impedance state.

Figure 6-5. Read Security Register



7. Deep Power-Down

During normal operation, the device is placed in the standby mode to consume less power as long as the $\overline{CS}$ pin remains deasserted and no internal operation is in progress. The Deep Power-Down command offers the ability to place the device into an even lower power consumption state called the Deep Power-Down mode.

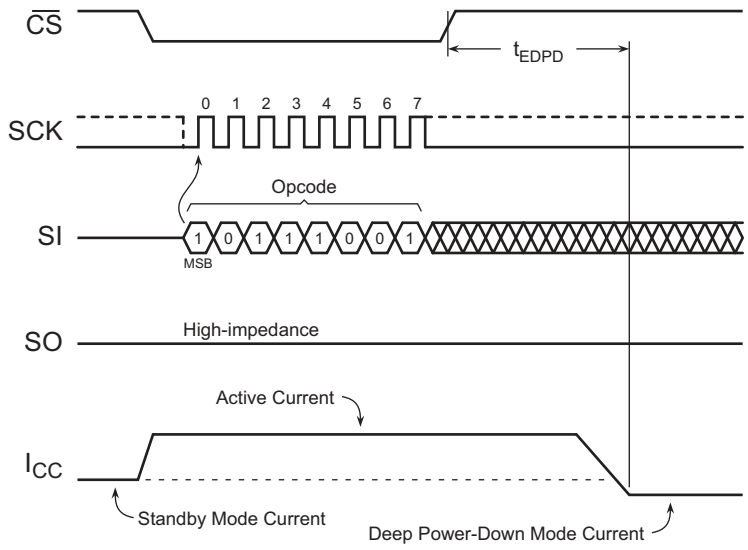
When the device is in the Deep Power-Down mode, all commands including the Status Register Read command are ignored with the exception of the Resume from Deep Power-Down command. Since all commands are ignored, the mode can be used as an extra protection mechanism against program and erase operations.

Entering the Deep Power-Down mode is accomplished by simply asserting the $\overline{CS}$ pin, clocking in the opcode B9h, and then deasserting the $\overline{CS}$ pin. Any additional data clocked into the device after the opcode are ignored. When the $\overline{CS}$ pin is deasserted, the device enters the Deep Power-Down mode within the maximum time of t_{EDPD}.

The complete opcode must be clocked in before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device aborts the operation and return to the standby mode once the $\overline{CS}$ pin is deasserted. In addition, the device defaults to the standby mode after a power cycle.

The Deep Power-Down command is ignored if an internally self-timed operation such as a program or erase cycle is in progress. The Deep Power-Down command must be reissued after the internally self-timed operation has been completed in order for the device to enter the Deep Power-Down mode.

Figure 7-1. Deep Power-Down



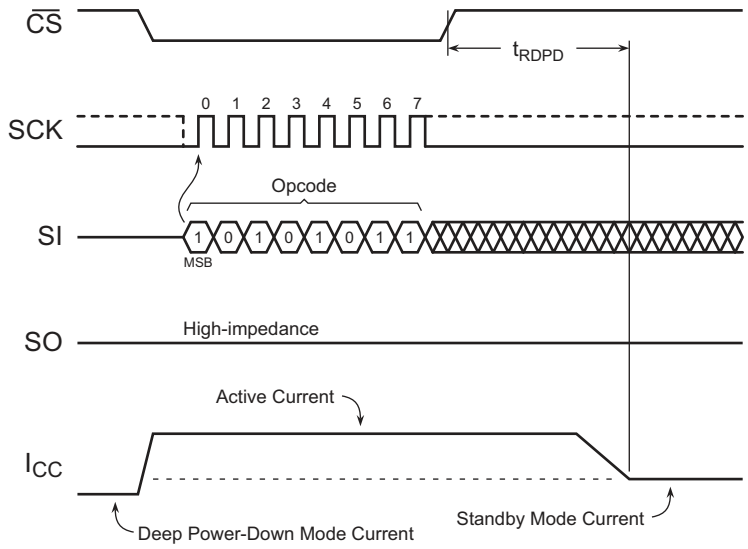
7.1 Resume from Deep Power-Down

In order to exit the Deep Power-Down mode and resume normal device operation, the Resume from Deep Power-Down command must be issued. The Resume from Deep Power-Down command is the only command that the device recognizes while in the Deep Power-Down mode.

To resume from the Deep Power-Down mode, the $\overline{CS}$ pin must first be asserted and then the opcode ABh must be clocked into the device. Any additional data clocked into the device after the opcode is ignored. When the $\overline{CS}$ pin is deasserted, the device exits the Deep Power-Down mode and return to the standby mode within the maximum time of t_{RDPD}. After the device has returned to the standby mode, normal command operations such as Continuous Array Read can be resumed.

If the complete opcode is not clocked in before the $\overline{CS}$ pin is deasserted, or if the $\overline{CS}$ pin is not deasserted on an even byte boundary (multiples of eight bits), then the device aborts the operation and return to the Deep Power-Down mode.

Figure 7-2. Resume from Deep Power-Down



7.2 Ultra-Deep Power-Down

The Ultra-Deep Power-Down mode allows the device to consume far less power compared to the standby and Deep Power-Down modes by shutting down additional internal circuitry. Since almost all active circuitry is shutdown in this mode to conserve power, the contents of the SRAM buffers cannot be maintained. Therefore, any data stored in the SRAM buffers is lost once the device enters the Ultra-Deep Power-Down mode.

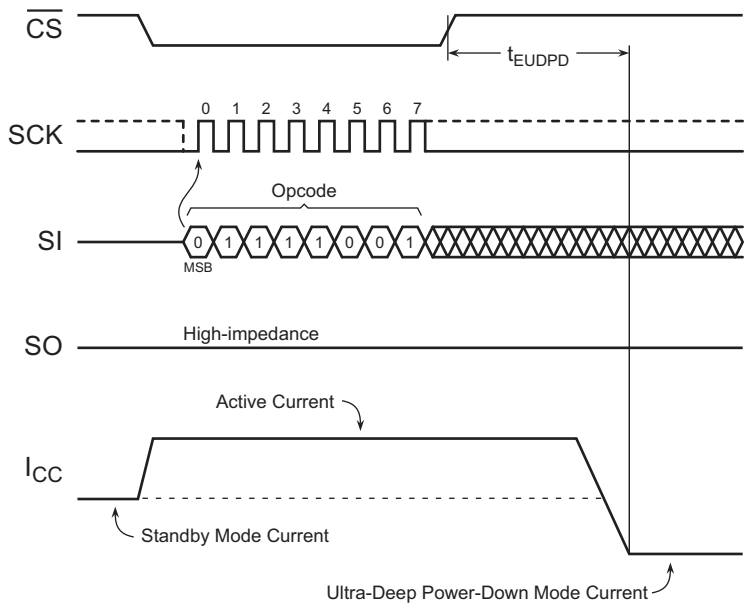
When the device is in the Ultra-Deep Power-Down mode, all commands including the Status Register Read and Resume from Deep Power-Down commands is ignored. Since all commands are ignored, the mode can be used as an extra protection mechanism against program and erase operations.

Entering the Ultra-Deep Power-Down mode is accomplished by simply asserting the $\overline{CS}$ pin, clocking in the opcode 79h, and then deasserting the $\overline{CS}$ pin. Any additional data clocked into the device after the opcode is ignored. When the $\overline{CS}$ pin is deasserted, the device enters the Ultra-Deep Power-Down mode within the maximum time of t_{EUDPD}.

The complete opcode must be clocked in before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device aborts the operation and return to the standby mode once the $\overline{CS}$ pin is deasserted. In addition, the device defaults to the standby mode after a power cycle.

The Ultra-Deep Power-Down command is ignored if an internally self-timed operation such as a program or erase cycle is in progress. The Ultra-Deep Power-Down command must be reissued after the internally self-timed operation has been completed in order for the device to enter the Ultra-Deep Power-Down mode.

Figure 7-3. Ultra-Deep Power-Down

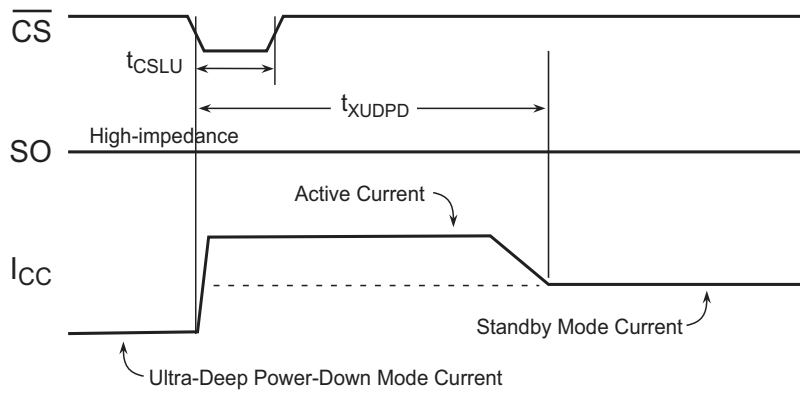


7.2.1 Exit Ultra-Deep Power-Down

To exit from the Ultra-Deep Power-Down mode, the $\overline{CS}$ pin must simply be pulsed by asserting the $\overline{CS}$ pin, waiting the minimum necessary t_{CSLU} time, and then deasserting the $\overline{CS}$ pin again. To facilitate simple software development, a dummy byte opcode can also be entered while the $\overline{CS}$ pin is being pulsed just as in a normal operation like the Program Suspend operation; the dummy byte opcode is simply ignored by the device in this case. After the $\overline{CS}$ pin has been deasserted, the device exits from the Ultra-Deep Power-Down mode and return to the standby mode within a maximum time of t_{XUDPD}. If the $\overline{CS}$ pin is reasserted before the t_{XUDPD} time has elapsed in an attempt to start a new operation, then that operation is ignored and nothing is performed. The system must wait for the device to return to the standby mode before normal command operations such as Continuous Array Read can be resumed.

Since the contents of the SRAM buffers cannot be maintained while in the Ultra-Deep Power-Down mode, the SRAM buffers contain undefined data when the device returns to the standby mode.

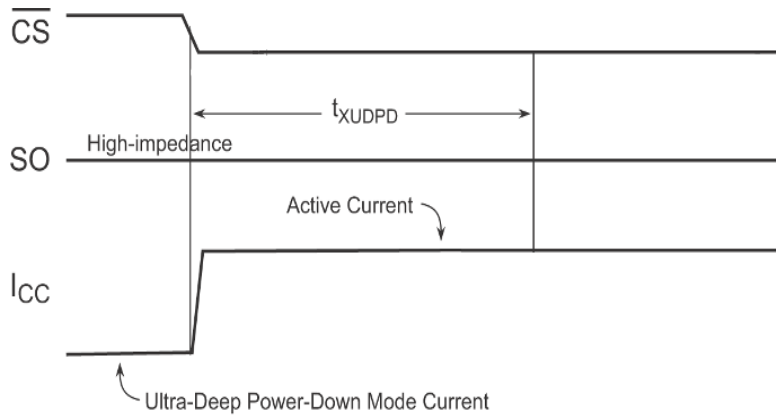
Figure 7-4. Exit Ultra-Deep Power-Down



Chip Select Low

By asserting the $\overline{CS}$ pin, waiting the minimum necessary t_{XUDPD} time, and then clocking in the first bit of the next Opcode command cycle. If the first bit of the next command is clocked in before the t_{XUDPD} time has elapsed, the device exits Ultra Deep Power Down, however the intended operation is ignored.

Figure 7-5. Exit Ultra-Deep Power-Down (Chip Select Low)



8. Buffer and Page Size Configuration

The memory array of DataFlash device is actually larger than other Serial Flash devices in that extra user-accessible bytes are provided in each page of the memory array. Some applications, however, may not want to take advantage of this extra memory and instead architect their software to operate on a “power of 2” binary, logical addressing scheme. To allow this, the DataFlash can be configured so that the buffer and page sizes are 256 bytes instead of the standard 264 bytes. In addition, the configuration of the buffer and page sizes is reversible and can be changed from 264 bytes to 256 bytes or from 256 bytes to 264 bytes. The configured setting is stored in an internal nonvolatile register so that the buffer and page size configuration is not affected by power cycles. The nonvolatile register has a limit of 10,000 erase/program cycles; therefore, care should be taken to not switch between the size options more than 10,000 times.

The AT45DB322F devide is initially shipped from Adesto with the buffer and page sizes set to 264 bytes. Devices can be ordered from Adesto pre-configured for the “power of 2” binary size of 256bytes. For details and ordering information, see Section 24.

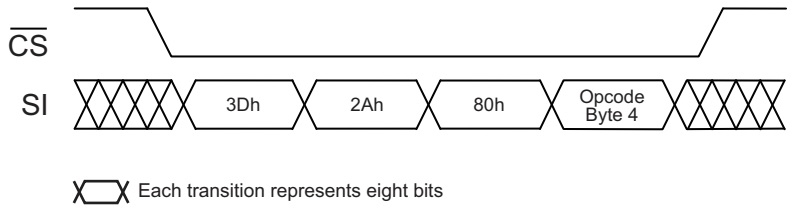
To configure the device for “power of 2” binary page size (256 bytes), a 4-byte opcode sequence of 3Dh, 2Ah, 80h, and A6h must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed configuration process and nonvolatile register program cycle. The programming of the nonvolatile register should take place in a time of t_{EP}, during which time the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy. The device does not need to be power cycled after the completion of the configuration process and register program cycle in order for the buffer and page size to be configured to 256 bytes.

To configure the device for standard DataFlash page size (264 bytes), a 4-byte opcode sequence of 3Dh, 2Ah, 80h, and A7h must be clocked into the device. After the last bit of the opcode sequence has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed configuration process and nonvolatile register program cycle. The programming of the nonvolatile register should take place in a time of t_{EP}, during which time the RDY/$\overline{BUSY}$ bit in the Status Register indicates that the device is busy. The device does not need to be power cycled after the completion of the configuration process and register program cycle in order for the buffer and page size to be configured to 256 bytes.

Table 8-1. Buffer and Page Size Configuration Commands

Command	Byte 1	Byte 2	Byte 3	Byte 4
“Power of 2” binary page size (256 bytes)	3Dh	2Ah	80h	A6h
DataFlash page size (264 bytes)	3Dh	2Ah	80h	A7h

Figure 8-1. Buffer and Page Size Configuration



9. Manufacturer and Device ID Read

Identification information can be read from the device to enable systems to electronically query and identify the device while it is in the system. The identification method and the command opcode comply with the JEDEC Standard for “Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices”. The type of information that can be read from the device includes the JEDEC-defined Manufacturer ID, the vendor-specific Device ID, and the vendor-specific Extended Device Information.

The Read Manufacturer and Device ID command is limited to a maximum clock frequency of f_{CLK}. Since not all Flash devices are capable of operating at very high clock frequencies, applications should be designed to read the identification information from the devices at a reasonably low clock frequency to ensure that all devices to be used in the application can be identified properly. Once the identification process is complete, the application can then increase the clock frequency to accommodate specific Flash devices that are capable of operating at the higher clock frequencies.

To read the identification information, the $\overline{CS}$ pin must first be asserted and then the opcode 9Fh must be clocked into the device. After the opcode has been clocked in, the device begins outputting the identification data on the SO pin during the subsequent clock cycles. The first byte to be output is the Manufacturer ID, followed by two bytes of the Device ID information. The fourth byte output is the Extended Device Information (EDI) String Length, which is 01h, indicating that one byte of EDI data follows. After the one byte of EDI data is output, the SO pin is placed into the high-impedance state. Therefore, additional clock cycles have no affect on the SO pin and no data is output. As indicated in the JEDEC Standard, reading the EDI String Length and any subsequent data is optional.

Deasserting the $\overline{CS}$ pin terminates the Manufacturer and Device ID Read operation and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

Table 9-1. Manufacturer and Device ID Information

Byte No.	Data Type	Value
1	Manufacturer ID	1Fh
2	Device ID (Byte 1)	27h
3	Device ID (Byte 2)	02h
4	Extended Device Information (EDI) String Length	01h
5	[Optional to Read] EDI Byte 1	00h

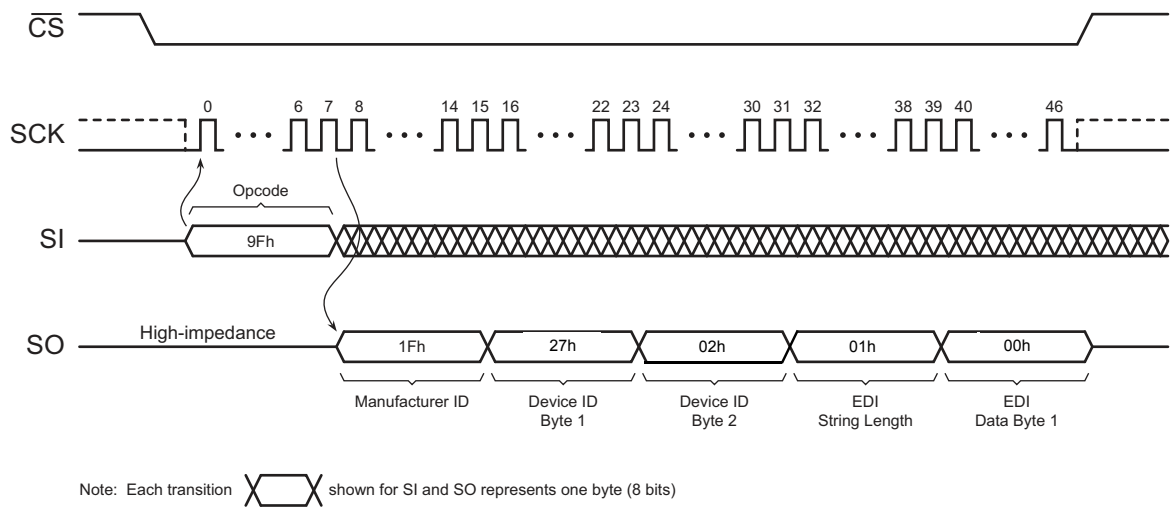
Table 9-2. Manufacturer and Device ID Details

Data Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Value	Details
Manufacturer ID	JEDEC Assigned Code								1Fh	JEDEC code: 0001 1111 (1Fh for Adesto)
	0	0	0	1	1	1	1	1		
Device ID (Byte 1)	Family Code			Density Code					27h	Family code: 001 (AT45Dxxx Family) Density code: 00111 (32-Mbit)
	0	0	1	0	0	1	1	1		
	Sub Code			Product Variant						
Device ID (Byte 2)	0	0	0	0	0	0	1	0	02h	Sub code: 000 (Standard Series) Product variant:00010

Table 9-3. AT45DB322F EDI Data

Byte Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Value	Details
5	RFU			Device Revision					00h	RFU: Reserved for Future Use Device revision:00000 (Initial Version)
	0	0	0	0	0	0	0	0		

Figure 9-1. Read Manufacturer and Device ID



Note: Each transition shown for SI and SO represents one byte (8 bits)

10. Software Reset

In some applications, it may be necessary to prematurely terminate a program or erase cycle early rather than wait the hundreds of microseconds or milliseconds necessary for the program or erase operation to complete normally. The Software Reset command allows a program or erase operation in progress to be ended abruptly and returns the device to an idle state.

To perform a Software Reset, the $\overline{CS}$ pin must be asserted and a 4-byte command sequence of F0h, 00h, 00h, and 00h must be clocked into the device. Any additional data clocked into the device after the last byte is ignored. When the $\overline{CS}$ pin is deasserted, the program or erase operation currently in progress is terminated within a time t_{SWRST}. Since the program or erase operation may not complete before the device is reset, the contents of the page being programmed or erased cannot be guaranteed to be valid.

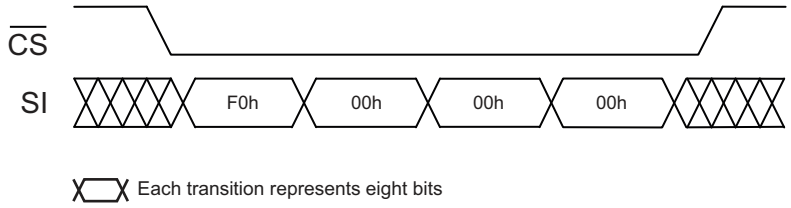
The Software Reset command has no effect on the states of the Sector Protection Register, the Sector Lockdown Register, or the buffer and page size configuration. The PS2, PS1, and ES bits of the Status Register, however, are reset back to their default states. If a Software Reset operation is performed while a sector is erase suspended, the suspend operation aborts and the contents of the page or block being erased in the suspended sector is left in an undefined state. If a Software Reset is performed while a sector is program suspended, the suspend operation aborts and the contents of the page that was being programmed and subsequently suspended is undefined. The remaining pages in the sector retain their previous contents.

The complete 4-byte opcode must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, no reset operation is performed.

Table 10-1. Software Reset

Command	Byte 1	Byte 2	Byte 3	Byte 4
Software Reset	F0h	00h	00h	00h

Figure 10-1. Software Reset



11. Operation Mode Summary

The commands described previously can be grouped into four different categories to better describe which commands can be executed at what times.

Group A commands consist of:

1. Main Memory Page Read
2. Continuous Array Read (SPI)
3. Read Sector Protection Register
4. Read Sector Lockdown Register
5. Read Security Register
6. Buffer 1 (or 2) Read

Group B commands consist of:

1. Page Erase
2. Block Erase
3. Sector Erase
4. Chip Erase
5. Main Memory Page to Buffer 1 (or 2) Transfer
6. Main Memory Page to Buffer 1 (or 2) Compare
7. Buffer 1 (or 2) to Main Memory Page Program with Built-In Erase
8. Buffer 1 (or 2) to Main Memory Page Program without Built-In Erase
9. Main Memory Page Program through Buffer 1 (or 2) with Built-In Erase
10. Main Memory Byte/Page Program through Buffer 1 without Built-In Erase
11. Auto Page Rewrite
12. Read-Modify-Write

Group C commands consist of:

1. Buffer 1 (or 2) Write
2. Status Register Read
3. Manufacturer and Device ID Read
4. Active Interrupt
5. Suspend/Resume
6. Software Reset

Group D commands consist of:

1. Erase Sector Protection Register
2. Program Sector Protection Register
3. Sector Lockdown
4. Program Security Register
5. Buffer and Page Size Configuration
6. Freeze Sector Lockdown

If a Group A command is in progress (not fully completed), then another command in Group A, B, C, or D should not be started. However, during the internally self-timed portion of Group B commands, any command in Group C can be executed. The Group B commands using Buffer 1 should use Group C commands using Buffer 2 and vice versa. Finally, during the internally self-timed portion of a Group D command, only the Status Register Read command should be executed.

Most of the commands in Group B can be suspended and resumed, except the Buffer Transfer, Buffer Compare, Auto Page Rewrite and Read-Modify-Write operations. If a Group B command is suspended, all of the Group A commands can be executed.

12. Command Tables

Table 12-1. Read Commands

Command	Opcode
Main Memory Page Read	D2h
Continuous Array Read (Low Power Mode)	01h
Continuous Array Read (Low Frequency)	03h
Continuous Array Read (High Frequency)	0Bh
Continuous Array Read (High Frequency)	1Bh
Continuous Array Read (Legacy Command – Not Recommended for New Designs)	E8h
Dual-output Read Array	3Bh
Quad-output Read Array	6Bh
Buffer 1 Read (Low Frequency)	D1h
Buffer 2 Read (Low Frequency)	D3h
Buffer 1 Read (High Frequency)	D4h
Buffer 2 Read (High Frequency)	D6h

Table 12-2. Program and Erase Commands

Command	Opcode
Buffer 1 Write	84h
Buffer 2 Write	87h
Dual-input Buffer 1 Write	24h
Dual-input Buffer 2 Write	27h
Quad-input Buffer 1 Write	44h
Quad-input Buffer 2 Write	47h
Buffer 1 to Main Memory Page Program with Built-In Erase	83h
Buffer 2 to Main Memory Page Program with Built-In Erase	86h
Buffer 1 to Main Memory Page Program without Built-In Erase	88h
Buffer 2 to Main Memory Page Program without Built-In Erase	89h
Main Memory Page Program through Buffer 1 with Built-In Erase	82h
Main Memory Page Program through Buffer 2 with Built-In Erase	85h
Main Memory Byte/Page Program through Buffer 1 without Built-In Erase	02h
Page Erase	81h
Block Erase	50h
Sector Erase	7Ch
Chip Erase	C7h + 94h + 80h + 9Ah
Program/Erase Suspend	B0h

Table 12-2. Program and Erase Commands

Command	Opcode
Program/Erase Resume	D0h
Read-Modify-Write through Buffer 1	58h
Read-Modify-Write through Buffer 2	59h

Table 12-3. Protection and Security Commands

Command	Opcode
Enable Sector Protection	3Dh + 2Ah + 7Fh + A9h
Disable Sector Protection	3Dh + 2Ah + 7Fh + 9Ah
Erase Sector Protection Register	3Dh + 2Ah + 7Fh + CFh
Program Sector Protection Register	3Dh + 2Ah + 7Fh + FCh
Read Sector Protection Register	32h
Sector Lockdown	3Dh + 2Ah + 7Fh + 30h
Read Sector Lockdown Register	35h
Freeze Sector Lockdown	34h + 55h + AAh + 40h
Program Security Register	9Bh + 00h + 00h + 00h
Read Security Register	77h

Table 12-4. Additional Commands

Command	Opcode
Main Memory Page to Buffer 1 Transfer	53h
Main Memory Page to Buffer 2 Transfer	55h
Main Memory Page to Buffer 1 Compare	60h
Main Memory Page to Buffer 2 Compare	61h
Auto Page Rewrite or Read-Modify-Write through Buffer 1	58h
Auto Page Rewrite or Read-Modify-Write through Buffer 2	59h
Deep Power-Down	B9h
Active Interrupt	25h
Resume from Deep Power-Down	ABh
Ultra-Deep Power-Down	79h
Status Register Read	D7h
Manufacturer and Device ID Read	9Fh
Read Configuration Register	3Fh
Quad Enable	3Dh + 2Ah + 81h + 66h
Quad Disable	3Dh + 2Ah + 81h + 67h
Configure “Power of 2” (Binary) Page Size	3Dh + 2Ah + 80h + A6h
Configure Standard DataFlash Page Size	3Dh + 2Ah + 80h + A7h
Software Reset	F0h + 00h + 00h + 00h

Table 12-5. Legacy Commands [1][2]

Command	Opcode
Buffer 1 Read	54H
Buffer 2 Read	56H
Main Memory Page Read	52H
Continuous Array Read	68H
Status Register Read	57H

Notes: 1. Legacy commands are not recommended for new designs.
2. Legacy commands operate from 2.30V to 3.60V Vcc only.

Table 12-6. Detailed Bit-level Addressing Sequence for AT45DB322F Binary Page Size (256 bytes)

Page Size = 256 bytes									Address Byte								Address Byte								Address Byte								Additional Dummy Bytes
Opcode	Opcode								Reserved	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
01h	0	0	0	0	0	0	0	1	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
02h	0	0	0	0	0	0	1	0	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
03h	0	0	0	0	0	0	1	1	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
0Bh	0	0	0	0	1	0	1	1	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	1
1Bh	0	0	0	1	1	0	1	1	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	2
25h	0	0	1	0	0	1	0	1	N/A								N/A								N/A								N/A
32h	0	0	1	1	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
35h	0	0	1	1	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
50h	0	1	0	1	0	0	0	0	X	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	X	X	X	N/A
53h	0	1	0	1	0	0	1	1	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
55h	0	1	0	1	0	1	0	1	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
58h[1]	0	1	0	1	1	0	0	0	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
59h[1]	0	1	0	1	1	0	0	1	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
58h[2]	0	1	0	1	1	0	0	0	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
59h[2]	0	1	0	1	1	0	0	1	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
60h	0	1	1	0	0	0	0	0	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
61h	0	1	1	0	0	0	0	1	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
77h	0	1	1	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
79h	0	1	1	1	1	0	0	1	N/A								N/A								N/A								N/A
7Ch	0	1	1	1	1	1	0	0	X	A	A	A	A	A	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
81h	1	0	0	0	0	0	0	1	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
82h	1	0	0	0	0	0	1	0	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
83h	1	0	0	0	0	0	1	1	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
84h	1	0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	N/A
85h	1	0	0	0	0	1	0	1	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	N/A
86h	1	0	0	0	0	1	1	0	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
87h	1	0	0	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	N/A
88h	1	0	0	0	1	0	0	0	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
89h	1	0	0	0	1	0	0	1	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	X	X	X	X	X	X	X	X	N/A
9Fh	1	0	0	1	1	1	1	1	N/A								N/A								N/A								N/A
B9h	1	0	1	1	1	0	0	1	N/A								N/A								N/A								N/A

Table 12-6. Detailed Bit-level Addressing Sequence for AT45DB322F Binary Page Size (256 bytes) *(continued)*

Page Size = 256 bytes									Address Byte								Address Byte								Address Byte								Additional Dummy Bytes
Opcode	Opcode								Reserved	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
ABh	1	0	1	0	1	0	1	1	N/A								N/A								N/A								N/A
B0h	1	0	1	1	0	0	0	0	N/A								N/A								N/A								N/A
D0h	1	1	0	1	0	0	0	0	N/A								N/A								N/A								N/A
D1h	1	1	0	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	N/A
D2h	1	1	0	1	0	0	1	0	X	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	4
D3h	1	1	0	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	N/A
D4h	1	1	0	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	1
D6h	1	1	0	1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A	A	A	A	A	A	A	A	1
D7h	1	1	0	1	0	1	1	1	N/A								N/A								N/A								N/A

Note: 1. Shown to indicate when the Auto Page Rewrite operation is executed.
2. Shown to indicate when the Read-Modify-Write operation is executed.
3. X = Dummy Bit

Table 12-7. Detailed Bit-level Addressing Sequence for AT45DB322F Standard DataFlash Page Size (264 bytes)

Page Size = 264 bytes									Address Byte								Address Byte								Address Byte								Additional Dummy Bytes
Opcode	Opcode								PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	
01h	0	0	0	0	0	0	0	1	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	N/A
02h	0	0	0	0	0	0	1	0	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	N/A
03h	0	0	0	0	0	0	1	1	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	N/A
0Bh	0	0	0	0	1	0	1	1	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	1
1Bh	0	0	0	1	1	0	1	1	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	2
25h	0	0	1	0	0	1	0	1	N/A								N/A								N/A								N/A
32h	0	0	1	1	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
35h	0	0	1	1	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
50h	0	1	0	1	0	0	0	0	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	X	X	N/A
53h	0	1	0	1	0	0	1	1	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
55h	0	1	0	1	0	1	0	1	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
58h[1]	0	1	0	1	1	0	0	0	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
59h[1]	0	1	0	1	1	0	0	1	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
58h[2]	0	1	0	1	1	0	0	0	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	N/A
59h[2]	0	1	0	1	1	0	0	1	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	N/A
60h	0	1	1	0	0	0	0	0	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
61h	0	1	1	0	0	0	0	1	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
77h	0	1	1	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
79h	0	1	1	1	1	0	0	1	N/A								N/A								N/A								N/A
7Ch	0	1	1	1	1	1	0	0	P	P	P	P	P	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N/A
81h	1	0	0	0	0	0	0	1	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
82h	1	0	0	0	0	0	1	0	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	N/A
83h	1	0	0	0	0	0	1	1	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
84h	1	0	0	0	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	B	N/A
85h	1	0	0	0	0	1	0	1	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	N/A
86h	1	0	0	0	0	1	1	0	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
87h	1	0	0	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	B	N/A

Table 12-7. Detailed Bit-level Addressing Sequence for AT45DB322F Standard DataFlash Page Size (264 bytes) *(continued)*

Page Size = 264 bytes									Address Byte								Address Byte								Address Byte								Additional Dummy Bytes
Opcode	Opcode								PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	
88h	1	0	0	0	1	0	0	0	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
89h	1	0	0	0	1	0	0	1	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	X	X	X	X	X	X	X	X	X	N/A
9Fh	1	0	0	1	1	1	1	1	N/A								N/A								N/A								N/A
B9h	1	0	1	1	1	0	0	1	N/A								N/A								N/A								N/A
ABh	1	0	1	0	1	0	1	1	N/A								N/A								N/A								N/A
B0h	1	0	1	1	0	0	0	0	N/A								N/A								N/A								N/A
D0h	1	1	0	1	0	0	0	0	N/A								N/A								N/A								N/A
D1h	1	1	0	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	B	N/A
D2h	1	1	0	1	0	0	1	0	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	4
D3h	1	1	0	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	B	N/A
D4h	1	1	0	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	B	1
D6h	1	1	0	1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B	B	B	B	B	B	B	B	B	1
D7h	1	1	0	1	0	1	1	1	N/A								N/A								N/A								N/A

Notes: 1. Shown to indicate when the Auto Page Rewrite operation is executed.

2. Shown to indicate when the Read-Modify-Write operation is executed.

3. P = Page Address Bit, B = Byte/Buffer Address Bit, X = Dummy Bit

13. Power-On/Reset State

When power is first applied to the device, or when recovering from a reset condition, the output pin (SO) is in a high impedance state, and a high-to-low transition on the $\overline{CS}$ pin is required to start a valid instruction. The SPI mode (Mode 3 or Mode 0) is automatically selected on every falling edge of $\overline{CS}$ by sampling the inactive clock state.

13.1 Power-Up / Power-Down Voltage and Timing Requirements

During power-up, the device must not be READ for at least the minimum t_{VCSL} time after the supply voltage reaches the minimum V_{POR} level (V_{POR} min). While the device is being powered-up, the internal Power-On Reset (POR) circuitry keeps the device in a reset mode until the supply voltage rises above the minimum V_{cc}. During this time, all operations are disabled and the device does not respond to any commands.

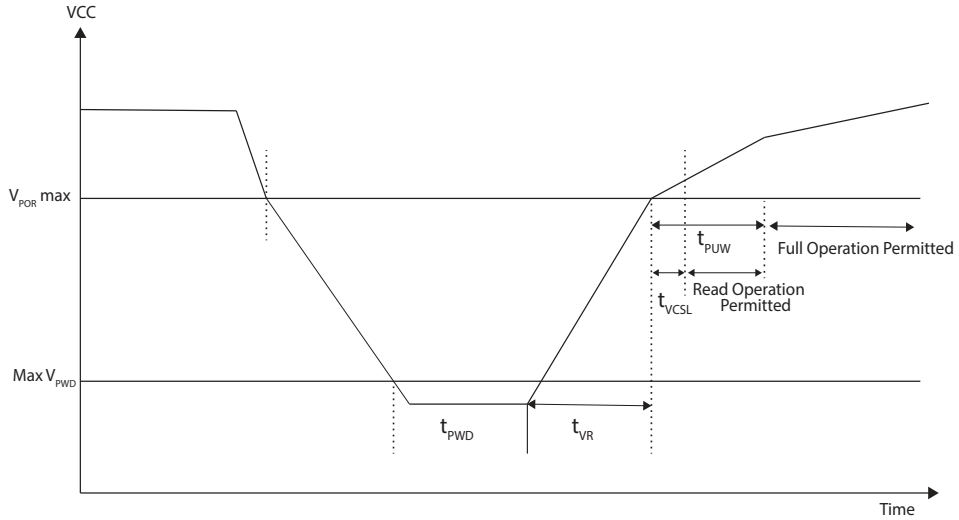
If the first operation to the device after power-up is a program or erase operation, then the operation cannot be started until the supply voltage reaches the minimum V_{CC} level and an internal device delay has elapsed. This delay is a maximum time of t_{PUW}. After the t_{PUW} time, the device is in the standby mode if $\overline{CS}$ is at logic high or active mode if $\overline{CS}$ is at logic low. For the case of Power-down then Power-up operation, or if a power interruption occurs (such that VCC drops below V_{POR} max), the V_{cc} of the Flash device must be maintained below V_{PWD} for at least the minimum specified T_{PWD} time. This is to ensure the Flash device resets properly after a power interruption.

Table 13-1. Voltage and Timing Requirements for Power-Up/Power-Down

Symbol	Parameter	Min	Max	Units
V_{PWD} (1)	V_{CC} for device initialization		1.0	V
t_{PWD} (1)	Minimum duration for device initialization	300		µs
t_{VCSL}	Minimum V_{CC} to chip select low time for Read command	70		µs
t_{VR} (1)	V_{CC} rise time	1	500000	µs/V
V_{POR}	Power on reset voltage	1.45	1.6	V
t_{PUW}	Power up delay time before Program or Erase is allowed		3	ms

1. Not 100% tested (value guaranteed by design and characterization).

Figure 13-1. Power-Up Timing



14. System Considerations

The serial interface is controlled by the Serial Clock (SCK), Serial Input (SI), and Chip Select ($\overline{CS}$) pins. These signals must rise and fall monotonically and be free from noise. Excessive noise or ringing on these pins can be misinterpreted as multiple edges and cause improper operation of the device. PCB traces must be kept to a minimum distance or appropriately terminated to ensure proper operation. If necessary, decoupling capacitors can be added on these pins to provide filtering against noise glitches.

As system complexity continues to increase, voltage regulation is becoming more important. A key element of any voltage regulation scheme is its current sourcing capability. Like all Flash memories, the peak current for DataFlash devices occurs during the programming and erasing operations. The supply voltage regulator needs to be able to supply this peak current requirement. An under specified regulator can cause current starvation. Besides increasing system noise, current starvation during programming or erasing can lead to improper operation and possible data corruption.

15. Electrical Specifications

15.1 Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (except V_{CC} but including NC pins) with Respect to Ground	-0.6V to V_{CC} + 0.6V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. The “Absolute Maximum Ratings” are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Voltage extremes referenced in the “Absolute Maximum Ratings” are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time.

15.2 DC and AC Operating Range

Name	Environment	Value
Operating Temperature (Case)	Industrial	-40°C to 85°C
V_{CC} Power Supply		1.65V to 3.6V

15.3 DC Characteristics

Symbol	Parameter	Condition	1.65 V to 3.6 V			2.3 V to 3.6 V			Unit
			Min	Typ	Max	Min	Typ	Max	
I_{UDPD}	Ultra-Deep Power-Down Current	$\overline{CS}$ = VCC. All other inputs at 0V or Vcc		0.2	0.5		0.2	0.5	µA
I_{DPD}	Deep Power-Down Current	$\overline{CS}$ = VCC. All other inputs at 0V or Vcc		9	15		9	15	µA
I_{SB}	Standby Current	$\overline{CS}$ = VCC. All other inputs at 0V or Vcc		20	35		20	35	µA
I_{CC1}	Active Current, Low Power Read (01h) Operation	f = 1 MHz, I_{OUT} = 0 mA		2	3		2	3	mA
		f = 20 MHz, I_{OUT} = 0 mA		2.5	3.5		2.5	3.5	mA
I_{CC2} (1)	Active Current, Read Operation	f = 50 MHz, I_{OUT} = 0 mA		5	6		5	6	mA
		f = 85 MHz, I_{OUT} = 0 mA		7	9		7.5	9	mA
I_{CC3}	Active Current, Program Operation	$\overline{CS}$ = Vcc		8	10		8	10	mA
I_{CC4}	Active Current, Erase Operation	$\overline{CS}$ = Vcc		5	7		5	7	mA
I_{LI}	Input Load Current	All inputs at CMOS levels			1			1	µA
I_{LO}	Output Leakage Current	All inputs at CMOS levels			1			1	µA
V_{IL}	Input Low Voltage				VCC x 0.3			VCC x 0.3	V
V_{IH}	Input Low Voltage		VCC x 0.7		VCC + 0.6	VCC x 0.7		VCC + 0.6	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA			0.4			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	VCC - 0.2V			VCC - 0.2			V

Notes: 1. Typical values measured at 3.0V at 25 °C.

15.4 AC Characteristics

Symbol	Parameter	1.65 V to 3.6 V			2.3 V to 3.6 V			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK}	SCK Frequency			85			104	MHz
f_{CAR1}	SCK Frequency for Continuous Read (opcode 0x0B)			70			85	MHz
f_{CAR2}	SCK Frequency for Continuous Read (Low Frequency opcode 0x03)			40			50	MHz
f_{CAR3}	SCK Frequency for Continuous Read (Low Power Mode opcode 0x01)			20			20	MHz
f_{CAR4}	SCK Frequency for Continuous Read (Fast Frequency opcode 0x1B)			85			104	MHz
f_{CAR5}	SCK Frequency for Dual I/O (opcode 0x3B)			85			85	MHz
f_{CAR6}	SCK Frequency for Quad I/O (opcode 0x6B)			70			70	MHz
t_{WH}	SCK High Time	4.5			4.5			ns
t_{WL}	SCK Low Time	4.5			4.5			ns
t_{SCKR}(1)	SCK Rise Time, Peak-to-peak	0.1			0.1			V/ns
t_{SCKF}(1)	SCK Fall Time, Peak-to-peak	0.1			0.1			V/ns
t_{CS}	Minimum $\overline{CS}$ High Time	25			25			ns
t_{CSS}	$\overline{CS}$ Low Setup Time	6			6			ns
t_{CSH}	$\overline{CS}$ Low Hold Time	5			5			ns
t_{SU}	Data In Setup Time	2			2			ns
t_{H}	Data In Hold Time	1			1			ns
t_{HO}	Output Hold Time	0			0			ns
t_{DIS}	Output Disable Time			8			6	ns
t_{V}	Output Valid Time			7			6	ns
t_{WPE}	$\overline{WP}$ Low to Protection Enabled			1			1	µs
t_{WPD}	$\overline{WP}$ High to Protection Disabled			1			1	µs
t_{LOCK}	Freeze Sector Lockdown Time (from $\overline{CS}$ High)			200			200	µs
t_{EUDPD}(1)	$\overline{CS}$ High to Ultra-Deep Power-Down			3			3	µs
t_{CSLU}(1)	Minimum $\overline{CS}$ Low Time to Exit Ultra-Deep Power Down	10			10			µs
t_{XUDPD}(1)	Exit Ultra-Deep Power Down Time			70			70	µs
t_{EDPD}(1)	$\overline{CS}$ High to Deep Power Down			3			3	µs
t_{RDPD}	Resume from Deep Power Down			10			10	µs
t_{XFR}	Page to Buffer Transfer Time			100			100	µs
t_{COMP}	Page to Buffer Compare Time			100			100	µs
t_{RST}	$\overline{RESET}$ Pulse Width	10			10			µs
t_{REC}	$\overline{RESET}$ Recovery Time		1			1		µs
t_{SWRST}	Software Reset Time		35			35		µs

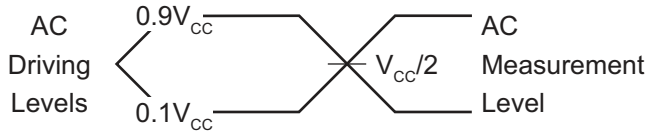
Note: 1. Values are based on device characterization, not 100% tested in production.

15.5 Program and Erase Characteristics

Symbol	Parameter	Condition	1.65 V to 3.6 V			2.3 V to 3.6 V			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{EP}	Page Erase and Programming Time (256/264 page size)	<= 20K cycles		19	150		19	150	ms
		<= 100K cycles		19	360		19	360	ms
t_{PP}	Page Programming Time (256/264 page size)	<= 20K cycles		3.5	4.5		3.5	4.5	ms
		<= 100K cycles		3.5	5		3.5	5	ms
t_{BP}	Byte Programming Time (256/264 page size)	<= 20K cycles		12			12		µs
		<= 100K cycles		12			12		µs
t_{PE}	Page Erase Time (256/264 page size)	<= 20K cycles		15	100		15	100	ms
		<= 100K cycles		15	400		15	400	ms
t_{BLKE}	Block Erase Time (2KB, 256/264 page size)	<= 20K cycles		60	200		60	200	ms
		<= 100K cycles		60	400		60	400	ms
t_{SE}	Sector Erase Time (256KB, 256/264 page size)	<= 20K cycles		7.6	8		7.6	8	s
		<= 100K cycles		7.6	16		7.6	16	s
t_{CE}	Chip Erase Time (256 KB Sectors / 2 KB Blocks)	<= 20K cycles		110	125		110	125	s
		<= 100K cycles		110	250		110	250	s
t_{SUSP}	Program Suspend Time			6	10		6	10	µs
	Erase Suspend Time			10	15		10	15	µs
t_{RES}	Program Resume Time			1	3		1	3	µs
	Erase Resume Time			1	3		1	3	µs
t_{OTPP}	OTP Security Register Program Time			100	300		100	300	µs

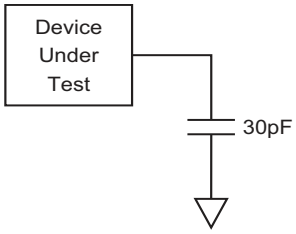
Notes: 1. Values are based on device characterization, not 100% tested in production.

16. Input Test Waveforms and Measurement Levels



t_R, t_F < 2ns (10% to 90%)

17. Output Test Load

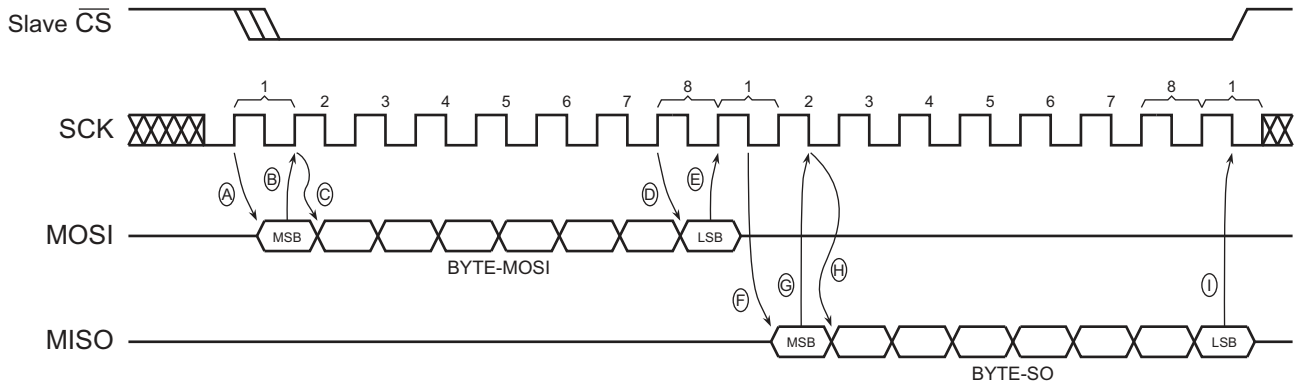


18. Utilizing the RapidS Function

To take advantage of the RapidS function's ability to operate at higher clock frequencies, a full clock cycle must be used to transmit data back and forth across the serial bus. The DataFlash is designed to always clock its data out on the falling edge of the SCK signal and clock data in on the rising edge of SCK.

For full clock cycle operation to be achieved, when the DataFlash is clocking data out on the falling edge of SCK, the host controller should wait until the next falling edge of SCK to latch the data in. Similarly, the host controller should clock its data out on the rising edge of SCK in order to give the DataFlash a full clock cycle to latch the incoming data in on the next rising edge of SCK.

Figure 18-1. RapidS Mode



MOSI = Master Out, Slave In
MISO = Master In, Slave Out
The Master is the host controller and the Slave is the DataFlash.

The Master always clocks data out on the rising edge of SCK and always clocks data in on the falling edge of SCK.
The Slave always clocks data out on the falling edge of SCK and always clocks data in on the rising edge of SCK.

A. Master clocks out first bit of BYTE-MOSI on the rising edge of SCK
B. Slave clocks in first bit of BYTE-MOSI on the next rising edge of SCK
C. Master clocks out second bit of BYTE-MOSI on the same rising edge of SCK
D. Last bit of BYTE-MOSI is clocked out from the Master
E. Last bit of BYTE-MOSI is clocked into the slave
F. Slave clocks out first bit of BYTE-SO
G. Master clocks in first bit of BYTE-SO
H. Slave clocks out second bit of BYTE-SO
I. Master clocks in last bit of BYTE-SO

Figure 18-2. Command Sequence for Read/Write Operations for Page Size 256 Bytes

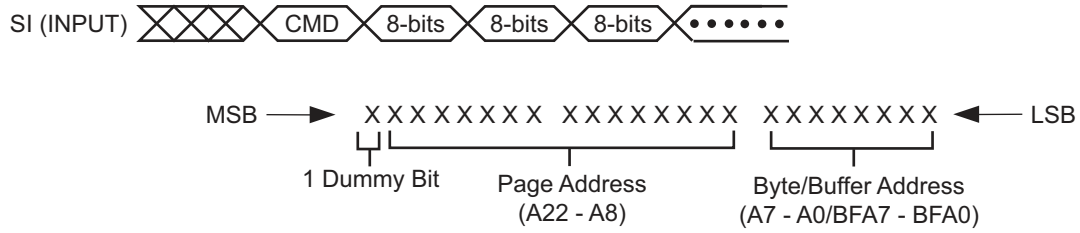
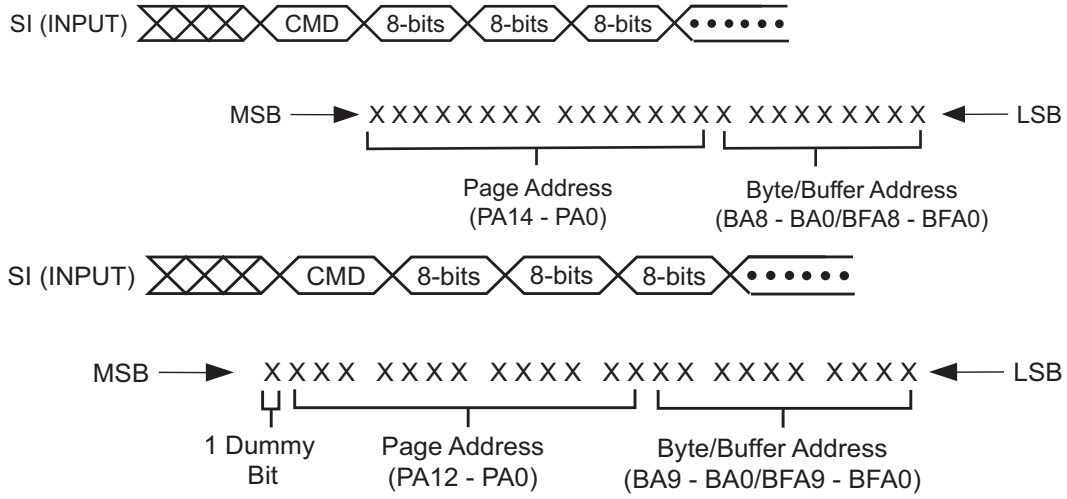


Figure 18-3. Command Sequence for Read/Write Operations for Page Size 264 bytes



19. AC Waveforms

Four different timing waveforms are shown in Figure 19-1 through Figure 19-4. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. In both cases, output SO becomes valid while the SCK signal is still low (SCK low time is specified as t_{WL}). Timing Waveforms 1 and 2 conform to RapidS serial interface but for frequencies up to 104 MHz. Waveforms 1 and 2 are compatible with SPI Mode 0 and SPI Mode 3, respectively.

Waveform 3 and 4 illustrate general timing diagram for RapidS serial interface. These are similar to Waveform 1 and 2, except that output SO is not restricted to become valid during the t_{WL} period. These timing waveforms are valid over the full frequency range (maximum frequency = 104 MHz) of the RapidS serial case.

Figure 19-1. Waveform 1 = SPI Mode 0 Compatible

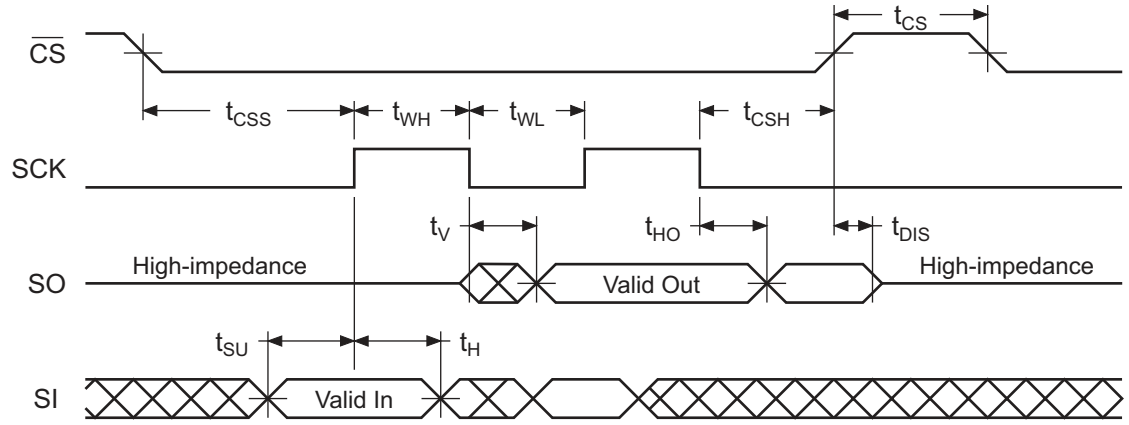


Figure 19-2. Waveform 2 = SPI Mode 3 Compatible

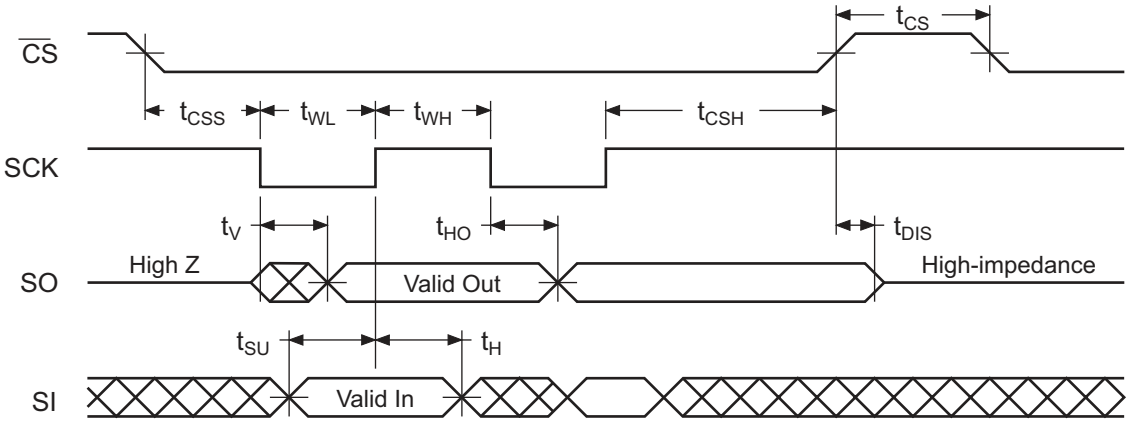


Figure 19-3. Waveform 3 = RapidS Mode 0

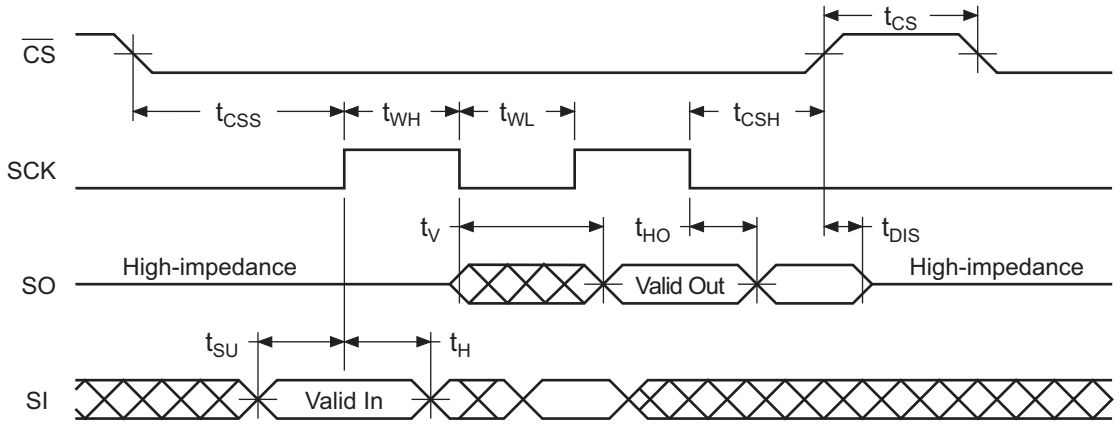
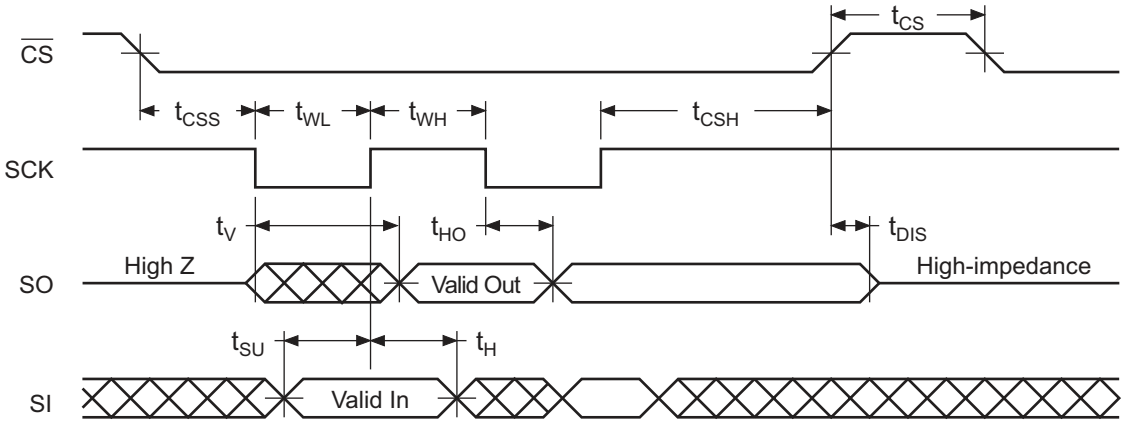


Figure 19-4. Waveform 4 = RapidS Mode 3



20. Write Operations

The following waveforms illustrate the various write sequences available.

Figure 20-1. Buffer Write

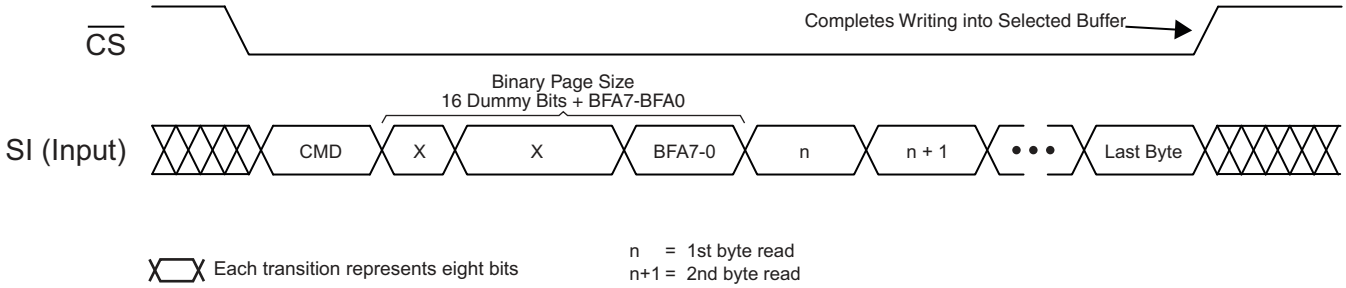
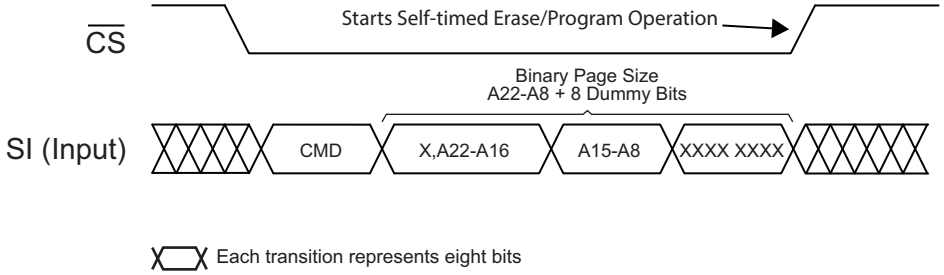


Figure 20-2. Buffer to Main Memory Page Program



21. Read Operations

The following waveforms illustrate the various read sequences available.

Figure 21-1. Main Memory Page Read

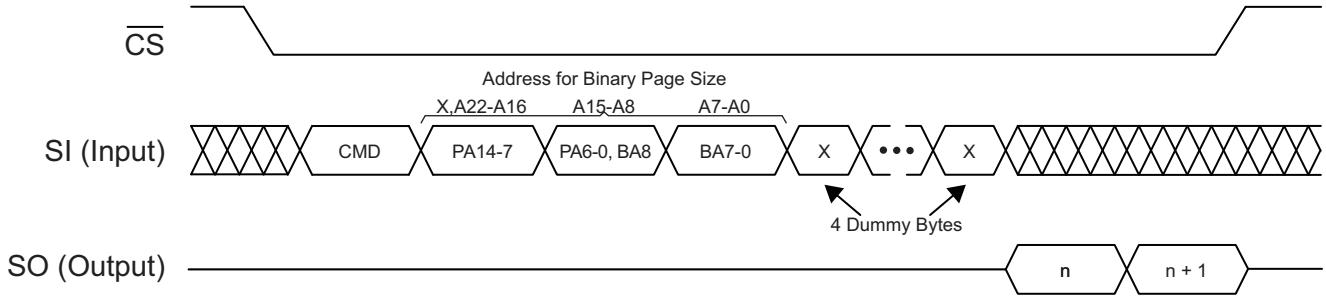
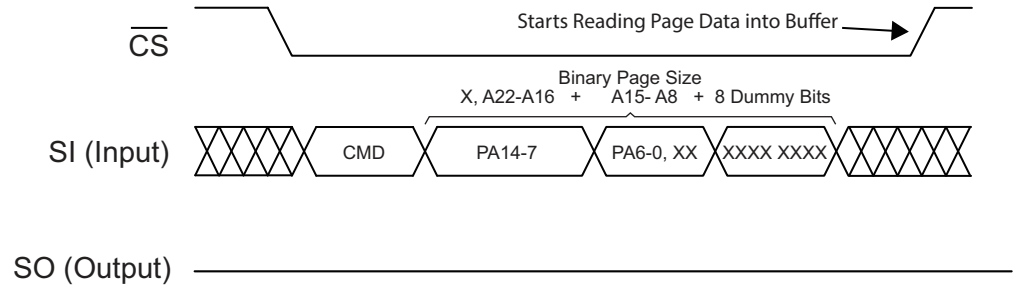
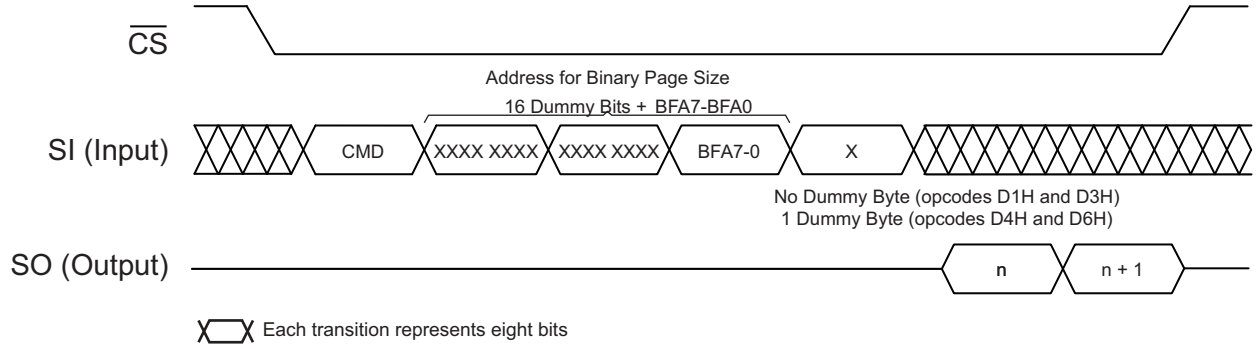


Figure 21-2. Main Memory Page to Buffer Transfer



Data from the selected Flash page is read into either SRAM Buffer.

Figure 21-3. Buffer Read



22. Detailed Bit-level Read Waveforms: RapidS Mode 0/Mode 3

Figure 22-1. Continuous Array Read (Legacy Opcode E8h)

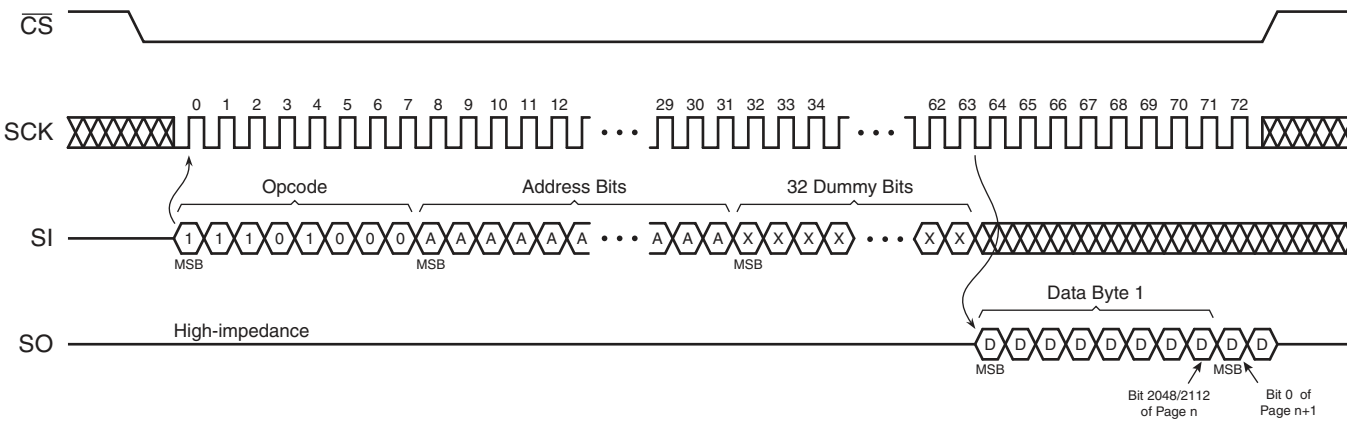


Figure 22-2. Continuous Array Read (Opcode 0Bh)

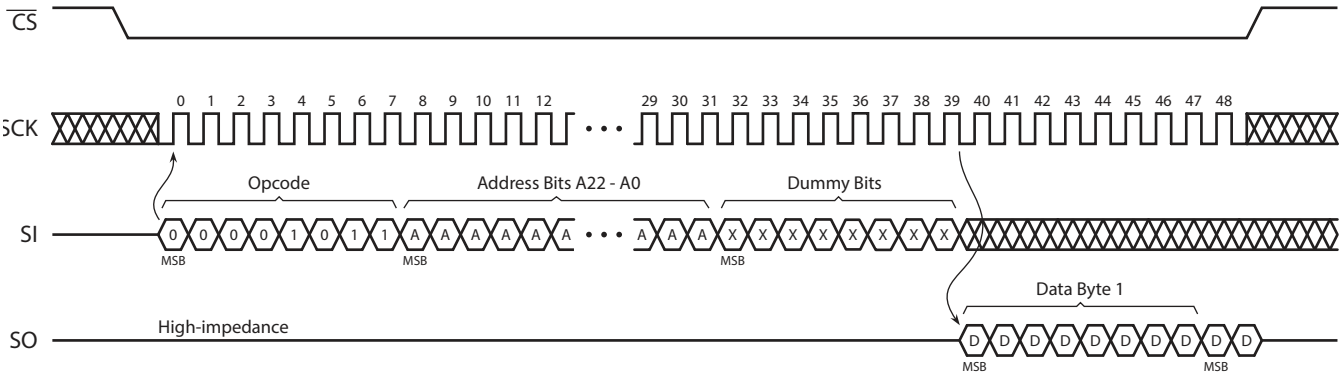


Figure 22-3. Continuous Array Read (Opcode 01h or 03h)

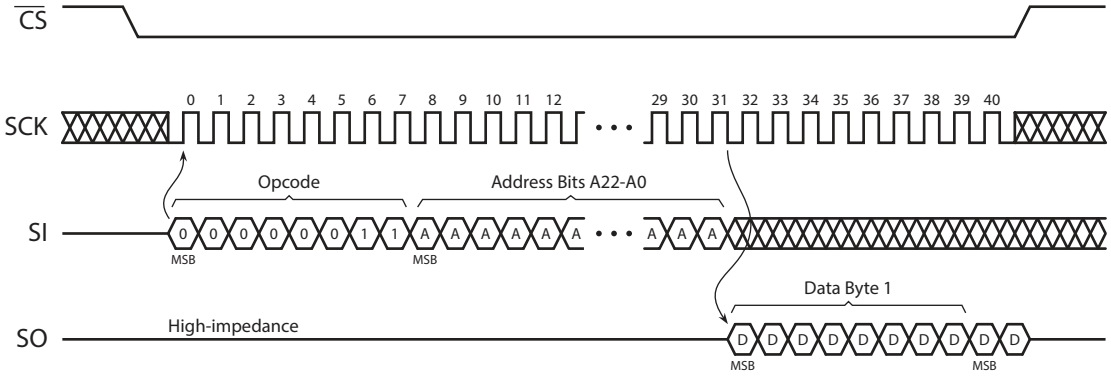


Figure 22-4. Main Memory Page Read (Opcode D2h)

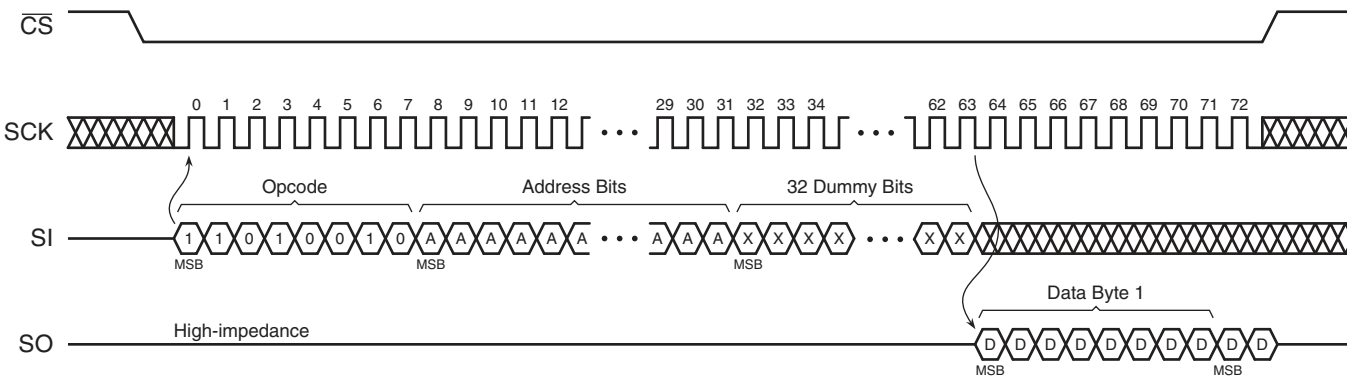


Figure 22-5. Buffer Read (Opcode D4h or D6h)

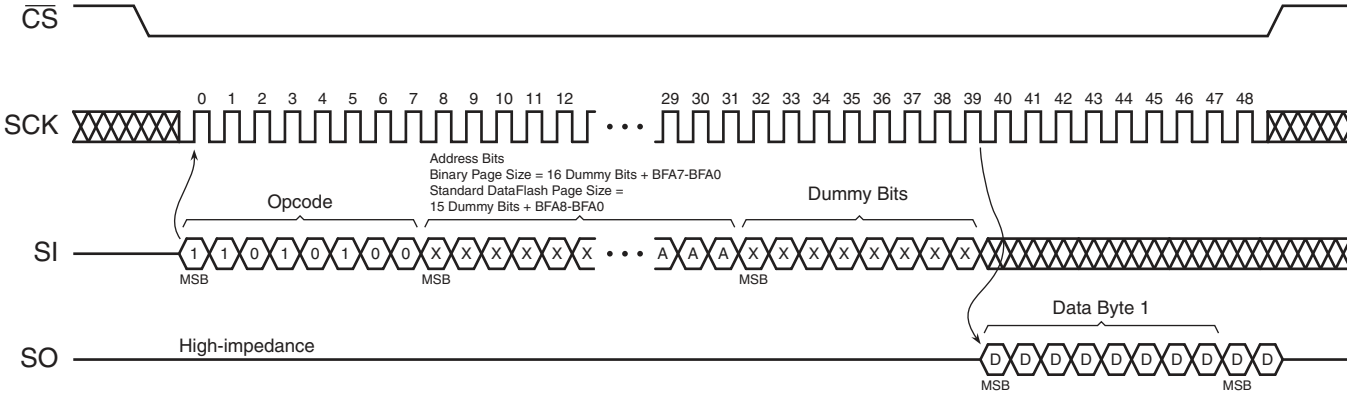


Figure 22-6. Buffer Read – Low Frequency (Opcode D1h or D3h)

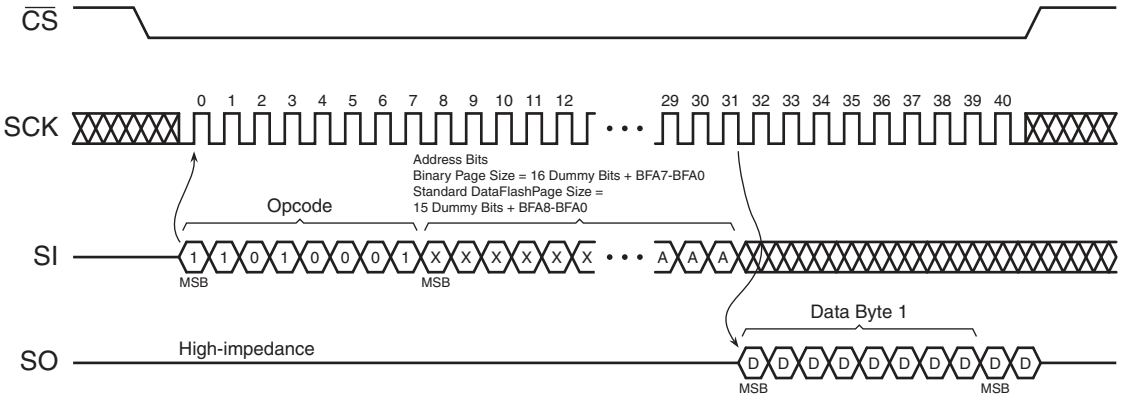


Figure 22-7. Read Sector Protection Register (Opcode 32h)

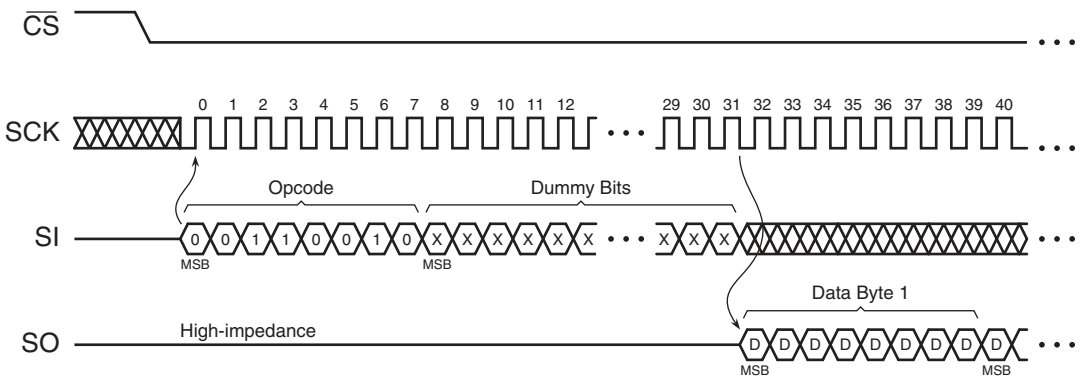


Figure 22-8. Read Sector Lockdown Register (Opcode 35h)

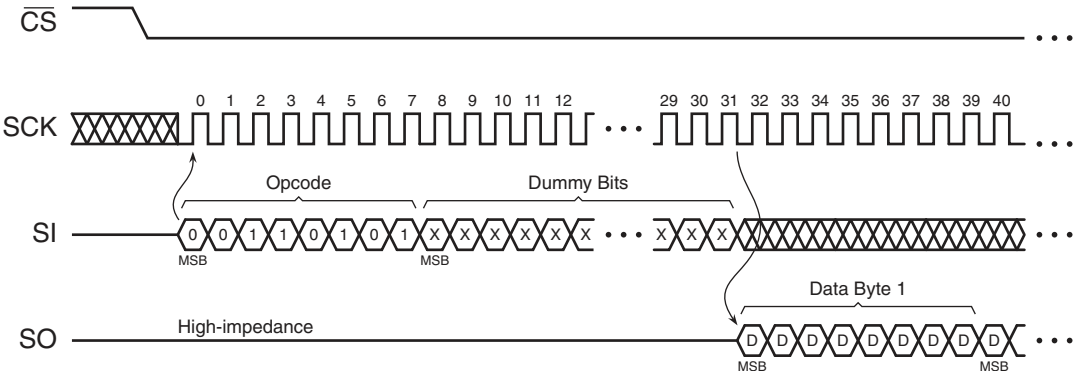


Figure 22-9. Read Security Register (Opcode 77h)

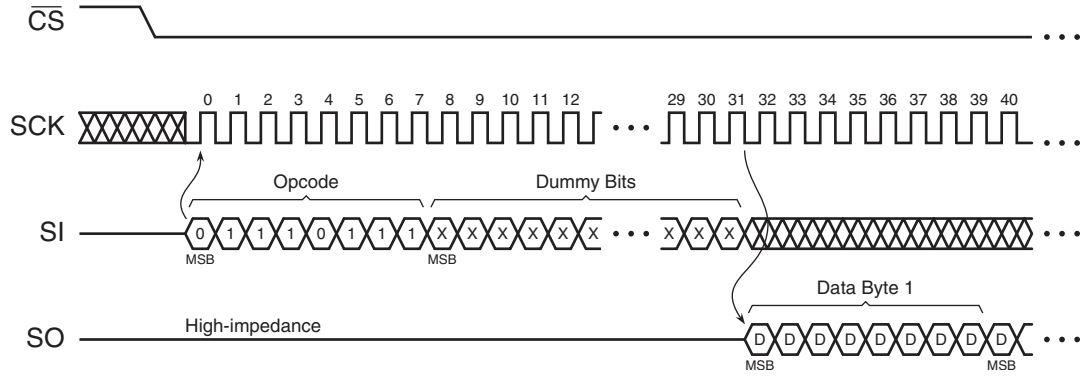


Figure 22-10. Status Register Read (Opcode D7h)

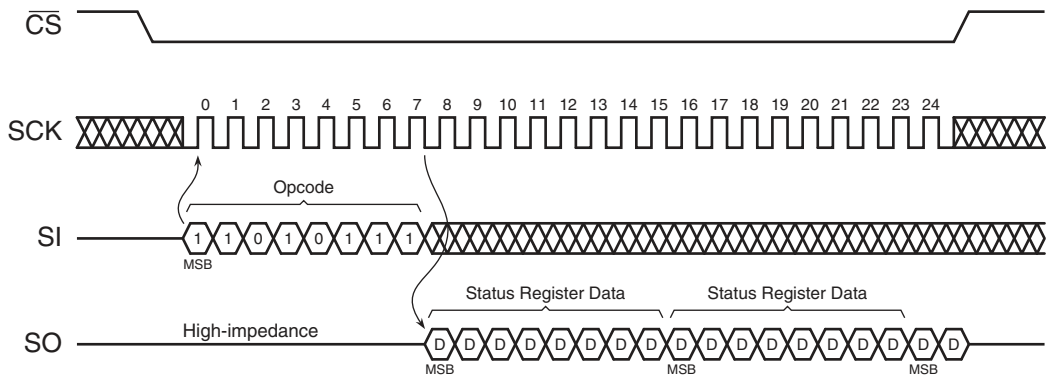
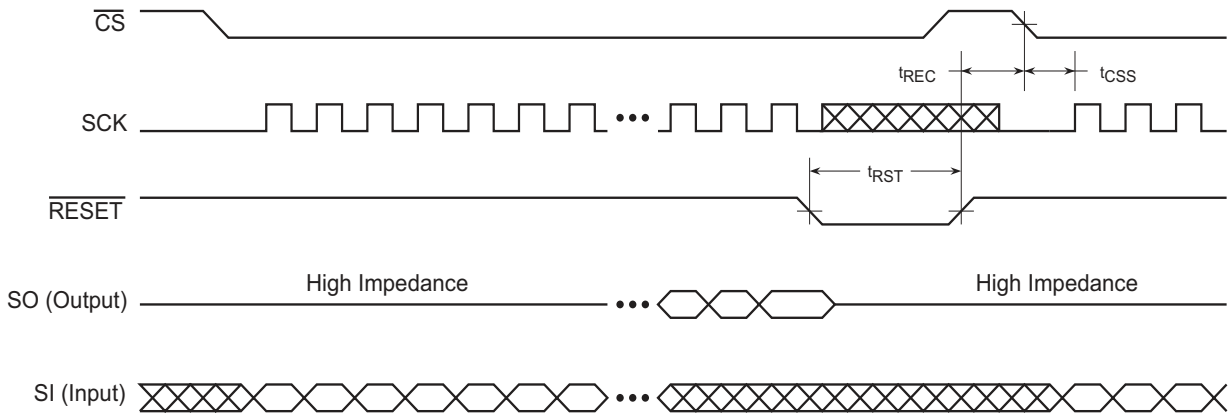


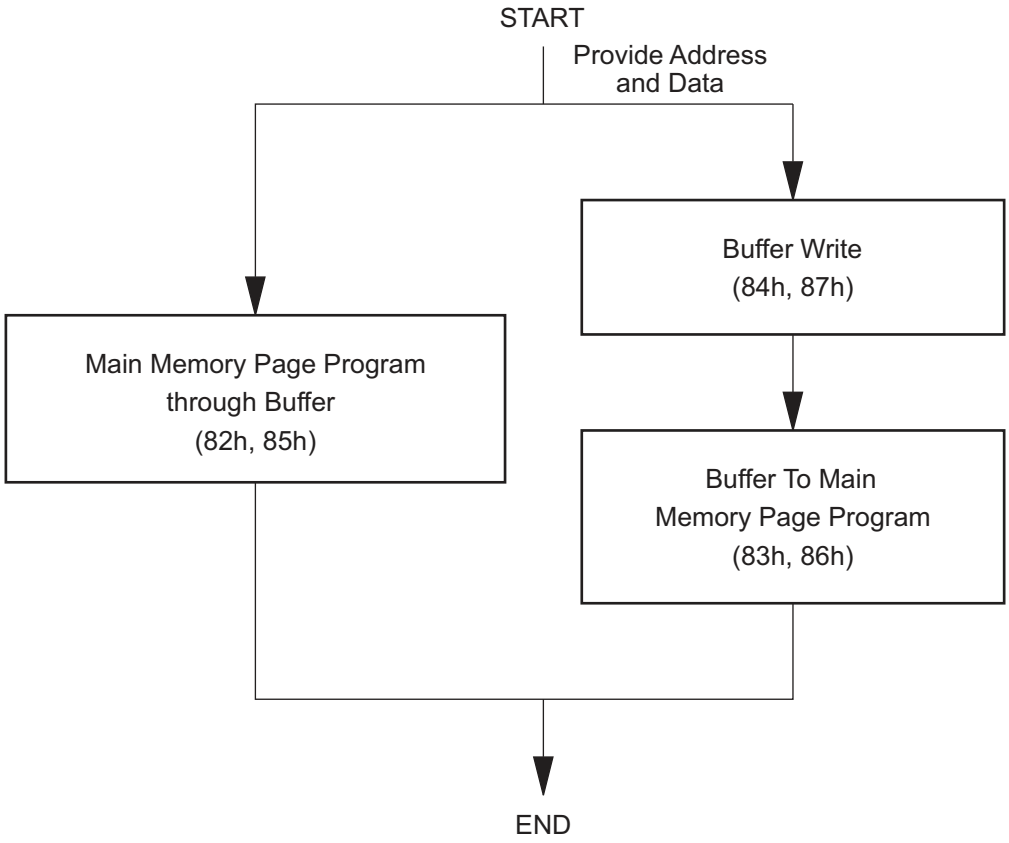
Figure 22-11. Reset Timing



Note: 1. The $\overline{CS}$ signal should be in the high state before the $\overline{RESET}$ signal is deasserted.

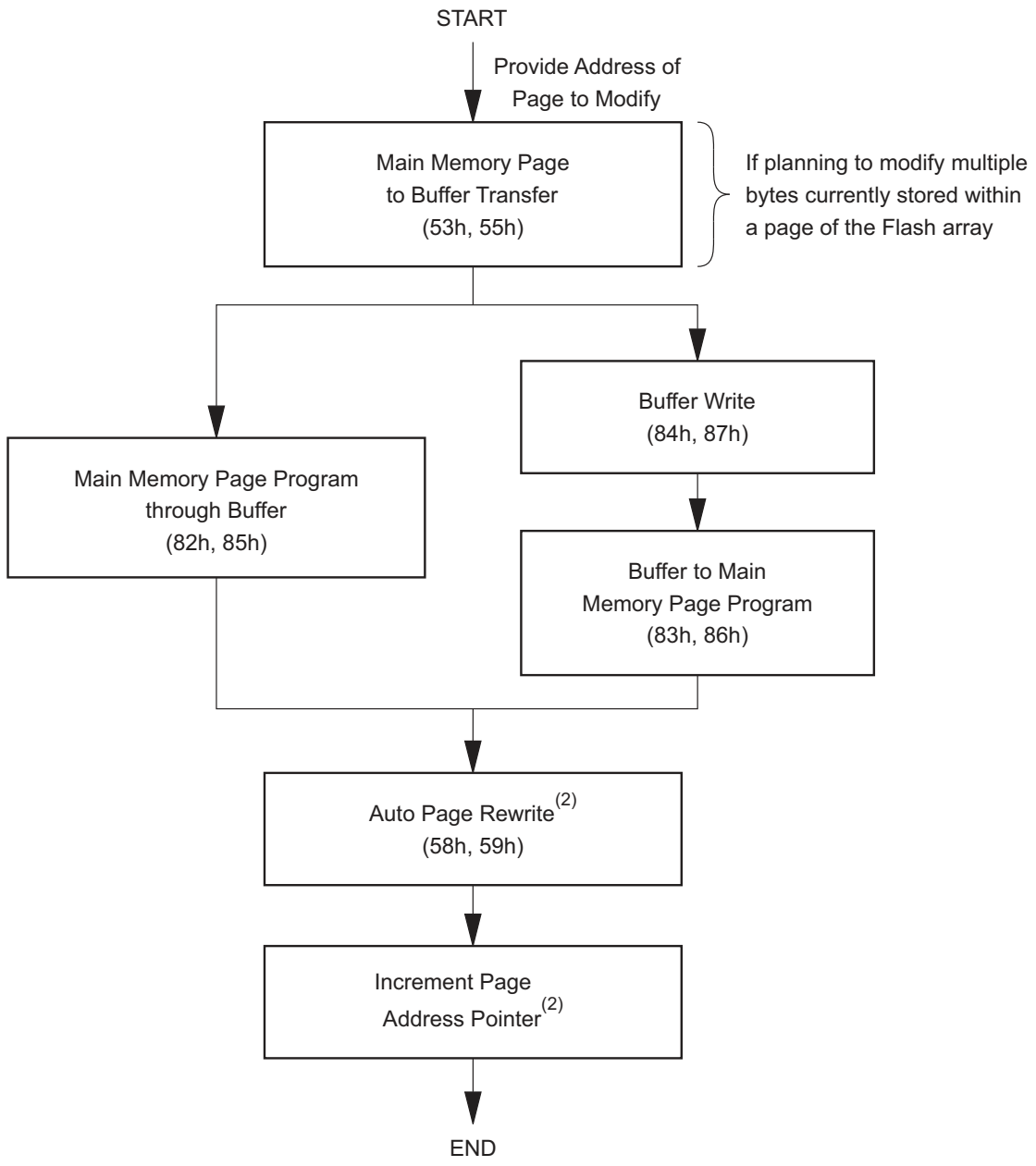
23. Auto Page Rewrite Flowchart

Figure 23-1. Algorithm for Programming or Re-programming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a buffer write operation followed by a buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm is repeated sequentially for each page within the entire array.

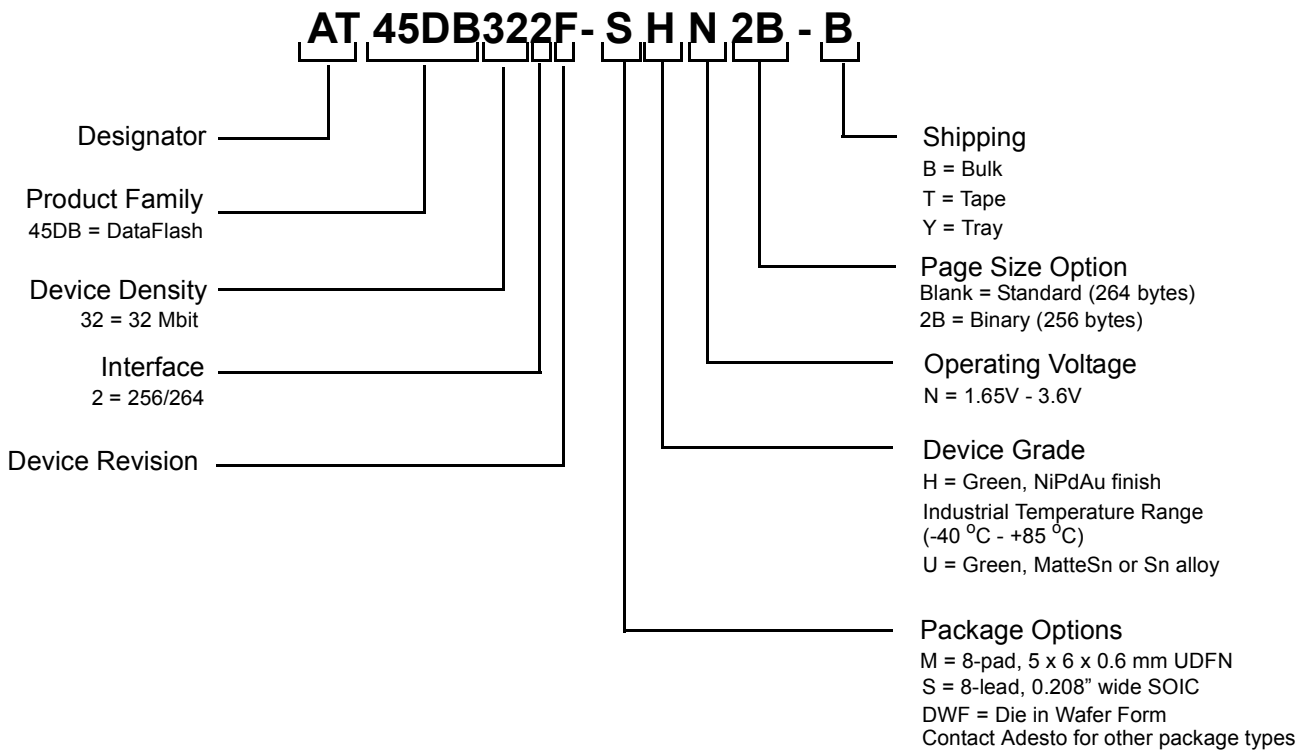
Figure 23-2. Algorithm for Programming or Re-programming of the Entire Array Randomly



Notes:
1. To preserve data integrity, each page of an DataFlash sector must be updated/rewritten at least once within every 50,000 cumulative page erase and program operations.
2. A page address pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the page address pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low-power applications may choose to wait until 50,000 cumulative page erase and program operations have accumulated before rewriting all pages of the sector.

24. Ordering Information

24.1 Ordering Detail



Package Type [1]	
8S2	8-lead 0.208" wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8MA1	8-pad (5 x 6 x 0.6mm body), Thermally Enhanced Plastic Ultra Thin Dual Flat No-lead (UDFN)
DWF	Die-wafer scale fully tested known good die

1. Contact Adesto for other package types.

24.2 Ordering Codes (Standard DataFlash Page Size)

Ordering Code	Package	Lead Finish	Operating Voltage	f_{SCK}	Device Grade
AT45DB322F-SHN-B[1]	8S2	NiPdAu	1.65V to 3.6V	104 MHz	Industrial (-40°C to 85°C)
AT45DB322F-SHN-T[1]					
AT45DB322F-MHN-Y[1]	8MA1				
AT45DB322F-MHN-T[1]					
AT45DB322F-DWF	Wafer (KGD)	n/a			

Notes: 1. The shipping carrier suffix is not marked on the device.

24.3 Ordering Codes (Binary Page Size)

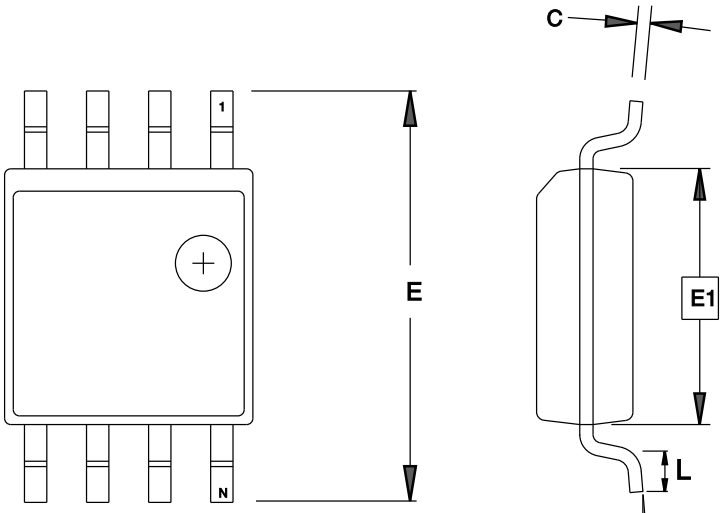
Ordering Code	Package	Lead Finish	Operating Voltage	f_{SCK}	Device Grade
AT45DB322F-SHN2B-T[1][2]	8S2	NiPdAu	1.65V to 3.6V	85MHz	Industrial (-40°C to 85°C)
AT45DB322F-MHN2B-T [1][2]	8MA1				

Notes: 1. The shipping carrier suffix is not marked on the device.

2. Parts ordered with suffix code ‘2B’ are shipped in tape and reel (T&R) with the page size set to 256 bytes. This option is only available for shipping in T&R (-T).

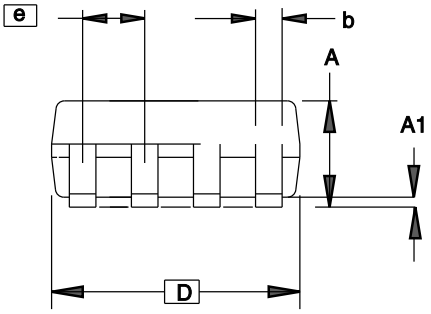
25. Packaging Information

25.1 8S2 – 8-lead EIAJ SOIC



TOP VIEW

END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

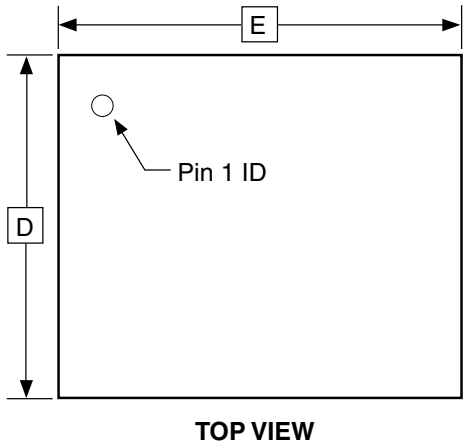
SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	4
C	0.15		0.35	4
D	5.13		5.35	
E1	5.18		5.40	2
E	7.70		8.10	
L	0.51		0.85	
q	0°		8°	
e	1.27 BSC			3

Notes: 1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs aren't included.
3. Determines the true geometric position.
4. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

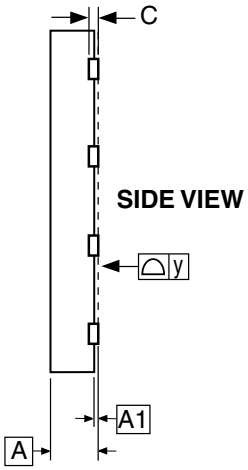
4/15/08

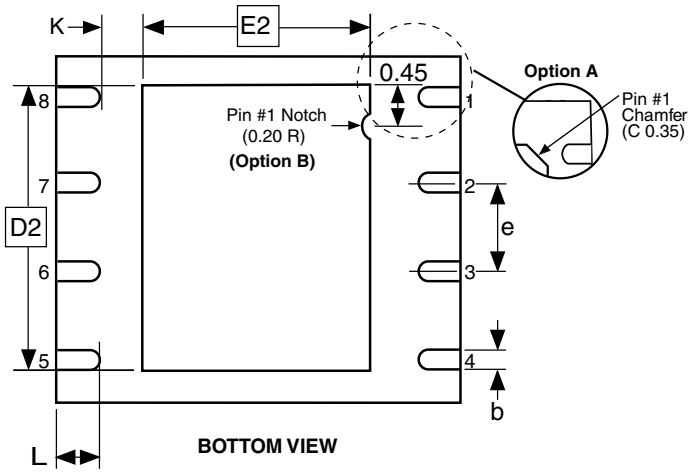
adesto TECHNOLOGIES **Package Drawing Contact:** contact@adestotech.com	**TITLE** **8S2,** 8-lead, 0.208" Body, Plastic Small Outline Package (EIAJ)	**GPC** STN	**DRAWING NO.** 8S2	**REV.** F

25.2 8MA1 – 8-pad UDFN



TOP VIEW





BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.45	0.55	0.60	
A1	0.00	0.02	0.05	
b	0.35	0.40	0.48	
C		0.152 REF		
D	4.90	5.00	5.10	
D2	3.80	4.00	4.20	
E	5.90	6.00	6.10	
E2	3.20	3.40	3.60	
e		1.27		
L	0.50	0.60	0.75	
y	0.00	–	0.08	
K	0.20	–	–	

Notes: 1. This package conforms to JEDEC reference MO-229, Saw Singulation.
2. The terminal #1 ID is a Laser-marked Feature.

4/15/08

	TITLE	GPC	DRAWING NO.	REV.
adesto TECHNOLOGIES **Package Drawing Contact:** contact@adestotech.com	**8MA1,** 8-pad (5 x 6 x 0.6 mm Body), Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	YFG	8MA1	D

26. Revision History

Revision	Date	Change Description
A	09/2018	Initial release of AT45DB322F Preliminary Data Sheet.
B	03/2019	Added clarification of WP pin usage to Section 1. Added clarification of the ‘2B’ suffix to product offerings in Table 2-1. Updated formatting in Section 15.5, Program and Erase Characteristics. Updated description of $\overline{WP}$ pin in Table 1.1, Pin Descriptions.

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