

# MC74VHCT259A

## Product Preview

### 8-Bit Addressable Latch/1-of-8 Decoder CMOS Logic Level Shifter with LSTTL-Compatible Inputs

The MC74VHC259 is an 8-bit Addressable Latch fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

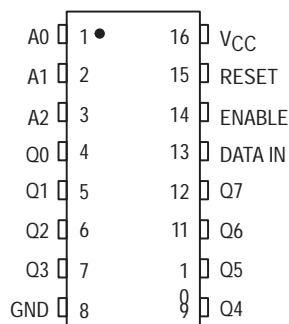
The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The VHC259 is designed for general purpose storage applications in digital systems. The device has four modes of operation as shown in the mode selection table. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one-of-eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode, all outputs are LOW and unaffected by the address and data inputs. When operating the VHC259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The MC74VHC259 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC259 to be used to interface 5 V circuits to 3 V circuits.

- High Speed:  $t_{PD} = 7.6 \text{ ns (Typ)}$  at  $V_{CC} = 5 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 2 \mu\text{A (Max)}$  at  $T_A = 25^\circ\text{C}$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- CMOS-Compatible Outputs:  $V_{OH} > 0.8 V_{CC}$ ;  $V_{OL} < 0.1 V_{CC} @\text{Load}$
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:  $\text{HBM} > 2000 \text{ V}$

#### PIN ASSIGNMENT

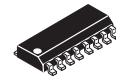


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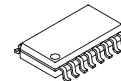
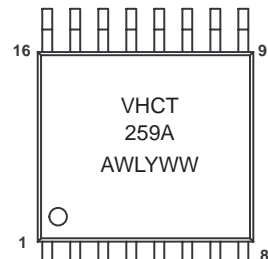
#### MARKING DIAGRAMS



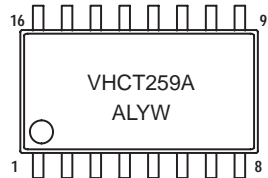
**SOIC-16**  
**D SUFFIX**  
**CASE 751B**



**TSSOP-16**  
**DT SUFFIX**  
**CASE 948F**



**SOIC EIAJ-16**  
**M SUFFIX**  
**CASE 966**



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

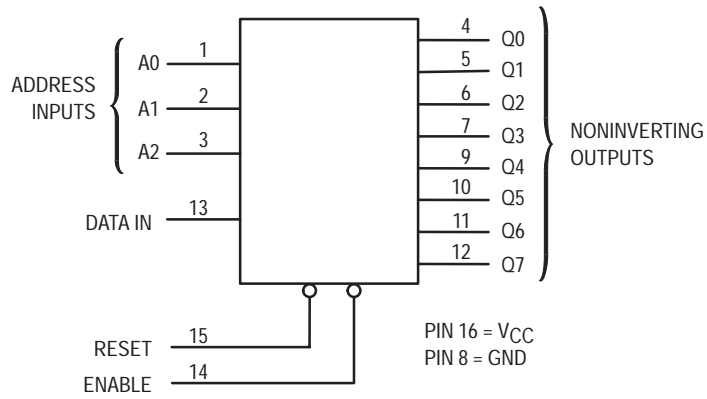
A = Assembly Location A = Assembly Location  
WL = Wafer Lot L = Wafer Lot  
Y = Year Y = Year  
WW = Work Week W = Work Week

#### ORDERING INFORMATION

Device	Package	Shipping
MC74VHCT259AD	SOIC-16	48 Units/Rail
MC74VHCT259ADR2	SOIC-16	2500 Units/Reel
MC74VHCT259ADT	TSSOP-16	96 Units/Rail
MC74VHCT259ADTEL	TSSOP-16	2000 Units/Reel
MC74VHCT259ADTR2	TSSOP-16	2500 Units/Reel
MC74VHCT259AM	SOIC EIAJ-16	50 Units/Rail
MC74VHCT259AMEL	SOIC EIAJ-16	2000 Units/Reel

# MC74VHCT259A

## LOGIC DIAGRAM



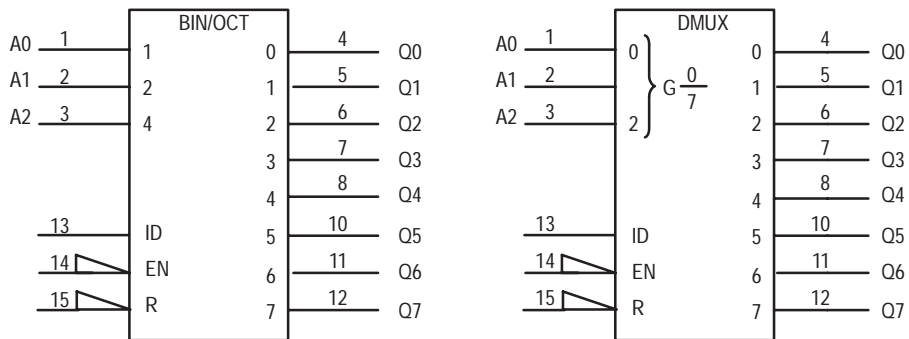
## MODE SELECTION TABLE

Enable	Reset	Mode
L	H	Addressable Latch
H	H	Memory
L	L	8-Line Demultiplexer
H	L	Reset

## LATCH SELECTION TABLE

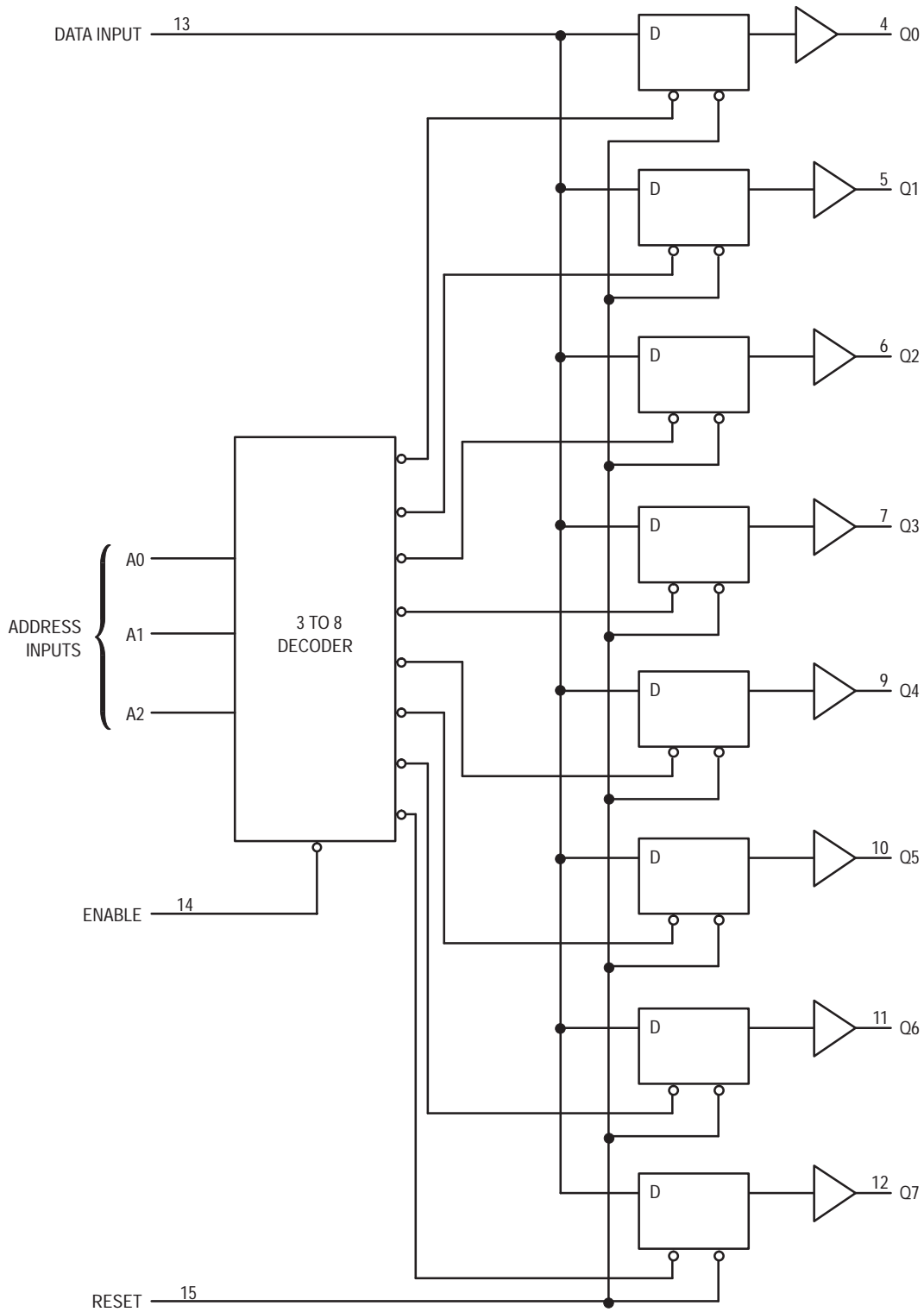
Address Inputs			Latch Addressed
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

## IEC LOGIC SYMBOL



# MC74VHCT259A

## EXPANDED LOGIC DIAGRAM



# MC74VHCT259A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage	- 0.5 to + 7.0	V
V <sub>out</sub>	DC Output Voltage	- 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input Diode Current	- 20	mA
I <sub>OK</sub>	Output Diode Current	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 75	mA
P <sub>D</sub>	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

† Derating — SOIC Packages: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	3.0	5.5	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage V <sub>CC</sub> = 0 High or Low State	0 0	5.5 V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time V <sub>CC</sub> = 5.0V ± 0.5V	0	20	ns/V

The  $\theta_{JA}$  of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

## DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

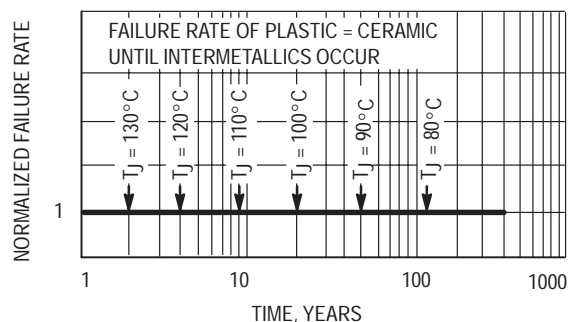


Figure 1. Failure Rate vs. Time Junction Temperature

# MC74VHCT259A

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> = ≤ 85°C		T <sub>A</sub> = ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		3.0 4.5 5.5	1.2 2.0 2.0			1.2 2.0 2.0		1.2 2.0 2.0		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -50 μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -4 mA I <sub>OH</sub> = -8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V <sub>OL</sub>	Maximum Low-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50 μA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0		± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			2.0		40.0		40.0	μA
I <sub>CC</sub> T	Quiescent Supply Current	Input: V <sub>IN</sub> = 3.4 V	5.5			1.35		1.50		1.65	mA
I <sub>OPD</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5 V	0.0			0.5		5.0		10	mA

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns)

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = ≤ 85°C		T <sub>A</sub> = ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Data to Output Fig. 2. and 7.	V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF			11.0 16.0	1.0 1.0	13.0 18.0	1.0 1.0	13.0 18.0	ns
		V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF			8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Address Select to Output Fig. 3. and 7.	V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF			11.0 16.0	1.0 1.0	13.0 18.0	1.0 1.0	13.0 18.0	ns
		V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF			8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Enable to Output Fig. 4. and 7.	V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF			11.0 16.0	1.0 1.0	13.0 18.0	1.0 1.0	13.0 18.0	ns
		V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF			8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Output Fig. 5. and 7.	V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF			11.0 16.0	1.0 1.0	13.0 18.0	1.0 1.0	13.0 18.0	ns
		V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF			8.0 10.0	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
C <sub>IN</sub>	Maximum Input Capacitance			6	10		10		10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Note 1.)	Typical @ 25°C, V <sub>CC</sub> = 5.0V	
		30	
			pF

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1.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$ .  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

## TIMING REQUIREMENTS (Input $t_r = t_f = 3.0ns$ )

Symbol	Parameter	Test Conditions	$T_A = 25^\circ C$			$T_A = \leq 85^\circ C$		$T_A = \leq 125^\circ C$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$t_w$	Minimum Pulse Width, Reset or Enable Fig. 6.	$V_{CC} = 3.3 \pm 0.3V$	5.0			5.5		5.5		ns
		$V_{CC} = 5.0 \pm 0.5V$	5.0			5.5		5.5		
$t_{su}$	Minimum Setup Time, Address or Data to Enable Fig. 6.	$V_{CC} = 3.3 \pm 0.3V$	4.5			4.5		4.5		ns
		$V_{CC} = 5.0 \pm 0.5V$	3.0			3.0		3.0		
$t_h$	Minimum Hold Time, Enable to Address or Data Fig. 4. or 5.	$V_{CC} = 3.3 \pm 0.3V$	2.0			2.0		2.0		ns
		$V_{CC} = 5.0 \pm 0.5V$	2.0			2.0		2.0		
$t_r, t_f$	Maximum Input, Rise and Fall Times Fig. 2.	$V_{CC} = 3.3 \pm 0.3V$			400		300		300	ns
		$V_{CC} = 5.0 \pm 0.5V$			200		100		100	

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## SWITCHING WAVEFORMS

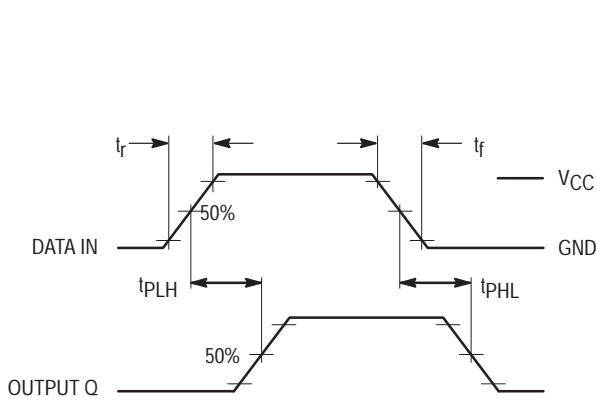


Figure 2.

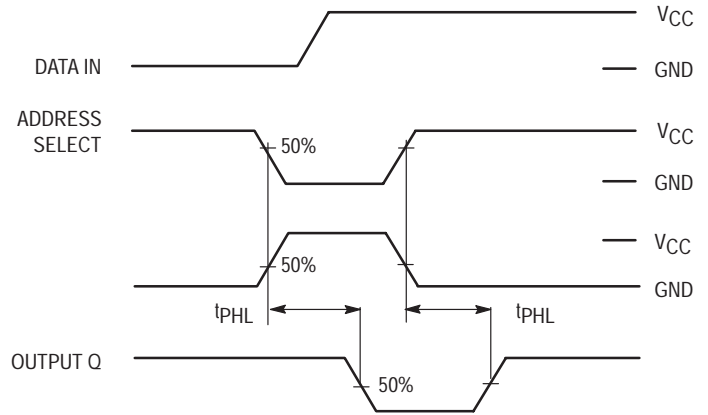


Figure 3.

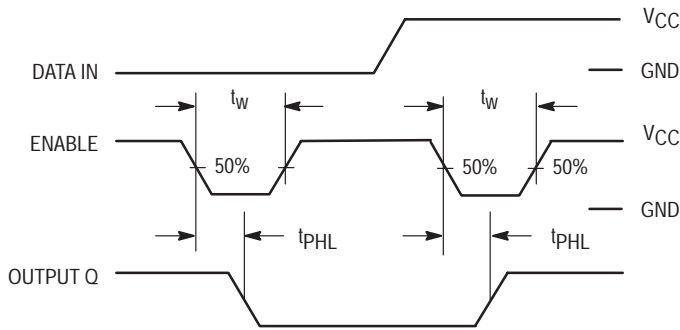


Figure 4.

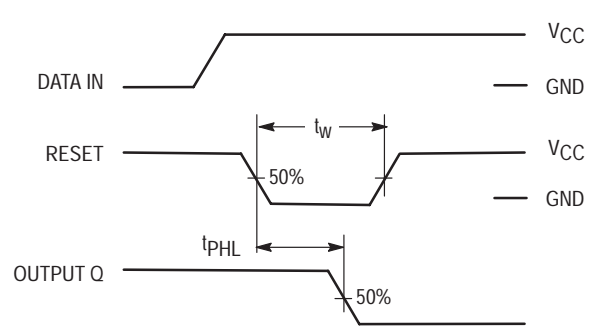


Figure 5.

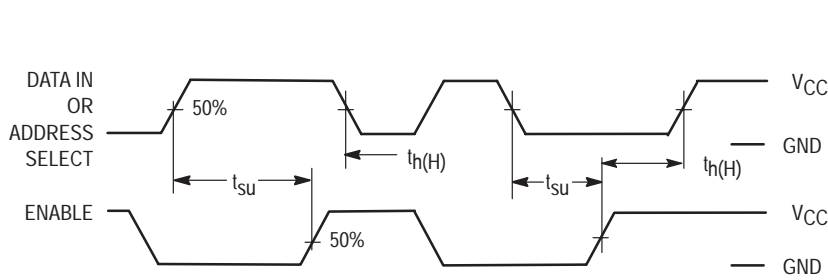
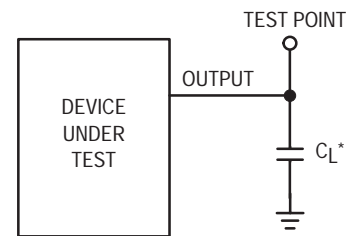


Figure 6.



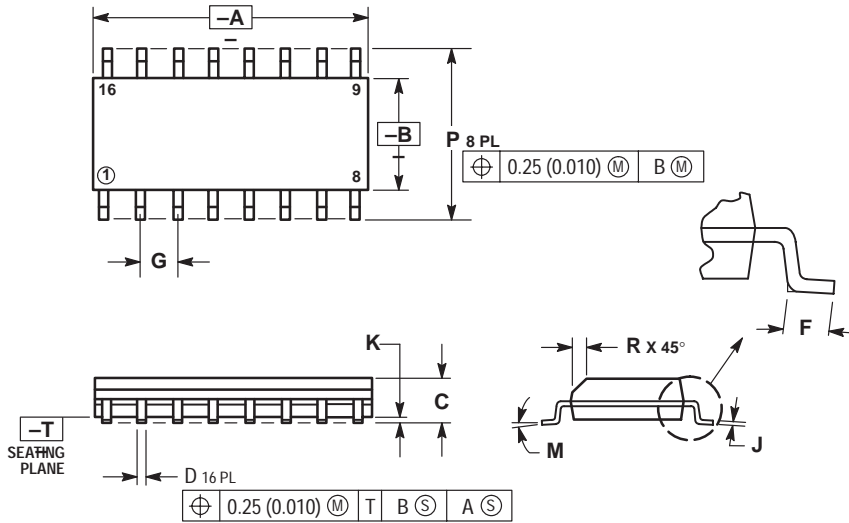
\*Includes all probe and jig capacitance

Figure 7. Test Circuit

# MC74VHCT259A

## PACKAGE DIMENSIONS

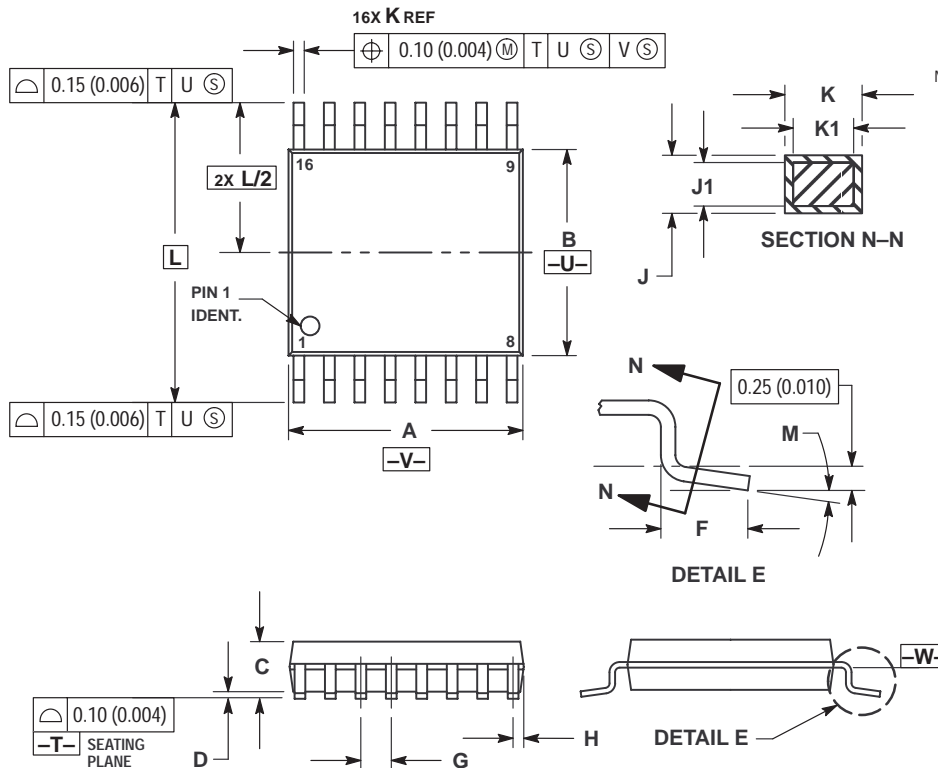
SOIC-16  
D SUFFIX  
CASE 751B-05  
ISSUE J



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: MILLIMETER.
  - DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  - MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  - DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

TSSOP-16  
DT SUFFIX  
CASE 948F-01  
ISSUE O



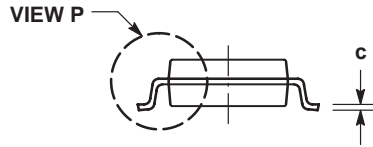
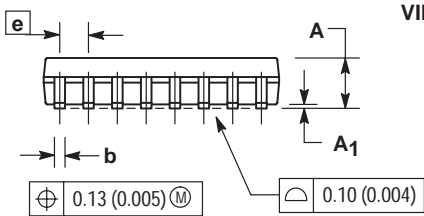
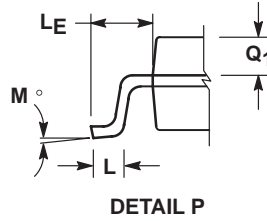
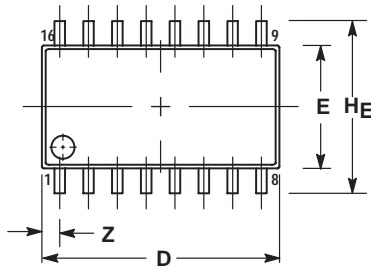
- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: MILLIMETER.
  - DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OF GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  - DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  - DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  - TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  - DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

# MC74VHCT259A

## PACKAGE DIMENSIONS

SOIC EIAJ-16  
M SUFFIX  
CASE 966-01  
ISSUE O




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>F</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>F</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

**Notes**

**Notes**

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