

DN8640S

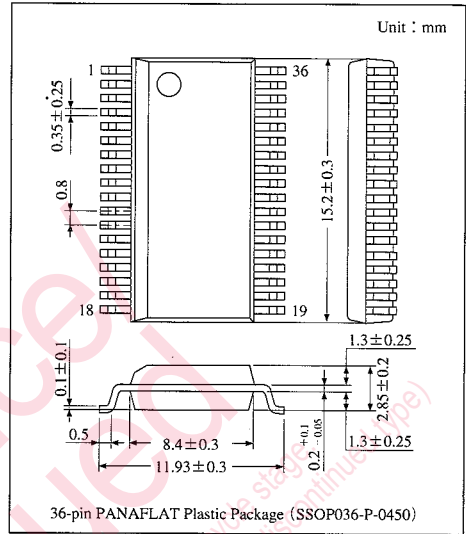
3X8-bit Shift Register Latch Driver IC

Overview

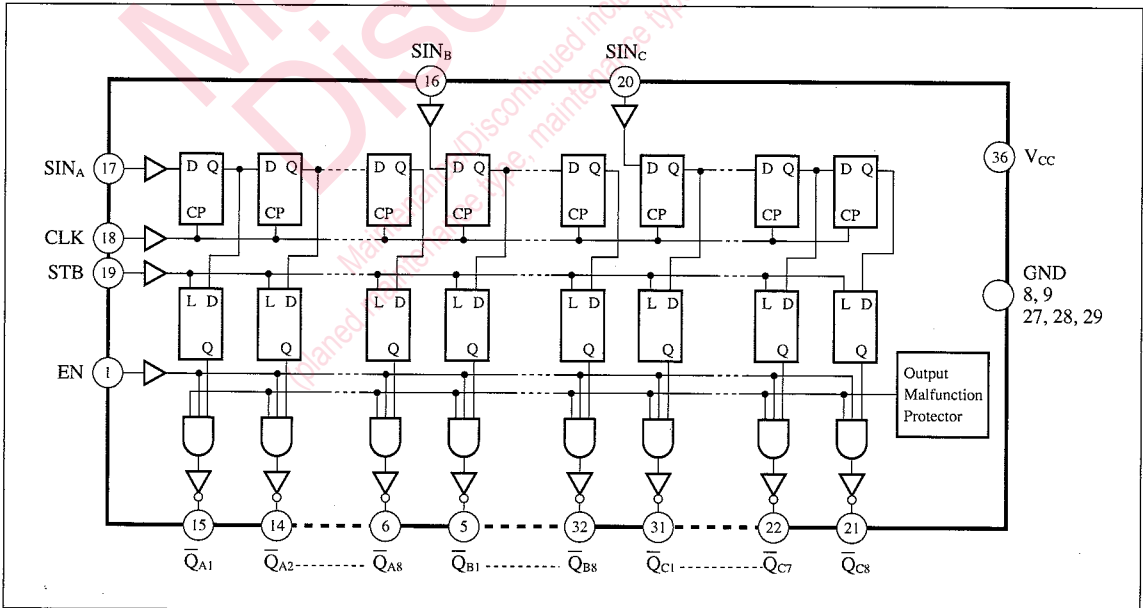
The DN8640S is an IC which incorporates a 3×8-bit shift register and a latch driver to meet high-speed operation, low power consumption and high-density printout of the thermal printers for the work processors, and so on. It employs the Bi-CMOS process in which the 3-circuit serial-in and 8-bit parallel-out functions are incorporated, the 3×8-step shift register block and latch block are composed of CMOS, and the 3×8-step parallel driver block is bipolar.

Features

- 3-circuit serial-in and parallel-out
Provided with CLK, EN, and STB input common to the 3 circuits
- Built-in output malfunctioning preventive circuit
- Low current at standby $I_{CC} = \leq 100 \mu A$
- High-breakdown, large current drive type output steps
Breakdown : 30V Output current : 120mA
- Surface mountable USONF-36D package (pin pitch : 0.8mm)



Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V _{CC}	0 to 7	V
Output voltage	V _O	0 to 30	V
Output current	I _O	120	mA
Power dissipation	P _D	1.3 *	W
Operating ambient temperature	T _{opr}	-20 to +75	°C
Storage temperature	T _{stg}	-55 to +125	°C

* When mounting onto the PCB, power dissipation is reduced at a rate of 10.4mW/°C from Ta=25°C

■ Recommended Operating Range (Ta=25°C)

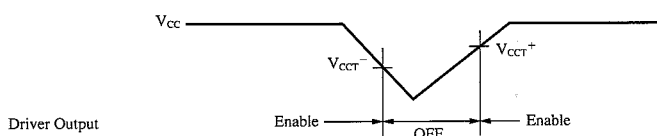
Parameter	Symbol	Condition	min	typ	max	Unit
Supply voltage	V _{CC}		4	5	6	V
Output voltage	V _O		—	—	30	V
Output current	I _O		—	—	100	mA
Clock frequency	f _{CLK}	Input Duty 40 to 60%	—	—	10	MHz
Input pulse width	CLK	t _w	40	—	—	ns
	STB		40	—	—	ns
Setup time	SIN	t _{su}	30	—	—	ns
	STB		40	—	—	ns
Hold time	SIN	t _h	20	—	—	ns
	STB		0	—	—	ns
Clock pulse rise time	t _r		—	—	500	ns
Clock pulse fall time	t _f		—	—	500	ns

* An allowable value changes depends on the number of simultaneously turned-on circuits and the duty. Use with power dissipation taken into full account.

■ Electrical Characteristics (Ta=25°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Input voltage	V _{IH}	V _{CC} =4 to 6V	0.7V _{CC}	—	V _{CC}	V
	V _{IL}		0	—	0.3V _{CC}	V
Input current	I _{IH}	V _{IH} =5V	—	—	25	μA
	I _{IL}	V _{IL} =0V	—	—	-25	μA
Output saturation voltage	V _{CE(sat)1}	I _{OL} =100mA	—	—	0.4	V
	V _{CE(sat)2}	I _{OL} =80mA	—	—	0.35	V
Output leakage current	I _{OLK1}	V _O =30V (output OFF)	—	—	50	μA
	I _{OLK2}	V _O =15V (output OFF)	—	—	25	μA
Supply current	I _{CC1}	Total driver output OFF	—	—	100	μA
	I _{CC2}	Driver output 1 circuit ON	—	—	5	mA
Output malfunctioning preventive Circuit operating voltage *	V _{CCR+}		2.9	—	3.9	V
	V _{CCR-}		2.6	—	3.6	V

* Output malfunctioning preventive circuit operating voltage timing chart



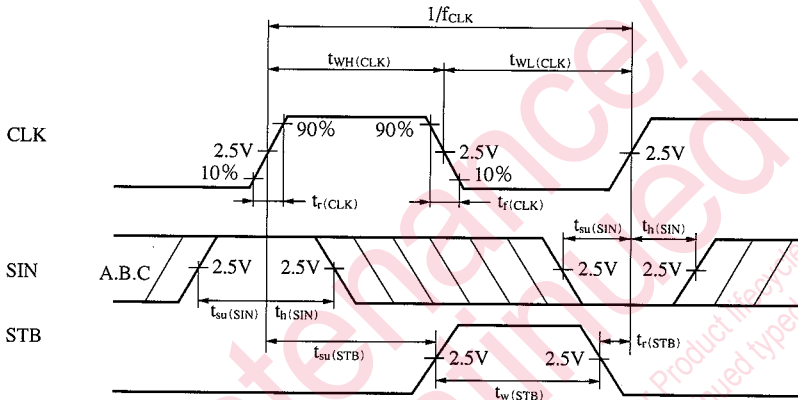
Others

■ Switching Characteristics (Ta=25°C)

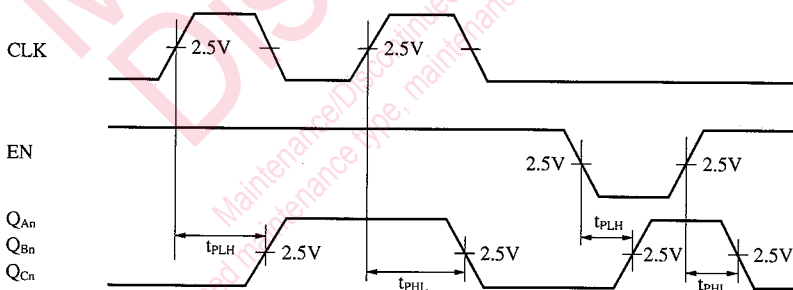
Parameter	Symbol	Input	Output	Condition	min	typ	max	Unit
Maximum clock frequency	f_{max}	CLK			10	—	—	MHz
Propagation delay time	t_{PLH}	CLK	\bar{Q}_n	$V_{CC}=5V$ $R_L=100\Omega$ $C_L=15pF$	—	—	2	μs
	t_{PHL}				—	—	0.5	μs
	t_{PLH}	EN	\bar{Q}_n		—	—	2	μs
	t_{PHL}				—	—	0.5	μs

■ Timing Chart

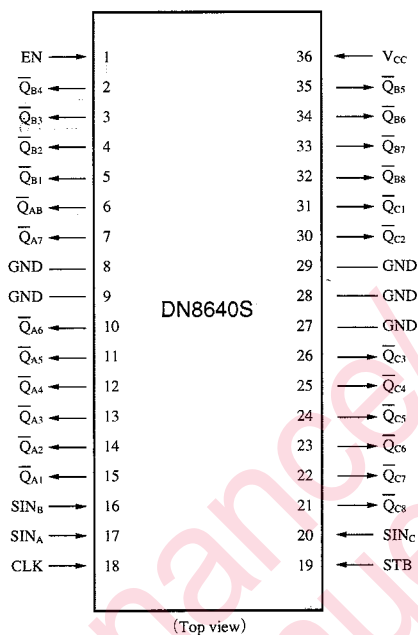
1. Input Timing



2. Propagation Delay Time



■ Pin Assignments



■ Functions Table

Input						Driver output					
CLK	EN	STB	SIN _A	SIN _B	SIN _C	\overline{Q}_{A1}	\overline{Q}_{An}	\overline{Q}_{B1}	\overline{Q}_{Bn}	\overline{Q}_{C1}	\overline{Q}_{Cn}
↑	L	×	×	×	×	H	H	H	H	H	H
↓	L	×	×	×	×	H	H	H	H	H	H
↑	H	L	×	×	×	nc	nc	nc	nc	nc	nc
↑	H	H	L	L	L	H	\overline{Q}_{An-1}	H	\overline{Q}_{Bn-1}	H	\overline{Q}_{Cn-1}
↑	H	H	H	H	H	L	\overline{Q}_{An-1}	L	\overline{Q}_{Bn-1}	L	\overline{Q}_{Cn-1}
↓	H	H	×	×	×	nc	nc	nc	nc	nc	nc

Note) H=High level, L=Low level, ×=Either "H" or "L" will do, ↑=Transition from "H" to "L", ↓=Transition from "H" to "L", nc=No change

Others

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