

CS1087

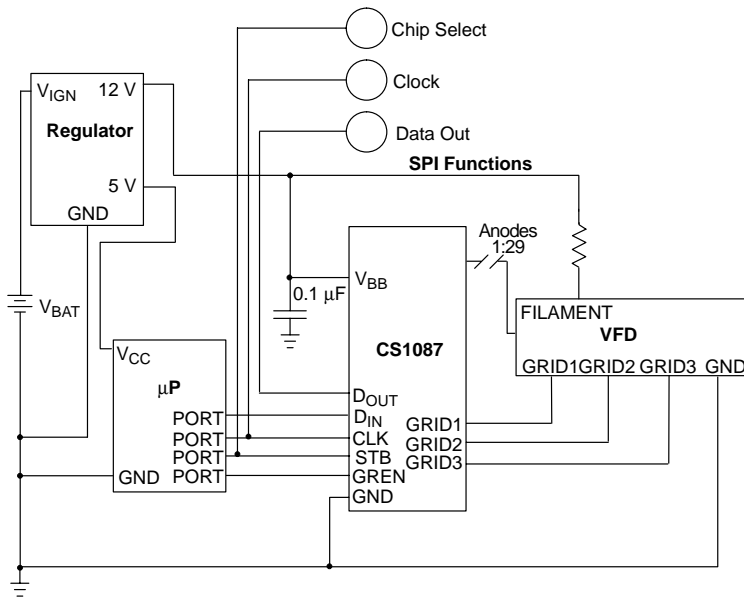
Vacuum Fluorescent Display Tube Driver

The VFD Driver is a microprocessor interface IC that drives a multiplexed VF (Vacuum Fluorescent) display tube. It consists of a 32-bit shift register, a 32-bit transparent data latch, a metal mask ROM, six 20 mA anode output drivers, twenty-three 2 mA anode output drivers, and three 50 mA grid drivers with output enables. The metal mask programmable ROM (at factory request) allows the 29 anode outputs and 3 grid outputs to be assigned to any of the 32 serial data bits.

Features

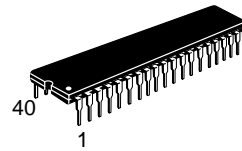
- Metal Mask ROM
- Six 20 mA Anode drivers
- Twenty-three, 2 mA Anode drivers
- Three, 50 mA Grid drivers
- Power On Reset
- Display Dimming Possible

APPLICATION DIAGRAM

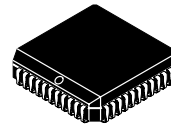


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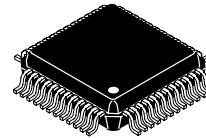
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**DIP-40
WIDE BODY
N SUFFIX
CASE 711**



**PLCC-44
FN SUFFIX
CASE 777**



**LQFP-48
FT SUFFIX
CASE 932**

ORDERING INFORMATION

Device	Package	Shipping
CS1087XN40	DIP-40 WIDE BODY	9 Units/Rail
CS1087XFN44	PLCC-44	23 Units/Rail
CS1087XFNR44	PLCC-44	500 Tape & Reel
CS1087XFTR48	LQFP-48	2000 Tape & Reel

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 7 of this data sheet.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit	
Supply Voltage (V_{BB})	-0.6 to +18	V	
Input Voltages (D_{IN} , CLK, STB, GREN)	-0.6 to +6.0	V	
Junction Temperature Range	-40 to +150	°C	
Storage Temperature Range	-55 to +150	°C	
ESD Susceptibility (Human Body Model)	2.0	kV	
ESD Susceptibility (Machine Model)	200	V	
Lead Temperature Soldering:	Wave Solder (through hole styles only) Note 1. Reflow (SMD styles only) Note 2.	260 Peak 230 Peak	°C

1. 10 second maximum.

2. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ($8.0\text{ V} \leq V_{BB} \leq 16.5\text{ V}$, $Gnd = 0\text{ V}$, $-40^\circ\text{C} \leq T_J \leq 105^\circ\text{C}$; unless otherwise stated.)

Parameter	Test Conditions	Min	Typ	Max	Unit
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 V_{BB} Input

V_{BB} Input Voltage	-	8.0	-	16.5	V
I_{BB0} Current	No outputs active, $V_{BB} = 16.5\text{ V}$	-	2.0	5.0	mA
Reset Mode	All outputs forced low.	-	6.5	7.5	V

 D_{IN} , CLK, STB Inputs

V_{IL1} , Input Low Voltage	-	-	-	1.6	V
V_{IH} , Input High Voltage	-	3.3	-	-	V
I_{IL} , Input Current	$V_{IN} = V_{IH}$	0	7.5	20.0	μA

GREN Input

V_{IL} , Input Low Voltage	-	-	-	1.6	V
V_{IH} , Input High Voltage	-	3.3	-	-	V
I_{IH} , Input Pull-down Current	$V_{IN} = 3.325\text{ V}$	-	30	60	μA

GRID1, GRID2, GRID3 Outputs

I_{OL}	Sink Current	1.0	-	-	mA
I_{OH}	Source Current	50	-	-	mA
V_{OL}	$I_{OUT} = 1.0\text{ mA}$	-	-	0.5	V
V_{OH}	$I_{OUT} = -50\text{ mA}$, $V_{BB} = 12\text{ V}$	$V_{BB} - 0.75$	-	V_{BB}	V

AN24 – AN29 Outputs

I_{OL}	Sink Current	400	-	-	μA
I_{OH}	Source Current	20	-	-	mA
V_{OL}	$I_{OUT} = 400\ \mu\text{A}$	-	-	0.5	V
V_{OH}	$I_{OUT} = -20\text{ mA}$, $V_{BB} = 12\text{ V}$	$V_{BB} - 0.5$	-	V_{BB}	V

AN1 – AN23 Outputs

I_{OL}	Sink Current	100	-	-	μA
I_{OH}	Source Current	2.0	-	-	mA
V_{OL}	$I_{OUT} = 100\ \mu\text{A}$	-	-	0.5	V
V_{OH}	$I_{OUT} = -2.0\text{ mA}$, $V_{BB} = 12\text{ V}$	$V_{BB} - 0.5$	-	V_{BB}	V

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ELECTRICAL CHARACTERISTICS (continued) (8.0 V ≤ V_{BB} ≤ 16.5 V, Gnd = 0 V, -40°C ≤ T_J ≤ 105°C; unless otherwise stated.)

Parameter	Test Conditions	Min	Typ	Max	Unit
D_{OUT} Output					
I _{OL}	Sink Current	1.0	–	–	mA
I _{OH}	Source Current	1.0	–	–	mA
V _{OL}	I _{OUT} = 1.0 mA	–	–	0.5	V
V _{OH}	I _{OUT} = -1.0 mA	3.9	–	5.0	V

AC Characteristics: Input and Output Timing

F _C , CLK Frequency	–	0	–	1.0	MHz
T _{CL} , CLK Low Time	–	200	–	–	ns
T _{CH} , CLK High Time	–	200	–	–	ns
T _{CR} , CLK Rise Time	–	–	–	100	ns
T _{CF} , CLK Fall Time	–	–	–	100	ns
T _{CD} , CLK Low to D _{OUT} Propagation Delay	–	–	–	200	ns
T _{DR} , D _{OUT} Rise Time	–	–	–	200	ns
T _{DF} , D _{OUT} Fall Time	–	–	–	200	ns
T _{SC} , STB Low to CLK High Time	–	50	–	–	ns
T _{ST} , STB High Time	–	500	–	–	ns
T _{AN} , STB High to Anode Output Propagation Delay	–	–	–	5.0	μs
T _{GL} , Grid Turn On Propagation Delay	V _{BB} = 12 V	–	–	2.0	μs
T _{GO} , Grid Turn Off Propagation Delay	V _{BB} = 12 V	–	–	5.0	μs
T _{GR} , Grid Rise Time	At rated load. Note 1.	0.50	–	2.00	μs
T _{GF} , Grid Fall Time	At rated load. Note 1.	0.35	–	2.00	μs
T _{AR} , Anode Rise Time	At rated load. Note 1.	0.40	–	2.00	μs
T _{AF} , Anode Fall Time	At rated load. Note 1.	0.40	–	2.50	μs

1. Grid and anode rise / fall times are measured from 10% and 90% points. Output currents are at the maximum rated currents for the respective stages.

PACKAGE LEAD DESCRIPTION

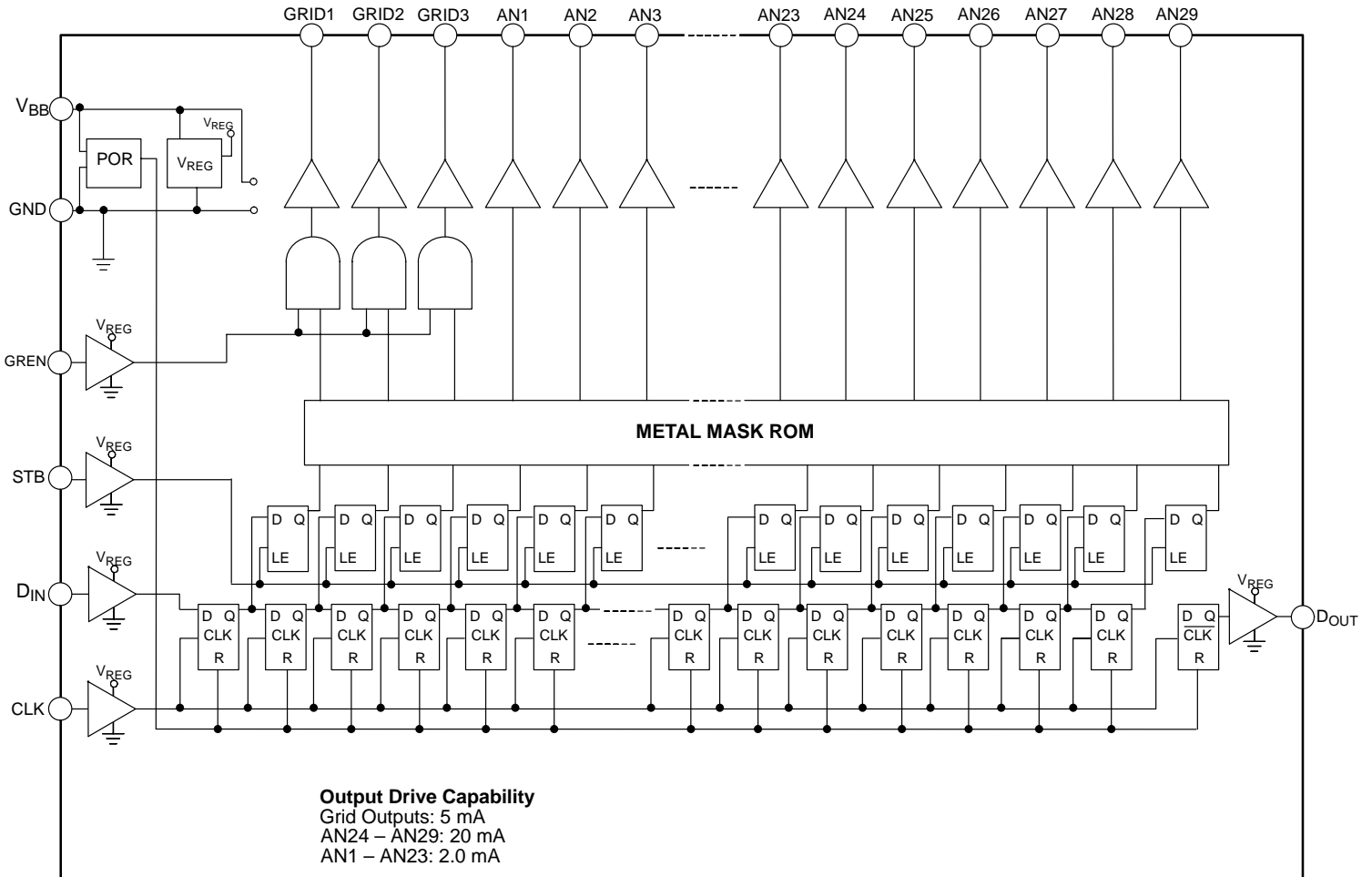
Package Lead Number			Lead Symbol	Function
40L DIP	44L PLCC	48L LQFP	(29 Anode Configuration)	
1	14	8	GRID1	50 mA grid output.
2	15	9	GRID2	50 mA grid output.
3	16	10	GRID3	50 mA grid output.
4	17	11	AN1	2.0 mA anode output.
5	18	13	AN2	2.0 mA anode output.
6	19	14	AN3	2.0 mA anode output.
7	20	15	AN4	2.0 mA anode output.
8	21	16	AN5	2.0 mA anode output.
9	22	17	AN6	2.0 mA anode output.
10	24	19	AN7	2.0 mA anode output.

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PACKAGE LEAD DESCRIPTION (continued)

Package Lead Number			Lead Symbol	Function
40L DIP	44L PLCC	48L LQFP	(29 Anode Configuration)	
11	25	20	AN8	2.0 mA anode output.
12	26	21	AN9	2.0 mA anode output.
13	27	22	AN10	2.0 mA anode output.
14	28	23	AN11	2.0 mA anode output.
15	29	25	AN12	2.0 mA anode output.
16	30	26	AN13	2.0 mA anode output.
17	31	27	AN14	2.0 mA anode output.
18	32	28	AN15	2.0 mA anode output.
19	33	29	AN16	2.0 mA anode output.
20	35	31	GND	Ground connection.
21	36	32	AN17	2.0 mA anode output.
22	37	33	AN18	2.0 mA anode output.
23	38	34	AN19	2.0 mA anode output.
24	39	35	AN20	2.0 mA anode output.
25	40	37	AN21	2.0 mA anode output.
26	41	38	AN22	2.0 mA anode output.
27	42	39	AN23	2.0 mA anode output.
28	43	40	AN24	20 mA anode output.
29	44	41	AN25	20 mA anode output.
30	2	43	AN26	20 mA anode output.
31	3	44	AN27	20 mA anode output.
32	4	45	AN28	20 mA anode output.
33	5	46	AN29	20 mA anode output.
34	6	47	D _{OUT}	Shift register data output.
35	7	1	D _{IN}	Shift register data input.
36	8	2	CLK	Shift register clock input.
37	9	3	STB	Transfer contents of shift registers to output stages.
38	10	4	GREN	Grid outputs enable.
39	1, 11, 12, 23, 34	5, 6, 12, 18, 24, 30, 36, 42, 48	NC	No connection.
40	13	7	V _{BB}	Supply voltage input.

BLOCK DIAGRAM



OPERATION DESCRIPTION

Upon the initial application of power, the power on reset function will cause all of the anode and grid driver outputs to be off and all shift register outputs to be set low. Data is fed into the shift register through the **D_{IN}** pin at the rising edge of the **CLK** input. Thirty two bits of data are capable of being stored by the shift register. Once the desired pattern is stored in the shift register, it can be transferred to the latch by setting the **STB** input high. The output of each latch drives its corresponding output stage. A logic high input to the shift register/latch will cause the corresponding output to turn on. A logic low input to the shift register/latch will cause the corresponding output to turn off. Please note that if the **STB** is held high, the outputs of the latch reflect the outputs of the corresponding shift register bits and will change if data is shifted in.

The three **GRID** outputs are gated by the **GREN** input. When **GREN** is low, the **GRID** outputs are forced low regardless of the state of the corresponding latch output. When **GREN** is high, the **GRID** outputs correspond to the state of their respective latch outputs. The anode outputs, **AN1** to **AN29** are always enabled.

The **D_{OUT}** pin is the output of the last stage of the shift register to allow serial cascading of this IC with other devices. Data from the last stage of the shift register is supplied to the **D_{OUT}** pin delayed by 1/2 **CLK** cycle. Data on the **D_{OUT}** output changes with the falling edges of the **CLK** to prevent logic race conditions between the **CLK** and the **D_{IN}** of the next IC in the serial chain.

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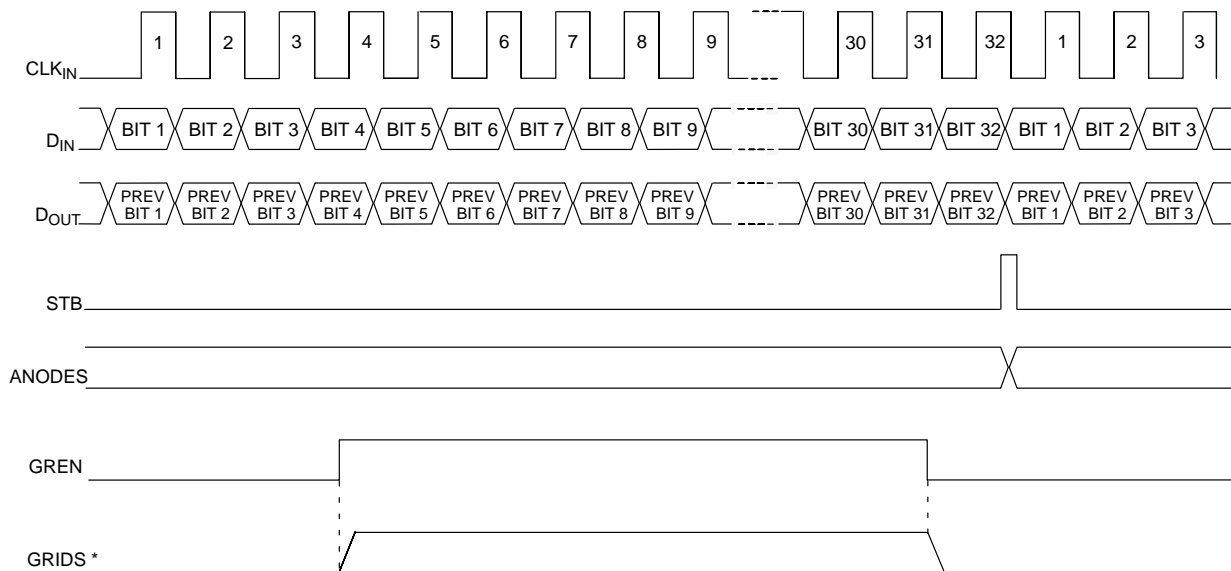
APPLICATION INFORMATION

Bit #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	G1	G2	G3	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13

Bit #	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29

Table 1: Bit Pattern, G = Grid, A = Anode.

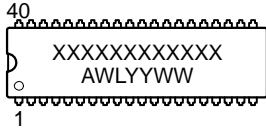
TYPICAL OPERATION



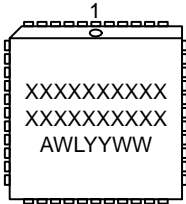
* Selected grid goes high only if input bit pattern from shift register to grid is high.

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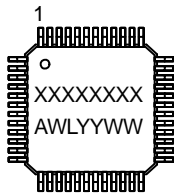
MARKING DIAGRAMS



**DIP-40
WIDE BODY
N SUFFIX
CASE 711**



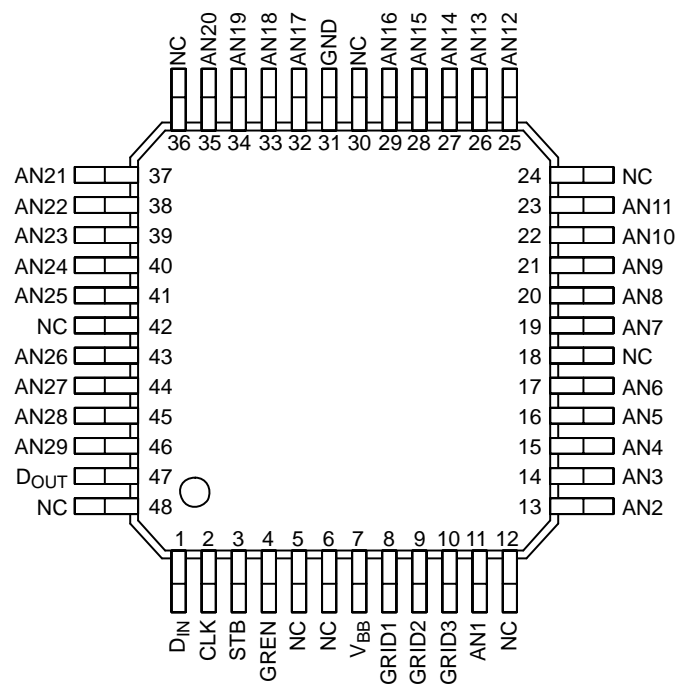
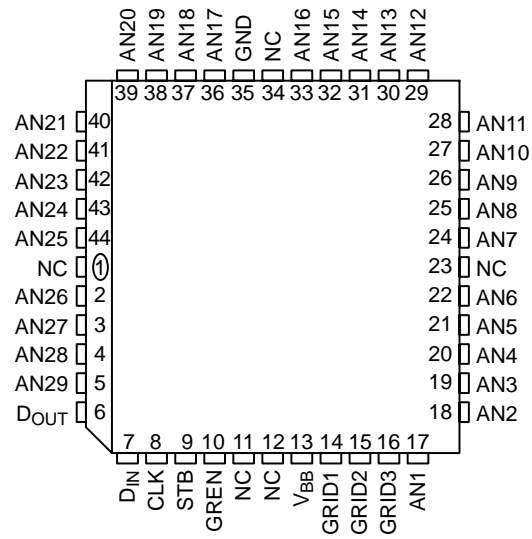
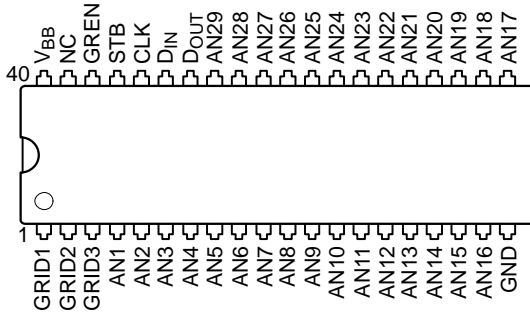
**PLCC-44
FN SUFFIX
CASE 777**



**LQFP-48
FT SUFFIX
CASE 932**

XXX... = Specific Device Code
 A = Assembly Location
 WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week

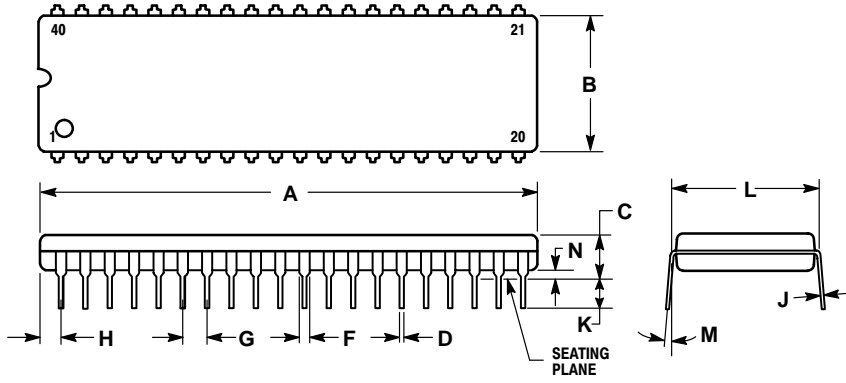
PIN CONNECTIONS



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PACKAGE DIMENSIONS

DIP-40
WIDE BODY
N SUFFIX
CASE 711-03
ISSUE C



NOTES:

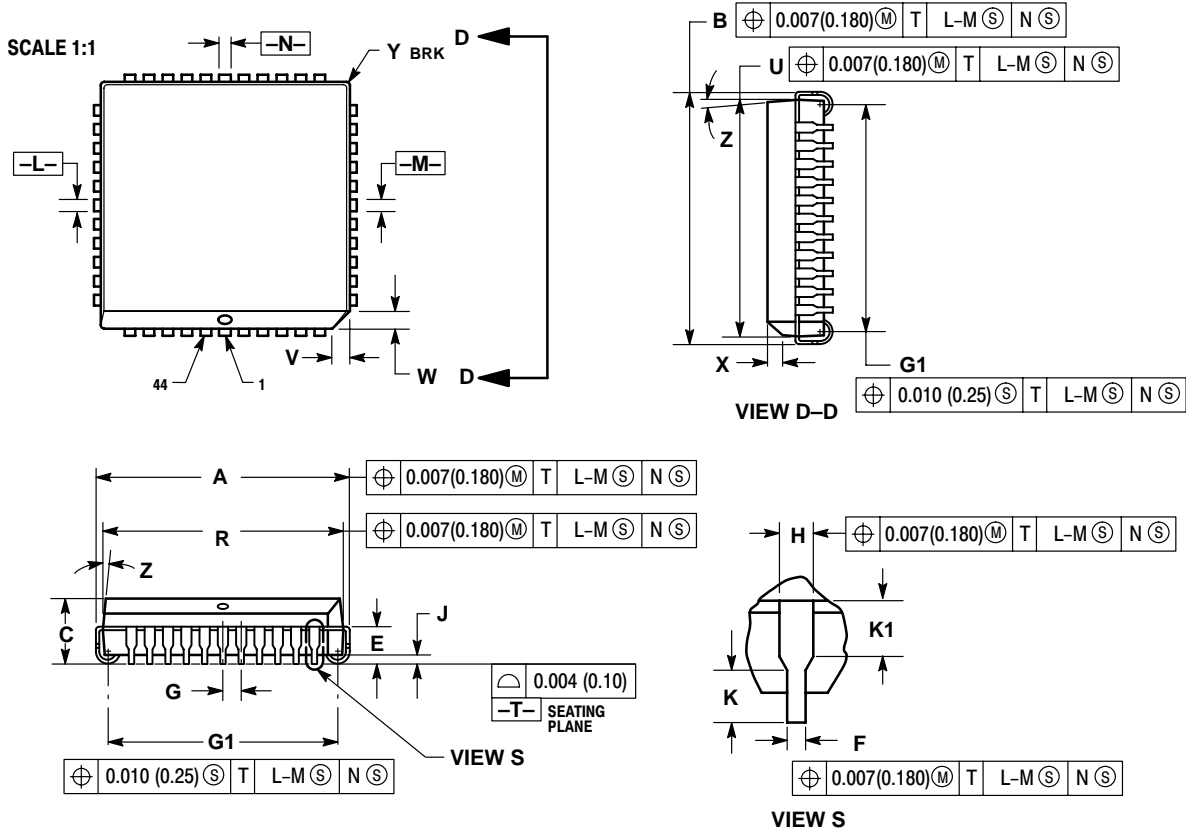
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

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PACKAGE DIMENSIONS

PLCC-44
FN SUFFIX
CASE 777-02
ISSUE C



NOTES:

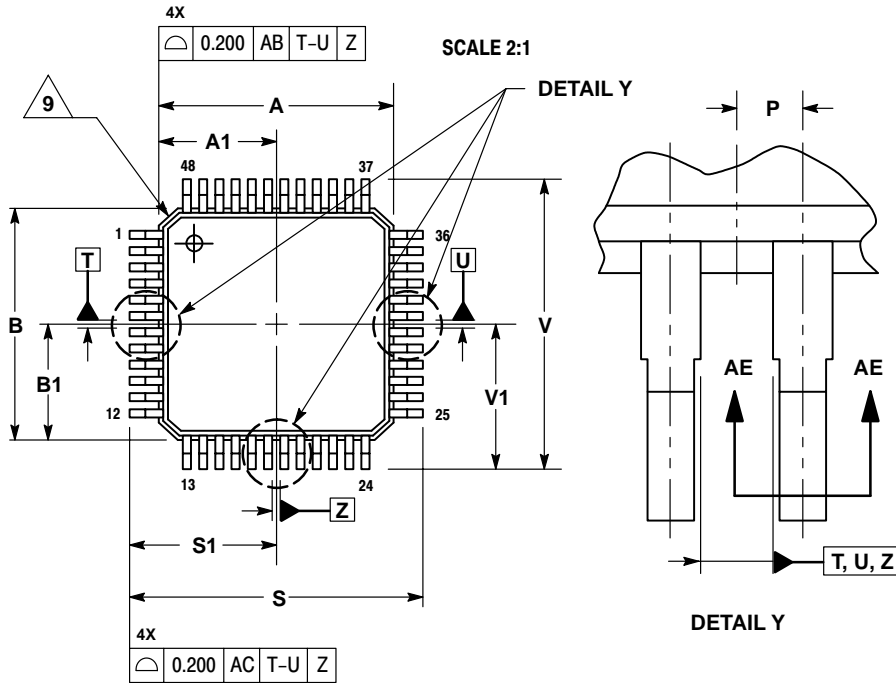
- DATUMS -L-, -M-, AND -N- ARE DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	---	1.02	---

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PACKAGE DIMENSIONS

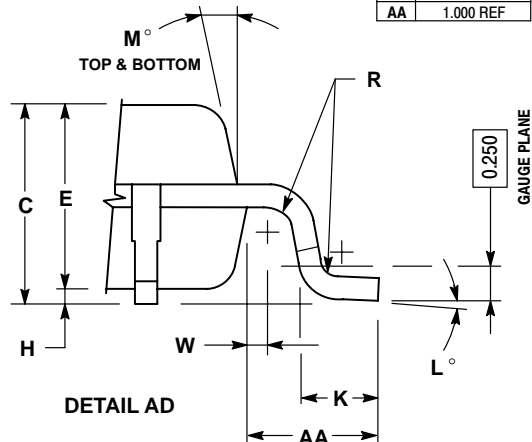
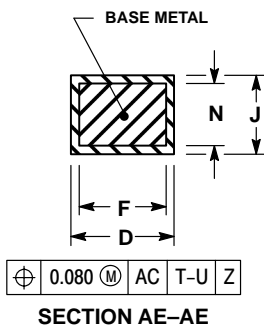
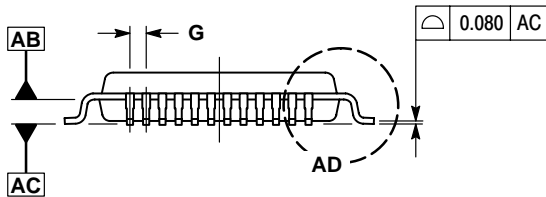
LQFP-48
FT SUFFIX
CASE 932-02
ISSUE E



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
 4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
 5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
 6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
 7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
 8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
- △ EXACT SHAPE OF EACH CORNER IS OPTIONAL.

DIM	MILLIMETERS	
	MIN	MAX
A	7.000	BSC
A1	3.500	BSC
B	7.000	BSC
B1	3.500	BSC
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	1°	5°
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	



PACKAGE THERMAL DATA

Parameter	DIP-40 WIDE BODY	PLCC-44	LQFP-48	Unit
R _{θJC}	Typical	20	16	°C/W
R _{θJA}	Typical	45	55	°C/W

Notes

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JAPAN: ON Semiconductor, Japan Customer Focus Center

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Phone: 81-3-5740-2745
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