SAMSUNG SEMICONDUCTOR

KDA0484

85MHz Monolithic CMOS True-Color RAM DAC

Preliminary — March, 1994

KDA0484 FEATURES

- 8:1, 4:1, 2:1, 1:1 MUX Pixel Ports
- 85MHz, 75MHz Pixel Clock
- Separate 8-bit VGA Port
- Triple 8-bit D/A Converters
- Three 256x8 Color Palette RAMs
- Hardware Cursor 32x32x2
- Three 3x8 Cursor Color Palettes
- 0 or 7.5 IRE Blanking Pedestal
- Voltage Reference
- Snow-Free Circuitry
- Power-Down Mode
- Dual Port Video Memory Support
- VRAM and WRAM Shift Clock Support
- Supports VGA in a True-Color Window
- Monitors SENSE Output
- 84-Pin PLCC Package

OVERVIEW

The KDA0484 is designed for high-performance color graphics applications. The KDA0484 has four byte-wide pixel input ports (A through D), three 256x8 color look-up tables with triple 8-bit video D/A converters (configurable for 6-bit or 8-bit D/A), and a programmable 32x32x2 cursor with its own color palette. The KDA0484 is also configurable for lower-performance VGA mode.

The color palette may be by-passed in any true-color mode. There are 32 pins allocated for the P7:P0 port, support pseudo-color (8-bit) true-color (16- and 24-bit), and a variety of packed and sparse pixel formats. The color palette may be by-passed in any of the operational modes, except VGA (8:1 and 4:1 MUX modes). The KDA0484 generates RS-343A-compatible video signals into a doubly-terminated 75Ω load.

FUNCTIONAL DESCRIPTION

Microprocessor Interface

The KDA0484 support a standard microprocessor bus interface to directly access to the color palette RAM. Microprocessor data is transferred through the D0-D7 data pins. Read/write timing is controlled by the RD* and WR* inputs (Figure 1).

The RS0-RS3 select inputs specify which control register the microprocessor accesses. The 8-bit address register addresses the color palette RAM, eliminating the need for external address multiplexers. For DATA and ADDRESS, the LSB is D0 and ADDR0, respectively.

Reading Data From Color Palette RAM

The microprocessor loads the address register with the address of the color palette RAM location to be read. The contents at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The microprocessor performs three successive read cycles (8 bits each of red, green, and blue), using RS0-RS3 to select the color palette RAM. Following the blue read cycle, the contents at the address specified by the address register are copied into the RGB registers, and the address register increments again. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles, until the entire block is read.

Writing Data To Color Palette RAM

The microprocessor writes the address register with the address of the color palette RAM location to be modified. The microprocessor performs three successive write cycles (8-bits each of red, green, and blue), using RS0-RS3 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are assembled into a 24-bit word and written to the location specified by the address register. The address register increments to the next location, which the microprocessor may modify by writing another sequence of RGB data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block is written.

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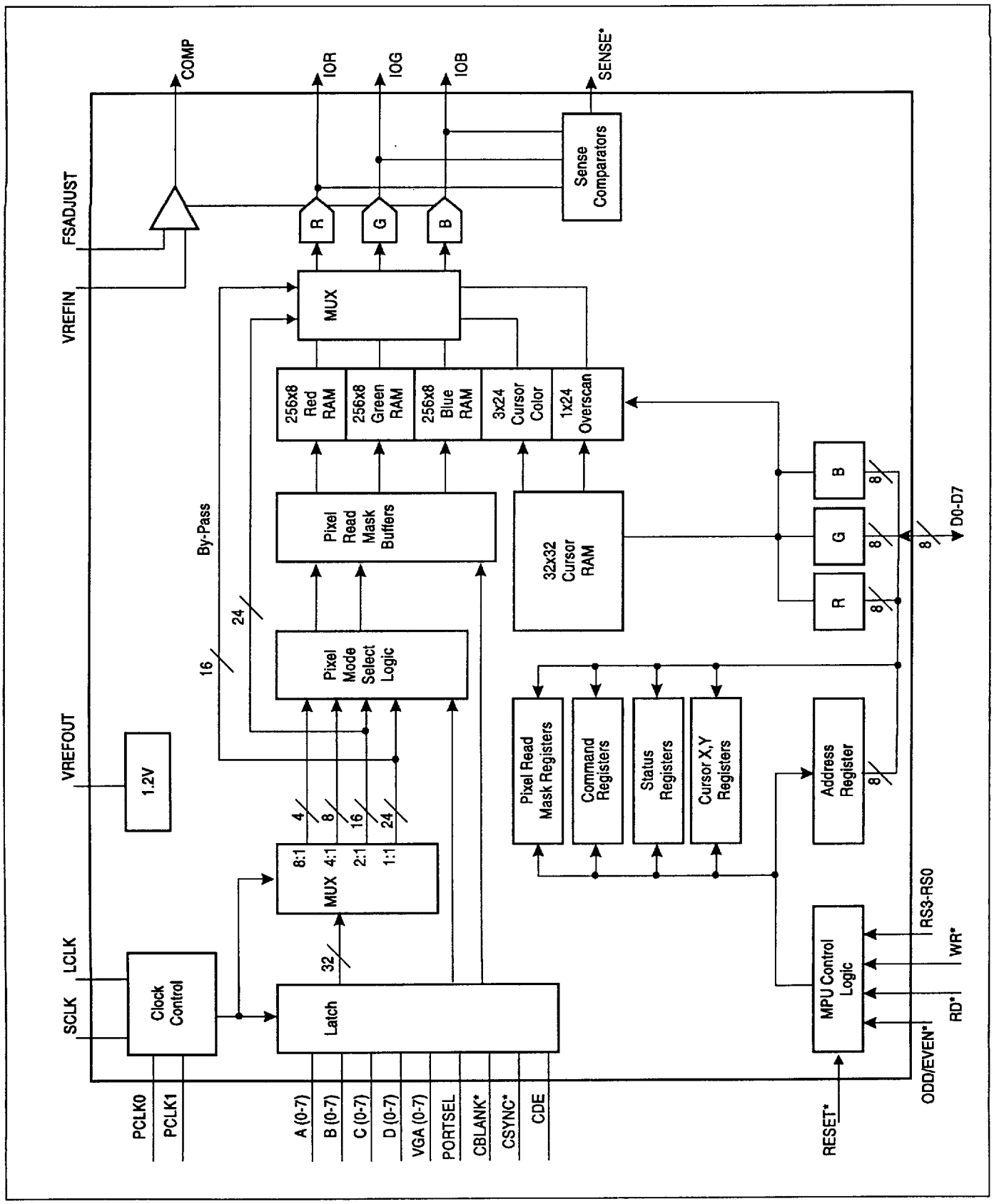

Figure 1. KDA0484 Block Diagram

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FUNCTIONAL DESCRIPTION

Writing Cursor and Overscan Color Data

The microprocessor writes the address register with the address of the cursor color location to be modified. The microprocessor performs three successive write cycles (8-bits each of red, green, and blue), using RS0-RS3 to select the cursor color registers. After the blue write cycle, the 3 bytes of red, green, and blue color information are assembled into a 24-bit word and written to the cursor color location specified. The address register increments to the next location, which the microprocessor may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block is written.

RS3-RS0	Access	Addressed by MPU
0000	R/W	address register; palette/cursor RAM write
0001	R/W	6/8-bit color palette data
0010	R/W	pixel mask register
0011	R/W	address register; palette/cursor RAM read
0100	R/W	address register; cursor/overscan color write
0101	R/W	cursor overscan and color data
0110	R/W	command register 0
0111	R/W	address register; cursor/overscan color read
1000	R/W	command register 1
1001	R/W	command register 2
1010	R	status register
1011	R/W	cursor RAM array data
1100	R/W	cursor x-low register
1101	R/W	cursor x-high register
1110	R/W	cursor y-low register
1111	R/W	cursor y-high register

Table 1. Control Input Truth Table

Reading Cursor Color Data

The microprocessor loads the address register with the address of the cursor color location to be read. The contents of the cursor color register at a given address are copied into the RGB registers, and the address register increments to the next cursor color location. The microprocessor performs three successive read cycles (8 bits each of red, green, and blue), using RS0-RS3 to select the cursor color register.

Following the blue read cycle, the contents at the address specified by the address register are copied into the RGB registers, and the address register increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles, until the entire block is read.

Additional Information

When accessing the color palette RAM, the address register resets to $00, following a blue read or write cycle to RAM location $FF. The microprocessor interface operates asynchronously to the pixel clock. Data transfers (occurring between the color palette RAM and the color registers) are synchronized by internal logic, and take place between microprocessor accesses. Internal logic maintains previous output color data on the analog outputs during transfer between RGB registers and look-up table RAMs. This ensures a snow-free screen during microprocessor access to the color palette RAMs.

To track RGB read/write cycles, the address register has extra ADDRa and ADDRb bits to count modulo three. These bits are reset to zero when the microprocessor writes to the address register, but not reset to zero when the microprocessor reads the address register. The microprocessor does not have access to these bits. The microprocessor may read the address register at any time without modifying its contents or the existing read/write mode.

Cursor RAM Array Access

The 32x32x2 cursor RAM is also accessed in a planar format, in which only 7 address bits are used. The 8th bit determines which plane (0 or 1) of the cursor RAM array is accessed. A single address presented to the cursor RAM accesses 8-bit locations in plane 0 or 1, depending on the state of address bit 7.

After each planar format access, the address increments. The microprocessor uses the binary ADDRcounter to access the cursor RAM array (Table 2). ADDR is the same binary counter used for RGB auto-incrementing. A write to ADDR, after cursor auto-incrementing is initiated, resets the cursor auto-incrementing logic until the cursor RAM array is re-accessed.

Cursor auto-incrementing then begins from the address written. A read from the ADDR does not reset the auto-incrementing logic. Color palette RAM and cursor RAM share one external address register. Microprocessor addressing for this and all other registers is determined by the external register select lines RS3-RS0 (Tables 1 and 2).

Operation In 6-Bit And 8-Bit

The CR01 bit specifies if 6- or 8-bits of color information per cycle. For 6-bit operation, the KDA0484's full-scale output current is about 1.5% lower than during 8-bit operation (the 2 LSBs of each 8-bit DAC are "0"s in 6-bit mode). In 6-bit mode, color data is contained on the lower 6 bits of the data bus. When writing color data, D6 and D7 are ignored; during color read cycles (D6=0 and D7=0).

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FUNCTIONAL DESCRIPTION

In 8-bit mode, D0 is LSB and D7 is MSB of color data, while in 6-bit operation D0 is LSB and D5 is MSB. Accessing the cursor RAM array does not depend on the resolution of the DACs.

Frame Buffer Clocking

The KDA0484 generates the video frame buffer shift clock. SCLK is one-eighth, one-fourth, or one-half the pixel clock rate, depending on whether multiplexing is 8:1, 4:1, or 2:1, respectively.

In the 1:1/VGA mode, SCLK=LCLK. P0-P7 (A through D) are pixel data, 8-bits per pixel (4:1 MUX) and 4-bit per pixel (8:1 MUX) for 4 and 8 horizontally-consecutive pixels. P0-P7 (A through D) are always latched on the rising edge of LCLK. The pixel clock is specified to be either PCLK0 or PCLK1 by command bit CR24.

Power-Down Mode

The KDA0484 incorporates a power-down capability controlled by bit CR00. If CR00=0, the KDA0484 functions normally; if CR00=1, the DACs and power to the RAM are turned off, but RAM retains data.

Also, the microprocessor may read or write to the RAM while the pixel clock is running. The RAM automatically powers up during read/write cycles and shuts down when access is completed. In power-down mode, the DACs do not output current, and the three command registers can still be written to or read by the microprocessor. The output DACs require about one second to turn off or on, depending on the compensation capacitor used.

Frame Buffer Pixel Port Interface

The KDA0484 has four 8-bit pixel ports (A through D) interface to frame buffer memory.

Port A corresponds to the first pixel of the first line of the display. This is the first pixel fed to the analog outputs, followed by B, then C, and finally D; repeating the pattern until the first scan line is displayed.

For the cursor display, the output sequence depends on CR23 and the ODD/EVEN* input. For example, when either interlaced or non-interlaced operation is selected, the current field is displayed.

Scan line 1 is always displayed first in interlaced mode and is the first line of the EVEN field. In the non-interlaced mode, scan line 2 follows scan line 1. In interlaced mode, scan line 2 is the first line of the ODD field and is displayed only after the entire EVEN field is displayed and the ODD/EVEN* pin has toggled. Only the ODD lines or only the EVEN lines are displayed, if ODD/EVEN* does not change.

ADDR 0-7 (counts binary)	ADDRa,b (modulo 3)	RS0	RS1	RS2	RS3	Addressed by MPU
$00-$FF	00	1	0	0	0	color palette RAM red component
	01	1	0	0	0	color palette RAM green component
	10	1	0	0	0	color palette RAM blue component
xxxx xx00	00	1	0	1	0	overscan color red component
	01	1	0	1	0	overscan color green component
	10	1	0	1	0	overscan color blue component
xxxx xx01	00	1	0	1	0	cursor color 1 red component
	01	1	0	1	0	cursor color 1 green component
	10	1	0	1	0	cursor color 1 blue component
xxxx xx10	00	1	0	1	0	cursor color 2 red component
	01	1	0	1	0	cursor color 2 green component
	10	1	0	1	0	cursor color 2 blue component
xxxx xx11	00	1	0	1	0	cursor color 3 red component
	01	1	0	1	0	cursor color 3 green component
	10	1	0	1	0	cursor color 3 blue component
$00-$7F	N/A	1	1	0	1	cursor RAM array, plane 0
$80-$FF	N/A	1	1	0	1	cursor RAM array, plane 1

When the cursor color register or overscan register is addressed, the 5MSBs of the address register are ignored. Therefore, when the address register is read and the previous access was to the cursor color registers or overscan register, address register bits [7-3] are returned as either ones or zeros.

Table 2: Address Register Operation And Auto-Incrementing

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FUNCTIONAL DESCRIPTION & OPERATING MODES

Figure 2 shows the interlaced and non-interlaced display scan. Non-interlaced display scan is equal to one frame. Interlaced display scan is equal to one frame with odd and even fields.

OPERATING MODES

4-Bits Per Pixel (8:1 MUX)

The 32 input bits are multiplexed 8:1 and configured for 4-bits-per-pixel. There are eight independent 4-bit pixel ports, P7:4 (A-D) and P3:0 (A-D). The pixel bits are latched on the LCLK rising edge, which occurs once every eight PCLK cycles. SCLK equals the PCLK selected, divided by 8. The 4 bits from each port select 1 of 16 locations (RAM address 0-15) in the palette (Table 6).

8-Bits Per Pixel (4:1 MUX)

The 32 input bits are multiplexed 4:1 and configured for 8-bits per pixel. There are four independent 8-bit pixel ports (A-D). The pixel bits are latched on the LCLK rising edge, which occurs once every four PCLK cycles. SCLK equals the PCLK selected, divided by 4. The 8-bits from each port select 1 of 256 palette locations (Table 6).

16-Bits Per Pixel (2:1 MUX)

The 32 input bits are multiplexed 2:1 and configured for 16-bits per pixel. Multiplexing of 2:1 is selected through bit CR12. There are two independent 16-bit pixel ports (B-A) and (D-C). The pixel bits are latched on the LCLK rising edge, which occurs once every two PCLK cycles. SCLK equals the PCLK selected, divided by 2. The pixel bits multiplexed in this mode are from the same ports of RGB color formats of 5:5:5 or 5:6:5. P7D and P7B are ignored when the 5:5:5 color format is selected (Tables 3, 4, and 6).

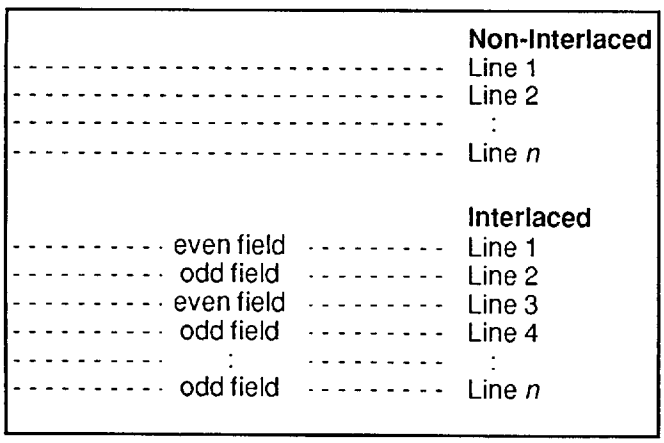

Figure 2: Interlaced and Non-Interlaced Display Operation

Bit CR14 enables or disables true-color palette by-pass. In by-pass mode, pixel data by-passes the palette as well as the pixel mask and is transferred to the proper MSBs of the respective DACs. When the by-pass mode is not selected, the pixel data indexes the proper location in the palette, and the correct color information is passed to the respective DACs.

Bit CR22 determines SPARSE or CONTIGUOUS palette addressing. For SPARSE palette addressing, each color component of pixel data is mapped to the MSBs of the respective palette address; the LSBs are set to zero. For CONTIGUOUS palette addressing, each color component is mapped to the LSBs of the respective palette address; the MSBs are set to zero. The color palette values indexed (for either SPARSE or CONTIGUOUS addressing) are transferred to the DACs.

In 5:5:5 or 5:6:5 color format, the display can contain 32K or 64K simultaneous colors. The DACs can be configured for 6- or 8-bits of resolution in this mode.

16-Bits Per Pixel (1:1 MUX)

The 1:1 multiplexing mode is selected through CR12. When this mode is selected, two independent 16-pit pixel ports, (B-A) and (D-C), are latched on the rising edge of LCLK and are multiplexed 1:1. Selection between the two ports is made by bit CR10. One rising edge of LCLK occurs every PCLK cycle. SCLK is equal to the PCLK selected.

Bit P7D switches between the two ports on a pixel-by-pixel basis if 5:5:5 RGB color format (CR13=0) and real-time pixel port switching are enabled (CR11=1). If PORTSEL is "0", the VGA port is multiplexed, regardless of the state of P7D. Bit P7B is ignored internally in 5:5:5 mode. Real-time pixel port switching is not supported for 5:6:5 RGB color format.

Bits P7B and P7D are ignored internally if 5:5:5 RGB color format is selected and real-time pixel port switching is disabled (CR11=0. Programming bit CR10 determines switching for both 5:5:5 and 5:6:5 RGB color formats.

CR14 enables or disables true-color palette by-pass. When enabled, pixel data by-passes the palette as well as the pixel mask and is transferred to the proper MSBs of the respective DACs. When disabled, the pixel data indexes the proper locations in the palette, and the independent RGB color values are passed on to the respective DACs. When either 5:5:5 or 5:6:5 color format is selected, the display can contain 32K or 64K simultaneous colors. The DACs can be configured for 6- or 8-bits of resolution in this mode.

OPERATING MODES

24-Bits Per Pixel (1:1 MUX)

If 24-bits per pixel is selected, there is one 24-bit pixel port. The pixel bits, P7:0(C-A), are latched on the rising edge of LCLK and are multiplexed 1:1. P(7:0)(D) are ignored. One rising edge of LCLK occurs every PCLK cycle. SCLK is equal to the PCLK selected. The RGB color format in this mode is 8:8:8.

CR14 enables or disables true-color palette by-pass. When enabled, the pixel data by-passes the palette and the pixel mask and is transferred to the proper MSBs of the respective DACs. When disabled, the pixel data indexes the proper locations in the palette, and the independent RGB color values are passed on to the respective DACs. When 8:8:8 color format is selected, the display can contain 16.8 million simultaneous colors. The DACs should be configured for 8-bits of resolution in this mode (Tables 5 and 7).

VGA Port

An 8-bit pixel port is provided to support VGA pixel data. The data is latched on the rising edge of LCLK, which occurs once every PCLK cycle. SCLK equals the PCLK selected. Setting PORTSEL=0 ensures that the VGA port is selected. PORTSEL=1 selects the pixel port.

To use the VGA PORTSEL feature, the RAM DAC must be configured in the 1:1 multiplexing mode through the RAM (CR14=0) or palette by-pass (CR14=1). After the RAM DAC is properly configured, the VGA PORTSEL can be used to select between the pixel port and the VGA port on a pixel-by-pixel basis. The VGA port always has priority over the color palette when selected. Only PCLK0 should be used when switching between the VGA and pixel ports on a pixel-by-pixel basis.

The 8-bit VGA data forms a common index into the palette, selecting 1 of 256 colors. Valid data begins at address zero.

Bit	MSB															LSB
Format	S	R	R	R	R	R	G	G	G	G	G	B	B	B	B	B
Port 1	S	P6B	P5B	P4B	P3B	P2B	P1B	P0B	P7A	P6A	P5A	P4A	P3A	P2A	P1A	P0A
Port 2	S	P6D	P5D	P4D	P3D	P2D	P1D	P0D	P7C	P6C	P5C	P4C	P3C	P2C	P1C	P0C

If CR11=0, then S=CR10 bit, 16-bit per pixel port swtich control (1:1 multiplexing). If CR11=1, then S=P7D bit, real-time pixel port switch (1:1 multiplexing).

Table 3: 5:5:5 RGB Color Format For 2:1 and 1:1 MUX

Bit	MSB															LSB
Format	R	R	R	R	R	G	G	G	G	G	G	B	B	B	B	B
Port 1	P7B	P6B	P5B	P4B	P3B	P2B	P1B	P0B	P7A	P6A	P5A	P4A	P3A	P2A	P1A	P0A
Port 2	P7D	P6D	P5D	P4D	P3D	P2D	P1D	P0D	P7C	P6C	P5C	P4C	P3C	P2C	P1C	P0C

Table 4: 5:6:5 RGB Color Format For 2:1 and 1:1 MUX

Bit	MSB																						LSB
Format	R	R	R	R	R	R	R	R	G	G	G	G	G	G	G	G	B	B	B	B	B	B	B	B
Port 1	P7C	P6C	P5C	P4C	P3C	P2C	P1C	P0C	P7B	P6B	P5B	P4B	P3B	P2B	P1B	P0B	P7A	P6A	P5A	P4A	P3A	P2A	P1A	P0A

Table 5: 24-Bits Per Pixel RGB Color Format

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OPERATING MODES

Operating Mode	MUX Rate	Ports MUXed	PORTSEL	P7D	CR10	CR11	CR12	CR13	CR15	CR16
VGA	1:1	VGA(7:0)	0	x	x	x	x	x	0	0
4 Bits Per Pixel	8:1	P7:4(A) P3:0(A) P7:4(B) P3:0(B) P7:4(C) P3:0(C) P7:4(D) P3:0(D)	1	Data	x	x	x	x	1	1
8 Bits Per Pixel	4:1	P7:0(A) P7:0(B) P7:0(C) P7:0(D)	1	Data	x	x	x	x	0	1
16 Bits Per Pixel (5:5:5—see Table 3)	2:1	P7:0(B-A) P7:0(D-C)	1	x	x	x	0	0	1	0
16 Bits Per Pixel (5:6:5—see Table 4)	2:1	P7:0(B-A) P7:0(D-C)	1	Data	x	x	0	1	1	0
16 Bits Per Pixel (5:5:5)	1:1	P7:0(B-A)	1	x	0	0	1	0	1	0
16 Bits Per Pixel (5:5:5)	1:1	P7:0(D-C)	1	x	1	0	1	0	1	0
16 Bits Per Pixel (5:5:5—see Table 3)	1:1	P7:0(B-A)	1	0	x	1	1	0	1	0
16 Bits Per Pixel (5:5:5—see Table 3)	1:1	P7:0(D-C)	1	1	x	1	1	0	1	0
16 Bits Per Pixel (5:6:5—see Table 4)	1:1	P7:0(B-A)	1	x	0	x	1	1	1	0
16 Bits Per Pixel (5:6:5—see Table 4)	1:1	P7:0(D-C)	1	Data	1	x	1	1	1	0
24 Bits Per Pixel (see Table 5)	1:1	P7:0(C-A)	1	x	x	x	x	x	0	0

Table 6: Operating Modes (Pixel Port Configuration)

OPERATING MODES

Pixel Read Mask Register

The pixel data can be masked with the 8-bit pixel read mask register before transfer to the color palette; this is achieved wit the 8-bit pixel mask register. The pixel data is bit-wise logically ANDed with the contents of the pixel read mask register. The result is used to address the color palette RAM. The addressed location provides 24-bits of color information to the three converters. Pixel masking is enabled for all modes of operation, except when true-color by-pass is enabled. The pixel read mask register is not initialized at power-up/reset and must be initialized (Table 7).

Cursor Operation

The KDA0484 has an on-chip, three-color 32x32x2, user-definable cursor. This cursor can be used with either interlaced or non-interlaced systems. The pattern for the cursor is provided by the cursor RAM, which may be accessed by the microprocessor at any time. The cursor is positioned through the cursor position register (Xp, Yp). A (0, 0) written to the cursor position registers will place the cursor off the screen. A (1, 1) will place the lower right pixel of the cursor on the upper left corner of the screen (Figure 3).

Cursor positioning is relative to CDE. The cursor position is not dependent on CBLANK*. The reference point of the cursor (row 0, column 0) is in the lower right corner. The cursor Xp position is relative to the first rising edge of LCLK when CDE is sampled at logical "1". The cursor Yp position is relative to the first rising edge of LCLK when CDE is sampled at logical "1" after the CDE vertical blanking interval is determined.

If a CDE transition from logical "0" to "1" (as determined by LCLK) does not occur within 2048 PCLKs (2048 LCLKs in 1:1 MUX mode), CDE is in vertical blanking. In 8:1, 4:1, or 2:1 MUX mode, cursor timing is based on the PCLK selected. When the MUX rate is 1:1, cursor timing is based on LCLK.

Only one cursor pattern per frame is displayed at the location specified for interlaced and non-interlaced display formats, regardless of the number of updates to (Xp, Yp). The cursor's vertical or horizontal location is not affected during any frame displayed.

The only restriction on updating (Xp, Yp) is that both cursor position registers be written when the cursor location is updated. Internal x- and y-position registers are loaded after the upper byte of Yp has been written to ensure one cursor pattern per frame at the correct location. The cursor pattern is displayed at the last cursor location written.

The cursor pattern can be displayed in an interlaced system if bit CR23 in command register 2 is a "1". If Yp is >32 ($0020), and ≤4095 ($0FFF), the first cursor line displayed depends on the state of the ODD/EVEN* pin and the value of Yp. If Yp is an even number, the data in row 31 of the cursor RAM array is displayed during the even field, starting at the position specified by (Xp, Yp). Each subsequent scan line displayed in the even field will correspond to every alternate active cursor line after row 31 in the cursor RAM array.

During the odd fields, the even rows from the cursor RAM array are displayed starting with row 30, at the position specified by (Xp, Yp+1). Each subsequent scan line displayed in the odd field will correspond to every alternate active cursor line after row 30 in the cursor RAM array.

If Yp is an odd number, then the data in row 31 of the cursor RAM array is displayed during the odd field, starting at the position specified by (Xp, Yp). Each subsequent scan line displayed in the odd field will correspond to every alternate active cursor line after row 31 in the cursor RAM array. During even fields, the even rows from the cursor RAM array are displayed starting with row 30, at the position specified by (Xp, Yp+1). Each subsequent scan line displayed in the even field corresponds to every alternate active cursor line after row 30 in the cursor RAM array.

If Yp is <32 ($0020), cursor display does not depend on whether Yp is odd or even. If the ODD/EVEN* pin is a "0", the first line of the cursor is displayed on scan line 0. Every alternate active cursor line in the cursor RAM array relative to the first active cursor line in the even field corresponds to subsequent scan lines in the even field. If the ODD/EVEN* pin is a "1", the second active cursor line in the cursor RAM array is displayed on scan line 1. Each subsequent scan line displayed in the odd field corresponds to alternate cursor lines in the cursor RAM array relative to the first active cursor line in the odd field.

If bit CR23=0, the cursor must be displayed in a non-interlaced system. Scan lines displayed in a frame correspond to sequential cursor lines in the cursor RAM relative to the first active cursor line in the frame. Figure 4 explains planar pixel format and cursor RAM array pixel mapping.

Cursor Color Support

The cursor has three modes for color selection. CR21 and CR20 determine which cursor mode is used. Mode 1 is a three-color cursor, mode 2 is a PM/Window cursor, and mode 3 is an X-Windows cursor (Table 8).

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OPERATING MODES

Highlight Logic

The highlight logic is enabled in cursor mode 2 when both plane data (plane 1 and plane 0) are "1"s. When enabled, highlight logic ensures a unique color to the highlighted pixel because the highlight logic bit-wise complements the 24- or 18-bit palette or by-pass data supplied to the DACs (Table 8).

Video Generation

The CSYNC* and CBLANK* inputs are latched on the rising edge of LCLK to maintain synchronization with the color data. They add appropriately-weighted currents to the analog outputs and produce specific output levels for video applications (Figures 5 and 6).

CR05 specifies whether a 0 IRE or a 7.5 IRE blanking pedestal is to be used. Bits CR02, CR03, and CR04 specify whether the RGB outputs contain sync information. Tables 9 and 10 detail how the CSYNC* and CBLANK* inputs modify the output levels.

SENSE* Output

SENSE* is a "0" if one or more of the IOR, IOG, or IOB outputs exceed the internal voltage reference level of the SENSE* comparator circuit. This output is used to determine the presence of a CRT monitor. With diagnostic code, the difference between a loaded or unloaded RGB line can be discerned.

The reference is generated by a voltage divider from the external 1.235V voltage reference on the V_{REF} pin. For the proper operation of the SENSE* circuit, the following levels should be applied to the comparator by the IOR, IOG, and IOB outputs:

- DAC low voltage equal to or less than 310mV
- DAC high voltage equal to or greater than 430mV

There is an additional ±3% tolerance on the above levels when the internal voltage reference is used. If CSYNC* is a "0", SENSE* is stable. The SENSE* output can drive only one CMOS load.

Mode	Function	MSB							LSB
Pixel Mask Register	Register Bits	7	6	5	4	3	2	1	0
VGA Data	Palette Index	7	6	5	4	3	2	1	0
4 Bits Per Pixel	Palette Index	x	x	x	x	3	2	1	0
8 Bits Per Pixel	Palette Index	7	6	5	4	3	2	1	0
16 Bits Per Pixel	Red Palette Index	x	x	x	4	3	2	1	0
5:5:5 Format	Green Palette Index	x	x	x	4	3	2	1	0
CONTIGUOUS	Blue Palette Index	x	x	x	4	3	2	1	0
16 Bits Per Pixel	Red Palette Index	7	6	5	4	3	x	x	x
5:5:5 Format	Green Palette Index	7	6	5	4	3	x	x	x
SPARSE	Blue Palette Index	7	6	5	4	3	x	x	x
16 Bits Per Pixel	Red Palette Index	x	x	x	4	3	2	1	0
5:6:5 Format	Green Palette Index	x	x	5	4	3	2	1	0
CONTIGUOUS	Blue Palette Index	x	x	x	4	3	2	1	0
16 Bits Per Pixel	Red Palette Index	7	6	5	4	3	x	x	x
5:6:5 Format	Green Palette Index	7	6	5	4	3	2	x	x
SPARSE	Blue Palette Index	7	6	5	4	3	x	x	x
24 Bits Per Pixel	Red Palette Index	7	6	5	4	3	2	1	0
8:8:8	Green Palette Index	7	6	5	4	3	2	1	0
	Blue Palette Index	7	6	5	4	3	2	1	0

Table 7: Pixel Index Masking

OPERATING MODES

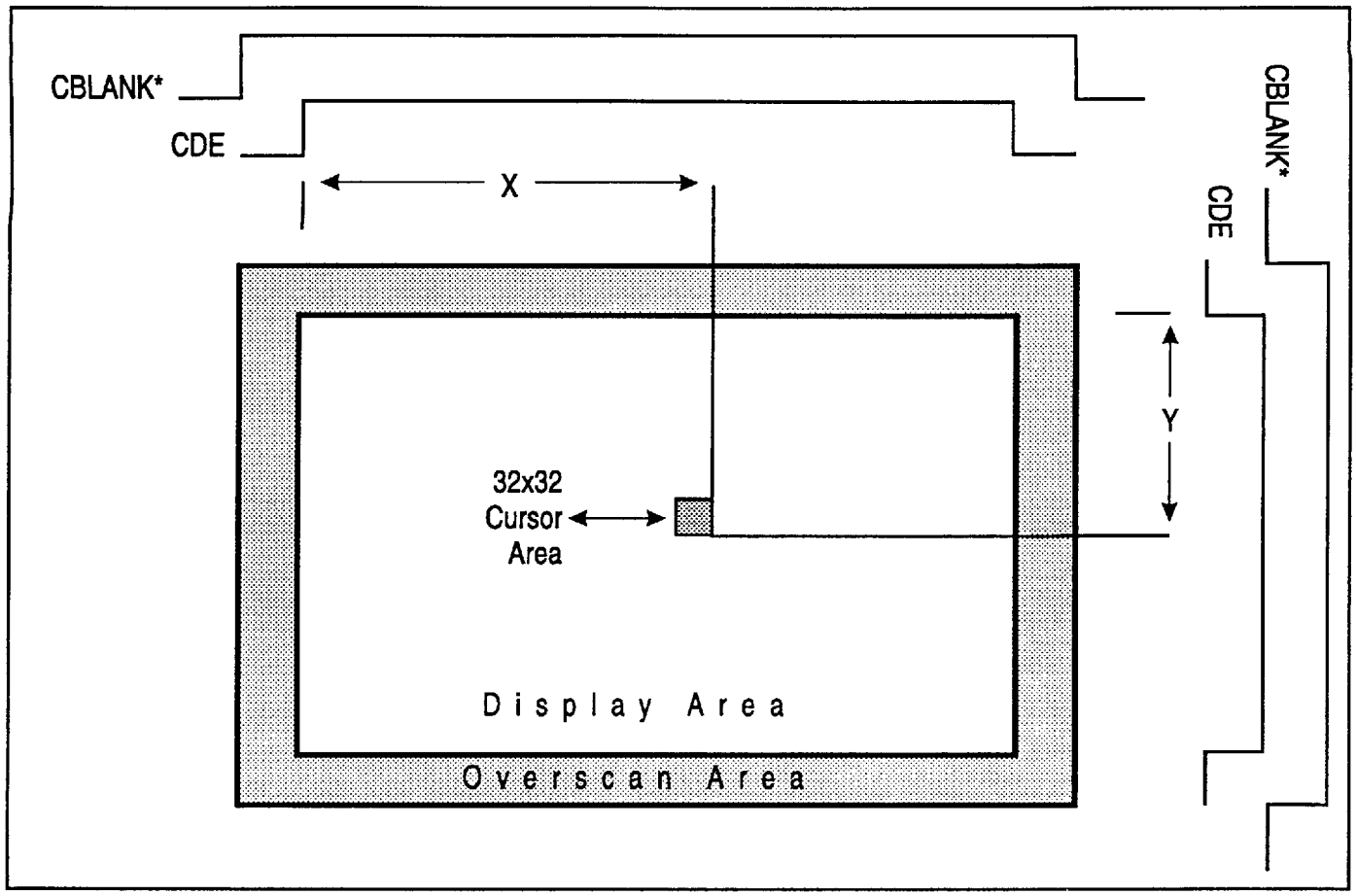

Figure 3: Cursor Positioning

Plane 1	Plane 0	Mode 1	Mode 2	Mode 3
0	0	Palette/By-Pass Data	Cursor Color 1	Palette/By-Pass Data
0	1	Cursor Color 1	Cursor Color 2	Palette/By-Pass Data
1	0	Cursor Color 2	Palette/By-Pass Data	Cursor Color 1
1	1	Cursor Color 3	Palette/By-Pass Data Complement	Cursor Color 2

Table 8: Cursor Color Modes

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OPERATING MODES

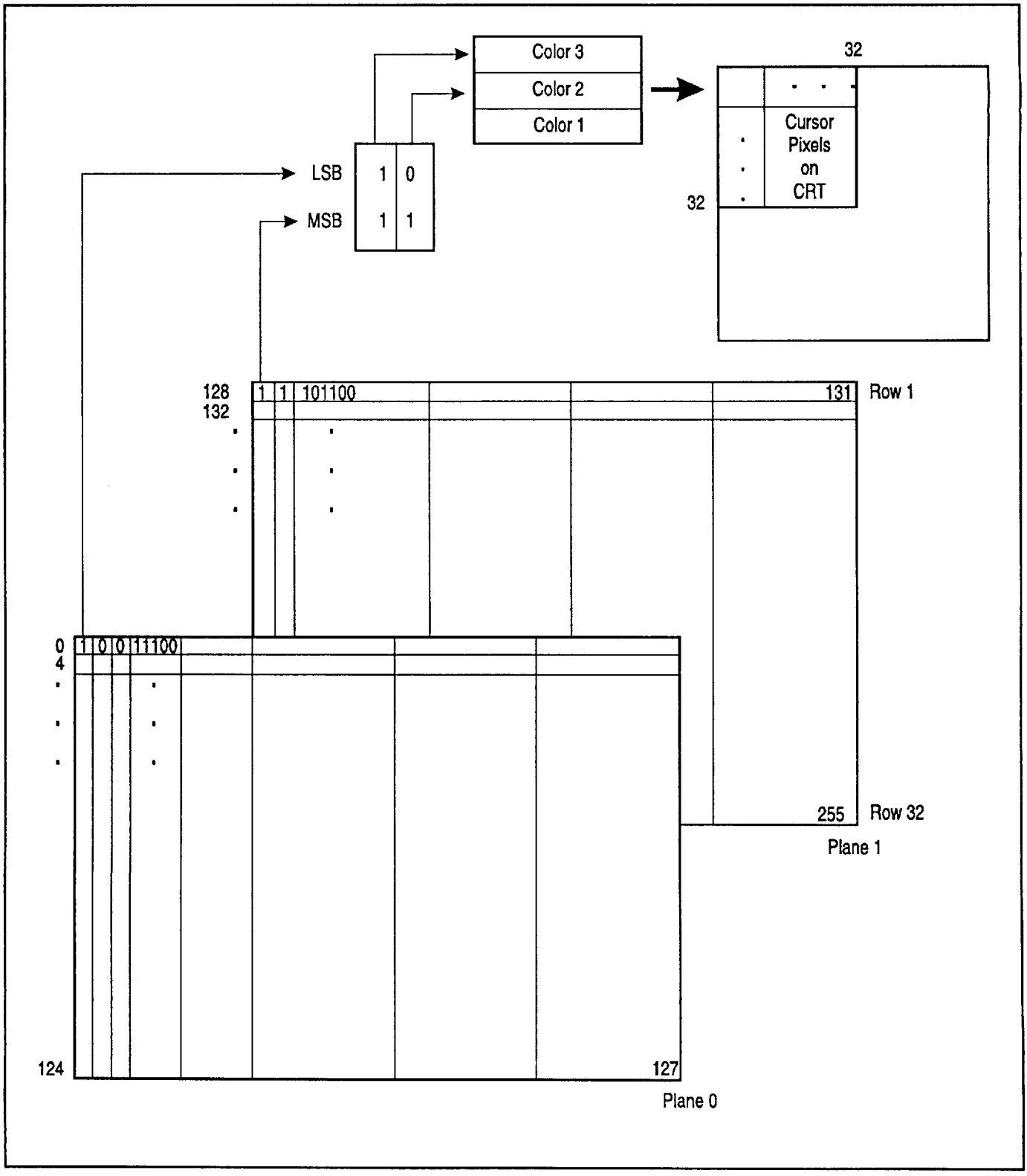
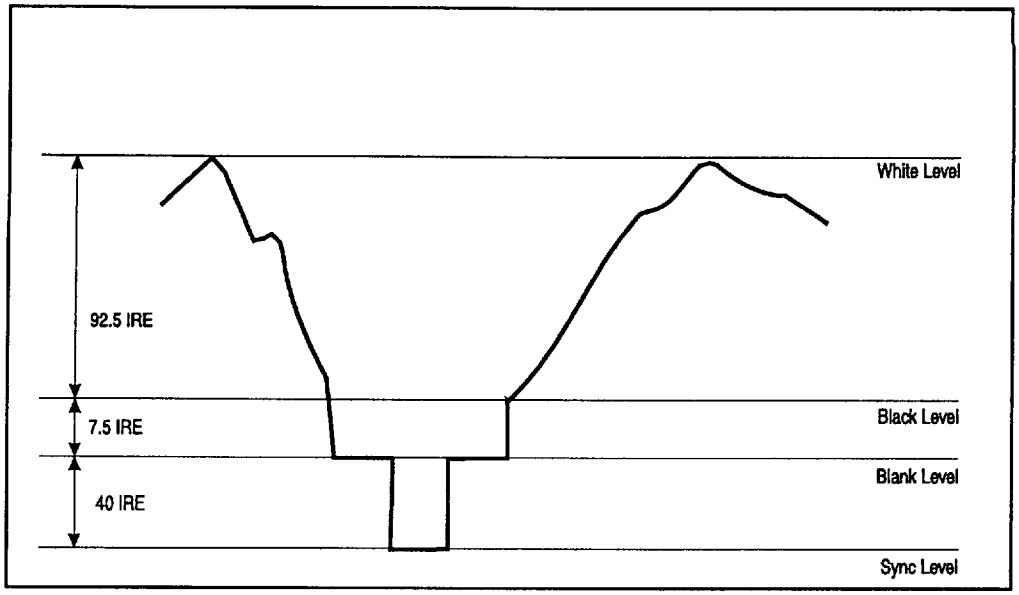


Figure 4: Planar Pixel Format And Cursor RAM Array Pixel Mapping

OPERATING MODES

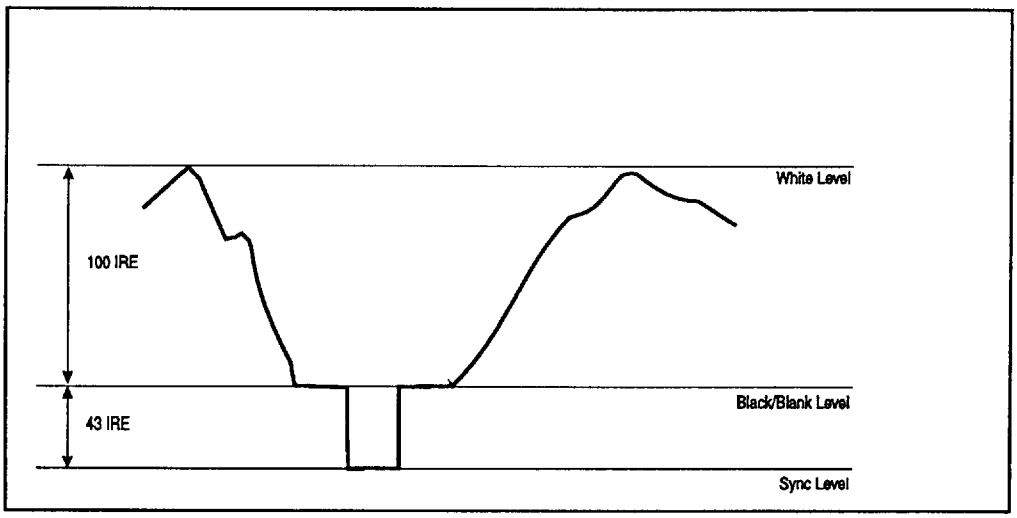
No Sync		Sync	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



75Ω doubly-terminated load, V_{REF} = 1.235V, and RESET ~ 147Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 5: Composite Video Output Waveforms (SETUP = 7.5 IRE)

No Sync		Sync	
mA	V	mA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



75Ω doubly-terminated load, V_{REF} = 1.235V, and RESET ~ 147Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 6: Composite Video Output Waveforms (SETUP = 0 IRE)

Description	Sync Enabled I_{out} (mA)	Sync Disabled I_{out} (mA)	CSYNC*	CBLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
BLACK	9.05	1.44	1	1	$00
DATA	data +9.05	data + 1.44	1	1	data
SYNC	0	0	0	0	$xx
DATA-SYNC	data +1.44	data + 1.44	0	1	data
BLACK-SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx

75Ω doubly-terminated load, V_{REF} = 1.235V, and RESET ~ 147Ω.

Table 9: Video Output Truth Table (SETUP = 7.5 IRE)

Description	Sync Enabled I_{out} (mA)	Sync Disabled I_{out} (mA)	CSYNC*	CBLANK*	DAC Input Data
WHITE	25.24	17.62	1	1	$FF
BLACK	7.62	0	1	1	$00
DATA	data+7.62	data	1	1	data
SYNC	0	0	0	0	$xx
DATA-SYNC	data	data	0	1	data
BLACK-SYNC	0	0	0	1	$00
BLANK	7.62	0	1	0	$xx

75Ω doubly-terminated load, V_{REF} = 1.235V, and RESET ~ 147Ω.

Table 10: Video Output Truth Table (SETUP = 0 IRE)

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INTERNAL REGISTERS

Bit	Function/Selection	Command Register 0 Comments
CR00	Power-Down Enable (0) Normal Operation (1) Power-Down Operation	In power-down mode the DACs and power to the RAM are turned off. The RAM retains the data, and CPU reads and writes occur with no loss of data
CR01	DAC 6-Bit/8-Bit Resolution (0) 6-Bit Operation (1) 8-Bit Operation	Specifies whether the microprocessor is reading and writing 6-bit or 8-bit color data
CR02	Red Sync Enable (0) Disable Sync (1) Enable Sync	Specifies whether IOR outputs should contain sync information
CR03	Green Sync Enable (0) Disable Sync (1) Enable Sync	Specifies whether IOG outputs should contain sync information
CR04	Blue Sync Enable (0) Disable Sync (1) Enable Sync	Specifies whether IOB outputs should contain sync information
CR05	Setup enable (0) Disable SETUP (0 IRE) (1) Enable SETUP (7.5 IRE)	Determines the video blanking pedestal
CR06	Clock Disabled ANDed with CR00 (0) Normal Operation (1) Disabled Internal Clocking	When this bit and CR00 are a "1", the internal clock is disabled for additional power conservation in power-down mode. RAM still retains the data; the MPU reads and writes can occur without loss of data. When this bit is a "0", internal clocking is enabled
CR07	Reserved ("0")	Reserved

This register may be written to or read by the microprocessor at any time and is not initialized at power-up. CR00 corresponds to data bus bit D0, the LSB.

Table 11: Command Register 0

Bit	Function/Selection	Command Register 1 Comments
CR10	16-Bit Per Pixel Port Switch Control (0) Multiplex Port [B-A] (1) Multiplex Port [D-C]	Specifies a 16-bit word for either 5:5:5 color format (CR11=0) when CR16=01, CR15=01, CR12=1, and CR11=0; or for 5:6:5 color format (CR11=1) when CR16=01, CR15=01, and CR12=1. This bit is ignored when real-time port switching is enabled.
CR11	16-Bit Real-Time Switch Enable (0) CR10 Controls Selection (1) P7D Controls Selection	Only valid if CR13=0 and CR12=1. When this bit is a "0", CR10 switches the ports multiplexed. When this bit is a "1", pixel port bit P7D switches the ports multiplexed. This bit is ignored when 5:6:5 RGB color format is selected
CR12	16-Bit Multiplexing Rate (0) 2:1 Multiplexing (1) 1:1 Multiplexing	When this bit is a "0" and CR15=1 and CR16=0, two 16-bit values are latched in during every LCLK cycle. Under the same conditions, when this bit is a "1", one 16-bit value is output per LCLK cycle. This bit is ignored if CR15 and CR16 specify 4-bit, 8-bit, or 24-bit per pixel operation
CR13	16-Bit RGB Color Format (0) 5:5:5 R:G:B Color Format (1) 5:6:5 R:G:B Color Format	Selects the RGB color format for 16-bits per pixel operation
CR14	True Color By-Pass Enable (0) Pixel Addresses Palette (1) Pixel By-Passes Palette	When this bit is "0", the pixel palette is addressed by the pixel data. When "1", the RGB pixel data by-passes the color palette and drives the DACs directly. True-color by-passing is available only for pixel sizes of 16 and 24-bits
CR16, CR15	Bit-Per-Pixel Selection (00) One 24-Bit Pixel (01) One or Two 16-Bit Pixels (10) Four 8-Bit Pixels (11) Eight 4-Bit Pixels	Select the pixel size depth and determine the multiplexing rates for 4, 8, and 24-bits per pixel operation. The 16-bit per pixel multiplexing rate is set by the state of CR12
CR17	Reserved ("0")	Reserved for future expansion. A "0" must be written to ensure proper operation

This register may be written to or read by the microprocessor at any time and is not initialized at power-up. CR10 corresponds to data bus bit D0, the LSB.

Table 12: Command Register 1

INTERNAL REGISTERS

Bit	Function/Selection	Command Register 2 Comments
CR21, CR20	Cursor Mode Selection (00) Cursor Disabled (01) Three Color Cursor (10) Two Color/Highlight Cursor (11) Two Color/X-Windows Cursor	Set the functionality of ther 32x32x2 cursor
CR22	16-Bit Per Pixel Palette Index Selection (0) SPARSE Indexing (1) CONTIGUOUS Indexing	When CR22=0, the RGB color components pixel data is mapped to the MSBs of the RGB palette address. If CR22=1, RGB color component pixel data is mapped to the LSBs of the palette address. The least and most significant bits (respectively) of the address are set to zero
CR23	Display Mode Selection (0) Non-Interlaced (1) Interlaced	The mode must be set properly to ensure proper operation of the internal cursor
CR24	CLKSEL Enable (0) PCLK0 Selected (1) PCLK1 Selected	To eliminate glitches on the SCLK output, switching between PCLKs should occur only when the multiplexing rate is 8:1 or 4:1. To ensure the integrity of the palette, the device should be put into power-down mode before switching clocks
CR25	PORTSEL Mask (0) Masked (VGA Port) (1) NoN-Masked (VGA or Pixel Port)	Determines the selection of the input port. It is logically ANDed with the PORTSEL pin
CR26	Test Path Enable (0) Normal Operation (1) Test Path Enabled	A "1" enables certain internal test paths to be set up, and pixel data is accessible on the MPU data bus. This involves any input mode and any inputs which affect access to the color palette RAM. If CR26 is enabled, the device will not operate at speed
CR27	SCLK Disabled (0) SCLK Enabled (1) SCLK Disabled	CR27 must equal a "0" to enable SCLK to be output. A "1" tri-states the output

This register may be written to or read by the microprocessor at any time and is not initialized at power-up. CR20 corresponds to data bus bit D0, the LSB.

Table 13: Command Register 2

Bit	Function/Selection	Status Register Comments
SR1, SR0	Address [a,b] State (00) Red Color Component (01) Green Color Component (10) Blue Color Component	When read, these bits reflect the color component address for the next RD*/WR* cycle when accessing the palette, cursor color registers, or overscan register
SR2	Read/Write Access Status (0) Write Cycle (1) Read Cycle	Provides RD/WR status when the register select bits equal $0, $3, $4, or $7. When address register $0 or $4 has been written, the device is in the write mode and this bit is a "0". When address register $3 or $7 has been written, the device is in the read mode and this bit is a "1"
SR3	The SENSE* bit	If a "0", one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (370mV). This bit determines the presence of a CRT monitor. With the diagnostic code, the difference between a loaded or unloaded RGB line can be discerned.
SR5, SR4	Revision Values (always "00")	
SR7, SR6	Identification Values SR7=0 SR6=1	

The 8-bit status register monitors and identifies certain devices. It may be read by the microprocessor at any time; write cycles to this register are ignored. D0 is the LSB corresponding to SR0. This register is not reset during power-up or reset.

Table 14: Status Register

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	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit X Address	D3 X11	D2 X10	D1 X0	D0 X8	D7 X7	D6 X6	D5 X5	D4 X4	D3 X3	D2 X2	D1 X1	D0 X0
	Cursor (y) High (CYHR)				**Cursor (y) Low (CYLR)**							
Data Bit Y Address	D3 X11	D2 X10	D1 X0	D0 X8	D7 X7	D6 X6	D5 X5	D4 X4	D3 X3	D2 X2	D1 X1	D0 X0

Table 15: Cursor (x,y) Registers

INTERNAL REGISTERS

This section describes the internal registers of the KDA0484 in detail. Command registers are discussed in detail in Tables 11 through 15. Refer to Table 16 for the RS values associated with each register. All command register bits are set to "0" when a low signal is asserted on the RESET* pin.

The Status Register

The status register can be accessed by writing 0000 0000 to the address register.

The status register (Table 14) cannot be written to. The 8-bit status register monitors and identifies certain devices. It may be read by the microprocessor at any time.

Cursor (x,y) Registers

These registers are used to specify the (x,y) coordinate of the 32x32x2 hardware cursor (Table 15). The cursor (x) register contains the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR). The cursor (y) register contains the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). The last value written to these registers is the value returned on a read. These registers may be written to or read from.

CXLR and CXHR cascade to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR cascade to form a 12-bit cursor (y) register. Bits D4-D7 are always "0". 32x32x2 cursor hardware:

Xp = desired display screen (x) position + 32 (or $0020)

Yp = desired display screen (y) position + 32 (or $0020)

Where the (x) or (y) reference points for the display screen, x = 0 or y = 0, is the upper left corner of the screen. The Xp or Yp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 (or $0FFF) may be written into the cursor (x) or (y) register. If Xp = 0 or Yp = 0, the cursor will be entirely off the screen (see Cursor Operation).

Pixel Read Mask Register

This register may be written to or read by the microprocessor at any time and is not initialized at power-up. D0 is the LSB. The register contents are bit-wise ANDed with the pixel data prior to addressing the color palette RAM. This register must be initialized to "1".

INTERNAL REGISTERS & PIN DESCRIPTION

Register	RS3-RS0
CR0	0110
CR1	1000
CR2	1001
CR3	1010
Pixel Read Mask	0010
Status	1010
Cursor X High	1101
Cursor X Low	1100
Cursor Y High	1111
Cursor Y Low	1110

Table 16: Internal Registers And Corresponding RS Values

PIN DESCRIPTION

<table>
<tr><th>Name</th><th>#</th><th>Description</th><th>Comments</th></tr>
<tr><td>CBLANK*</td><td>65</td><td>Composite Blank Control Input (TTL Compatible)</td><td>A "0" drives the analog outputs to the blanking level. CBLANK* is latched on the rising edge of LCLK. When BLANK* is a "0", the pixel inputs are ignored. The falling edge of this signal determines the polarity of the CSYNC* input pin. The on-board cursor positioning counters are referenced to this signal.</td></tr>
<tr><td>CDE</td><td>63</td><td>Composite Display Enable Control Input (TTL Compatible)</td><td>The state of this signal and CBLANK* determines whether the analog outputs are blanked or contain cursor color, pixel, or overscan data. This signal is latched on the rising edge of LCLK. If overscanning is not used, this pin should be tied to CBLANK*. The following is a list of combinations of CDE and CBLANK*:
<table>
<tr><th>PORTSEL* CR25</th><th>CDE</th><th>CBLANK*</th><th></th></tr>
<tr><td>x</td><td>x</td><td>0</td><td>Video blanking</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>VGA pixel data</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Cursor color or VGA data</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Overscan data</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Cursor color or pixel data</td></tr>
</table></td></tr>
<tr><td>COMP</td><td>41</td><td>Compensation Pin</td><td>A 0.1µF ceramic capacitor must be used to by-pass this pin to V_{AA}. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. (Please see PC Board Layout).</td></tr>
<tr><td>CSYNC*</td><td>64</td><td>Composite Sync Control Input (TTL compatible)</td><td>The polarity of this pin is determined before the falling edge of CBLANK*. A "0" switches off a 40 IRE current source on the analog outputs if enabled by CR01 - CR02 (Figures 5 and 6). CSYNC* does not override any other control or date input. It should be asserted only during the blanking interval. It is latched on the rising edge of LCLK. If sync information is not to be generated, this pin should be connected to GND. (Tables 9 and 10)</td></tr>
<tr><td>D0-D7</td><td>54-61</td><td>Data Bus (TTL Compatible)</td><td>Data is transferred into and out of the device over this 8-bit bi-directional data bus. D0 is the LSB.</td></tr>
</table>

Table 17: Pin Descriptions

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PIN DESCRIPTION

Name	#	Description	Comments
FS_{ADJUST}	33	Full-Scale Adjust Control	The IRE relationships in Figures 5 and 6 are maintained, regardless of the full-scale output current. With an external or the internal voltage reference is used, a resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal (Figures 11 and 12). The relationship between R_{SET} and the full-scale output current on each output is: R_{SET} (Ω) = K * 1,000 * V_{REF} (V)/I_{OUT}(mA) K is defined in the table below. It is recommended that a 147Ω R_{SET} resistor be used for doubly-terminated 75Ω loads.
GND	34,36, 38, 80, 82, 84	Analog Ground	All GND pins must be connected together on the same analog power plane
IOR, IOG, IOB	35, 37, 39	Red, Green, and Blue Current Outputs	These high-impedance current sources can directly drive a doubly-terminated 75Ω coaxial cable.
LCLK	81	Latch Clock Input (TTL Vompatible)	The rising edge of this signal latches P7:0 (A-D) or VGA [7:0], and CBLANK*, CDE, CSYNC*, and PORTSEL. The information latched by this signal is synchronized internally with SCLK. Because of this synchronization process, there is a timing window on both sides of SCLK where LCLK must not rise (Figure 9). This timing window is necessary so that data latched by LCLK does not interfere with the setup and hold times required by the internal synchronizing latch. Data is synchronized with the selected pixel clock once internally latched with SCLK. If the MUX rate is 8:1, 4:1, 2:1 or 1:1, this signal is equal to the selected pixel clock divided by 8, 4, 2, 1, or 1, respectively.
ODD/EVEN*	62	ODD/EVEN* Field Input (TTL Compatible)	This signal should be changed only during vertical blank. This input is used to ensure proper operation of the on-board cursor when interlaced operation is selected. When this signal is a "0", an even field is specified. When this signal is a "1", and odd field is specified. This input is ignored if non-interlaced operation is selected.
P7:0 (A-D)	1-32	Pixel Port Inputs (TTL Compatible)	This port is selected if PORTSEL is a "1". The appropriate pins on this port are multiplexed at rates of either 1:1, 2:1, 4:1, or 8:1, depending on the operating mode selected. This port is latched on the rising edge of LCLK. P0 is the LSB. Unused inputs should be connected to GND
PCLK0	78	Pixel Clock 0 Input (TTL Compatible)	This clock is selected when CR24 in command register 2 is a "0". The signal on this pin should be the VGA pixel clock. This clock should be specified when switching between the pixel and VGA ports on a pixel-by-pixel basis (in 1:1 mode only). It is recommended that all clock inputs be driven by a dedicated buffer to avoid reflection-induced jitter.
PCLK1	76	Pixel Clock 1 Input (TTL Compatible)	This clock is selected when CR24 in command register 2 is a "1". This input pin may also be used as a differential clock input by setting CR34 to 1. The signal on this pin is typically the high-speed pixel clock used during multiplexed operation of the pixel port.
PORTSEL	66	VGA/Pixel Port Select Input (TTL Compatible)	This pin is ANDed with control register bit CR25 to determine whether the pixel port or VGA port is selected. A "0" on this pin selects the VGA port, regardless of the state of CR25. A "1" selects the pixel port if CR25=1. If a 1:1 MUX rate has been specified, this pin may be used to switch between the pixel and VGA ports on a pixel-by-pixel basis. This switching cannot be done in 2:1, 4:1, or 8:1 MUX modes. This pin should not be left floating.

	Sync Enabled		Sync Disabled	
Setup	0 IRE	7.5 IRE	0 IRE	7.5 IRE
K (8 bits)	2.88	3.055	2.045	2.207
K (6 bits)	2.867	3.029	2.021	2.183

Table 17: Pin Descriptions (continued)

PIN DESCRIPTION

Name	#	Description	Comments
RD*	49	Read Control Input (TTL Compatible)	To read data from the device, RD* must be a "0". RS0-RS3 are latched on the falling edge of RD* during read operations. RD* and WR* should not be asserted simultaneously.
RESET*	47	Reset Input (TTL Compatible)	When this signal is low, all command register bits are set to zero and the device is in VGA mode. The pixel read mask register is not initialized on reset and must be initialized by the user to "1"s for proper operation.
RS0-RS3	50-53	Register Select Inputs (TTL Compatible)	RS0-RS3 specify the type of read or write operation being performed. (Tables 1 and 2)
SENSE*	46	Comparator Sense Output (CMOS Compatible)	This pin will be low if one or more of the IOR, IOG, and IOB analog output levels exceed the internal comparator reference levels. The sense output can drive only one CMOS load
SCLK	83	VRAM/WRAM Shift Clock Output (TTL Compatible)	The signal on this pin is equal to the selected pixel clock divided by 8, 4, 2 or 1, depending on the operating mode selected.
V_{AA}	40, 42, 45, 75, 77, 79	Analog Power	All V_{AA} pins must be connected together on the same analog power plane
VGA[7:0]	67-74	VGA Port Inputs (TTL Compatible)	This port is selected if PORTSEL is a "0". This port is multiplexed 1:1. This port is latched on the rising edge of LCLK. P0 is the LSB. Unused inputs should be connected to GND.
VREF OUT	44	Voltage Reference Output	This output provides a 1.235V (typical reference and may be connected directly to the V_{REF} pin. If the on-board reference is not used, this pin may be left floating. Up to four KDA0484s can be driven by this output. (Figures 11 and 12)
VREF IN	43	Voltage Reference Input	If an external voltage reference is used, it must supply this input with a 1.235V (typical) reference. A 0.1µF ceramic capacitor must be used to decouple this input to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When the internal reference is used, this pin should not drive any external circuitry, except the decoupling capacitor. (Figures 11 and 12)
WR*	48	Write Control Input (TTL Compatible)	D0-D7 data is latched on the rising edge of WR*. RS0-RS3 are latched on the falling edge of WR* during write operations. RD* and WR* should not be asserted simultaneously.

Table 17: Pin Descriptions (continued)

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PIN DESCRIPTION

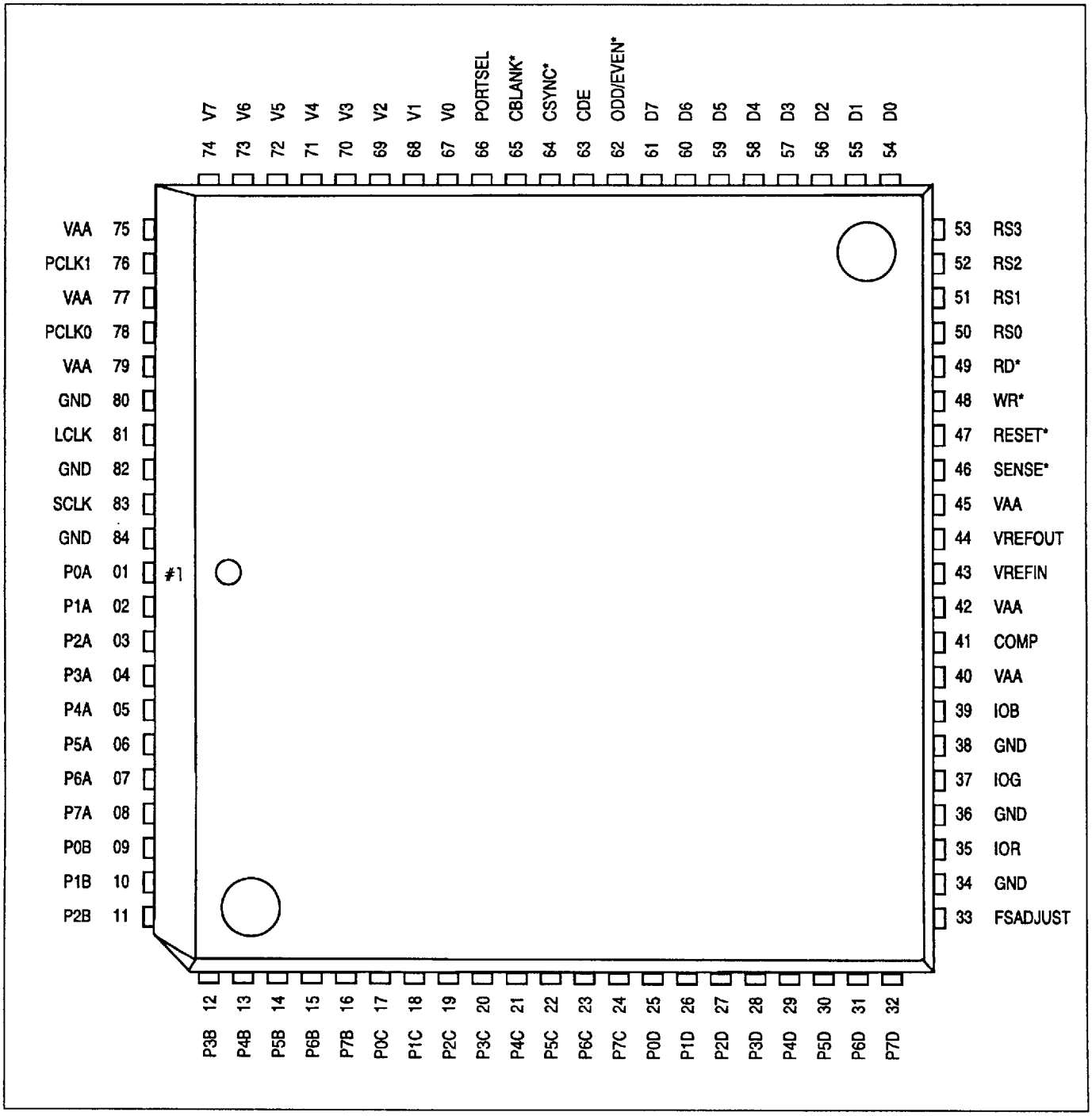

Figure 7: KDA0484 Pin Description Diagram (Top View)

DC CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units
Resolution (Each DAC)		8	8	8	Bits
Accuracy (Each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% gray scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	V_{IH}	2.0		V_{AA} +0.5	V
Input Low Voltage	V_{IL}	GND-0.5		0.8	V
Input High Current (V_{IN} = 2.4V)	I_{IH}			1	µA
Input Low Current (V_{IN} = 0.4V)	I_{IL}			-1	µA
Input Capacitance (f = 1MHz; V_{IN}= 2.4V)	C_{IN}			7	pF
Digital Outputs					
Output High Voltage (I_{OH} = -400µA)	V_{OH}	2.4			V
Output Low Voltage (I_{OL} = 3.2mA)	V_{OL}			0.4	V
Tri-State Current	I_{OZ}			50	µA
Output Capacitance	CD_{OUT}			7	pF
Analog Outputs					
Grey-Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative To Black		16.74	17.62	18.50	mA
Black Level Relative To Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
BLANK Level		6.29	7.62	8.96	mA
SYNC Level		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	V_{OC}	-0.2		+1.5	V
Output Impedance	RA_{OUT}		10		kΩ
Output Capacitance	CA_{OUT}			30	pF
(F = 1MHz, I_{OUT} = 0mA)					
V_{REF}	V_{REFOUT}	1.103	1.225	1.348	V
Voltage Reference Input Current	I_{VRIN}		1.4		µA
Power Supply Rejection Ratio	PSRR			0.5	% / % ΔV_{AA}
(COMP = 0.1µF; f= 1KHz)					

Test conditions to generate RS-343A standard video signals (unless otherwise specified); "Recommended Operating Conditions" with external voltage reference, SETUP=7.5 IRE, R_{SET}=147Ω, and V_{REF}=1.235V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature (room) and nominal voltage (5V).

When the internal reference is used, R_{SET} may require adjustment to meet these limits. Also, the gray scale output current (white level relative to black) will have a typical tolerance of ±3%, rather than the ±5% specified above.

In 6-bit mode, the output levels are approximately 1.5% lower than these values

Table 18: DC Characteristics

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AC CHARACTERISTICS

		85MHz			75MHz			
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
PCLK 0, PCLK 1 (clock doubled)	F_{max}			85			75	MHz
V_{AA} Supply Current (*Note 1*)	I_{AA}							
Normal Operation			260	330		260	330	mA
Power-down Mode (*Note 2*)			TBD	TBD		TBD	TBD	mA
LCLK Rate (Figure 9 and 10)	L_{max}							
0485 1:1 MUX				10.63			9.38	MHz
0486 4:3 MUX				21.25			18.75	MHz
0486 4:1 MUX				42.50			37.50	MHz
0486 2:1 MUX				85			75	MHz
SCLK Rate	S_{max}							
0485 1:1 MUX				10.63			9.38	MHz
0486 4:3 MUX				21.25			18.75	MHz
0486 4:1 MUX				42.50			37.50	MHz
0486 2:1 MUX				50.35			50.35	MHz
RS0-RS3 Setup Time (Figure 8)	1	10			10			ns
RSO-RS3 Hold Time	2	10			10			ns
RD* Asserted to D0-D7 Driven	3	2			2			ns
RD* Asserted to D0-D7 Valid	4			40			40	ns
RD* Negated to D0-D7 Tri-Stated	5			20			20	ns
Read D0-D7 Hold Time	6	2			2			ns
Write D0-D7 Setup Time	7	10			10			ns
Write D0-D7 Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*pclk			6*pclk			ns
PCLK0, PCLK 1 Cycle Time	11	11.77			13.33			ns
All MUX rates								
PCLK0, PCLK 1 Pulse Width High	12	5			5			ns
All MUX rates								
PCLK0, PCLK 1 Pulse Width Low	13	4			4			ns
All MUX rates								
LCLK Cycle Time	14							
8:1 MUX		94.12			106.61			ns
4:1 MUX		47.06			53.33			ns
2:1 MUX		23.53			26.67			ns
1:1 MUX or VGA		11.77			13.33			ns
LCLK Pulse Width High	15							
8:1 MUX		5			5			ns
4:1 MUX		5			5			ns
2:1 MUX		5			5			ns
1:1 MUX or VGA		5			5			ns
SCLK Pulse Width Low	16							
8:1 MUX		4			4			ns
4:1 MUX		4			4			ns
2:1 MUX		4			4			ns
1:1 MUX or VGA		4			4			ns
SCLK Cycle Time	17							
8:1 MUX		94.12			106.67			ns
4:1 MUX		47.06			53.33			ns
2:1 MUX		23.53			26.67			ns
1:1 MUX		19.86			19.86			ns

Table 19: AC Characteristics

AC CHARACTERISTICS

		85MHz			75MHz			
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
Data Setup to LCLK P7:0 (A-D), VGA (7:0), CDE, CBLANK*, CSYNC*, PORTSEL	18	1			1			ns
Data Hold from LCLK P7:0 (A-D), VGA (7:0), CDE, CBLANK*, CSYNC*, PORTSEL	19	5			5			ns
LCLK (*Note 3*) (valid skew with respect to SCLK)	20	-3		T-14	-3		T-14	ns
SCLK Output Delay (1:1 mode)	21		6	11		6	11	ns
SCLK Output Delay (MUX mode)			10	20		10	20	ns
Analog Output Delay	22			30			30	ns
Analog Output Rise & Fall Time	23		3			3		ns
Analog Output Settling Time (*Note 4*)	24		13			13		ns
Clock & Data Feedthrough (*Note 4*)			-30			-30		dB
Glitch Impulse (*Note 4*)			75			75		pV-second
SENSE* Output Delay	25		1			1		µs
DAC-to-DAC Cross-Talk			-23			-23		dB
Analog Output Skew				2			2	ns

Note 1: At 75MHz. I_{AA} (typ.) at V_{AA}=5.0V, 25°C. I_{AA} (max.) at V_{AA}=5.25V, 70°C. 4:1 MUX mode at 40% blanking. Temperature coefficient=0.4mA/°C for decreasing temperatures. The temperature coefficient will increase I_{AA} by 30mA/°C.

Note 2: External voltage reference is disabled during power-down mode, all inputs are low, and clock is running.

Note 3: T=SCLK cycle time.

Note 4: Clock and data feed through is a function of the number of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1KΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feed through. Glitch impulse includes clock and data feedthrough, and -3dB test bandwidth=2x clock rate.

Test conditions (unless otherwise specified); "Recommended Operating Conditions" with external voltage reference with SETUP=7.5 IRE, R_{SET}=147Ω, and V_{REF}=1.235V. TTL input values are 0V to 3V, with input rise/fall times ≤4ns (measured between 10% and 90% points). Timing reference points at 50% for input and outputs. Analog output load ≤10pF; SENSE* and D0-D7 output load ≤50pF. SCLK output load=50pF. See notes for Figures 8 and 12. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature (room) and nominal voltage (5V).

Table 19: AC Characteristics (continued)

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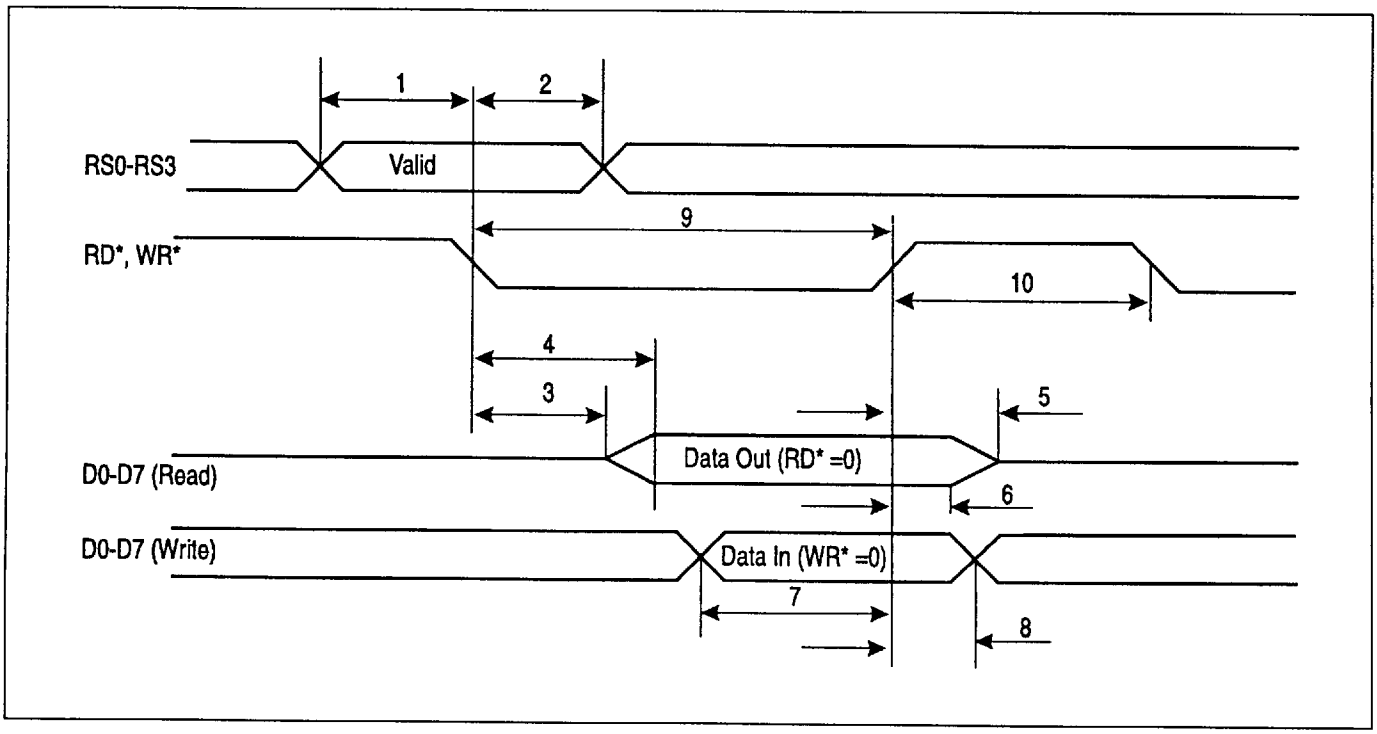
AC CHARACTERISTICS & TIMING DIAGRAMS

Pipeline Delay	Min.	Max.
1:1 VGA Mode (both)	8 LCLKs	8 LCLKs
2:1 Mode (KDA0485)	1 LCLK + 7 PCLKs	1 LCLK + 8 PCLKs
4:1 Mode (KDA0485)	1 LCLK + 7 PCLKs	1 LCLK + 10 PCLKs
8:1 Mode (KDA0485)	1 LCLK + 7 PCLKs	1 LCLK + 14 PCLKs

Pipeline delay (Min.) is the minimum number of clocks to latch in all pixels and output one pixel. Pipeline delay (Max.) is the maximum number of clocks to latch in all pixels and output one pixel. In the 1:1/VGA Mode, LCLK is the primary clock latching and pipelining for the pixels.

Table 20: Pipeline Delay

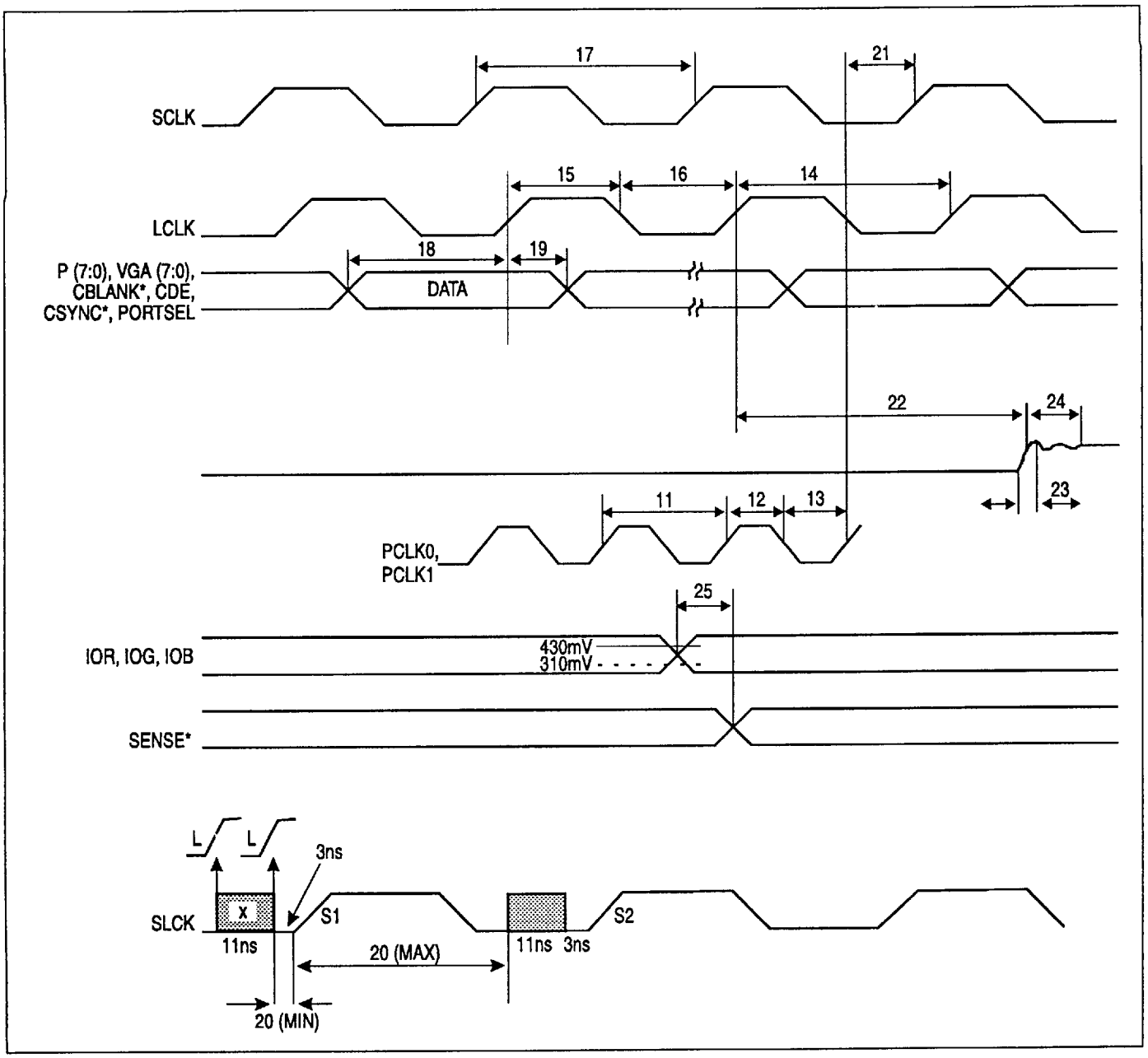
TIMING DIAGRAMS



Output delay is measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition. Settling time is measured from the 50% point of full-scale transition to the output remaining within ±1LSB. Output rise/fall time is measured between the 10% and 90% points of full-scale transition.

Figure 8: MPU Read/Write Timing

TIMING DIAGRAMS



Note 1: Output delay is measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time is measured from the 50% point of full-scale transition to the output remaining within ±1LSB.

Note 3: Output rise/fall time is measured between the 10% and 90% points of full-scale transition.

L = LCLK rising edges

S1 = First SCLK rising edge

S2 = Second SCLK rising edge

If the pixel data latched by LCLK is to be synchronized correctly wit the internal PCLK clock, an LCLK rising edge cannot occur in an invalid window, as illustrated above.

If L occurs within the 11ns invalid region (X), it is not guaranteed on which rising edge of SCLK (S1 or S2) the data will be synchronized. If L occurs before the 11ns invalid region, then the data is guaranteed to by synchronized on S1. If L occurs after the 11ns invalid region, then the data will not be synchronized on S1 and is guaranteed to be synchronized on S2.

Figure 9: Video Input/Output Timing (Non-1:1)

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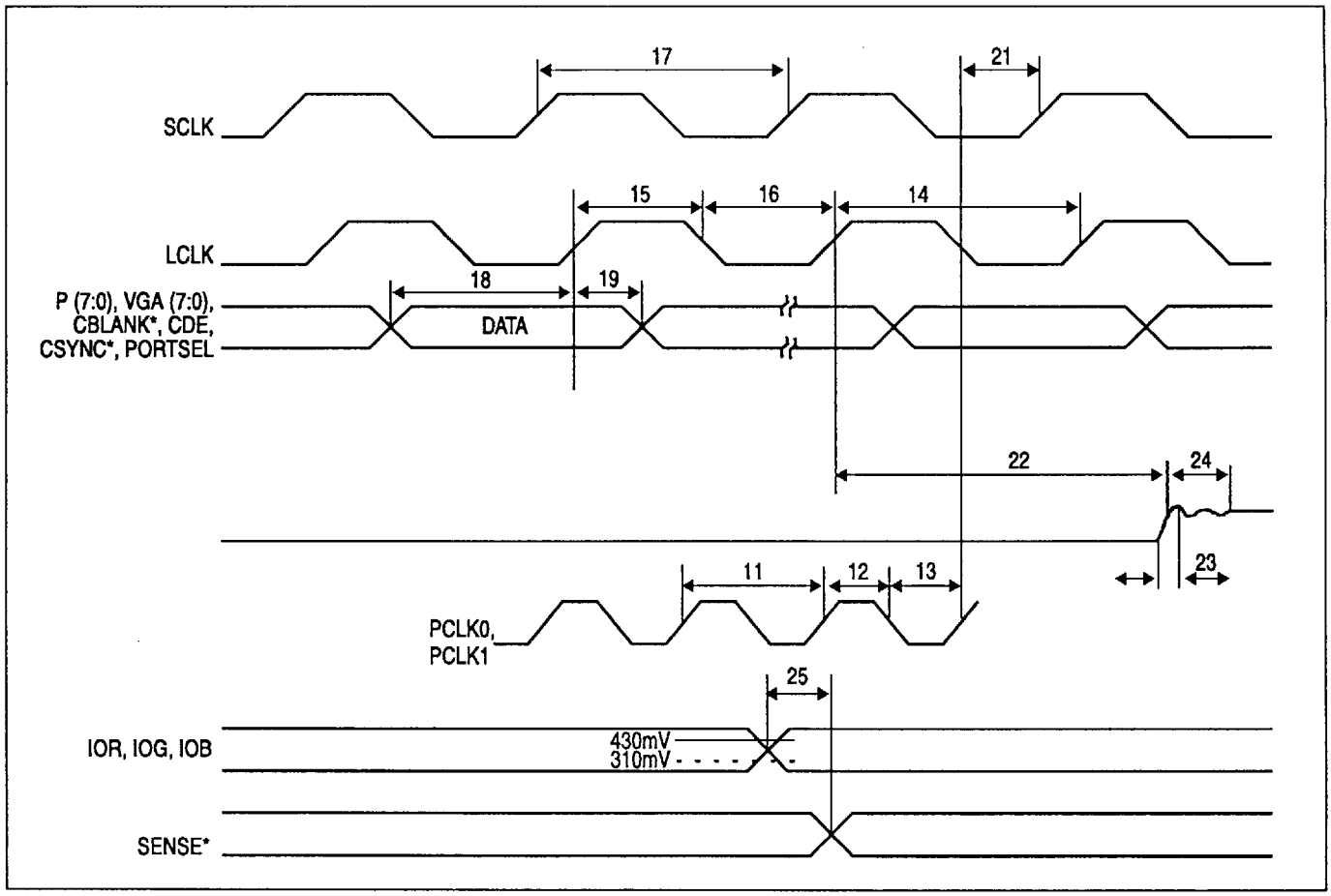
TIMING DIAGRAMS



Output delay is measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition. Settling time is measured from the 50% point of full-scale transition to the output remaining within ±1LSB. Output rise/fall time is measured between the 10% and 90% points of full-scale transition.

Figure 10: Video Input/Output Timing (1:1 MUX Rates)

DESIGNING WITH THE KDA0484

PC Board Considerations

Layout should be optimized for low noise on the KDA0484 power and ground planes by providing good decoupling. The trace length between groups of V_{AA} and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical in eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with the top and bottom layers allocated for signals and the middle two layers for power and ground.

An optimum layout enables the KDA0484 to be located as closely as possible to both the power supply connector and the video output connector.

Power And Ground Plane

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all power pins, V_{REF} circuitry, and COMP and V_{REF} decoupling. There should be at least a one-eighth inch gap between the digital power plane and the analog power plane.

Connect the analog power plane to the digital power plane (V_{CC}) at a single point through a ferrite bead (Figures 11 and 12). Locate this bead within three inches of the KDA0484. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

For optimum performance, a common digital and analog ground plane is recommended. Proper routing of all digital signal traces minimizes radiated noise and cross-talk.

Decoupling

All capacitors should be located as close as possible to the device, using the shortest possible leads (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for hip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1µF ceramic capacitor, decoupling each of the two groups of V_{AA} pins to GND. For operation above 75MHz, a 0.1µF capacitor in parallel with a 0.01µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device V_{AA} and GND pins and connected with short, wide traces.

The 10µF capacitor shown in Figure 5 is for low-frequency power supply ripple; the 0.1µF capacitors are for high-frequency power supply noise rejection. The decoupling capacitors should be connected at the V_{AA} and GND pins, with short, wide traces.

When a linear regulator is used, the power-up sequence must be verified to prevent latch-up. A linear regulator is recommended to filter the analog power supply if the power supply noise is ⊕200mV, or >10LSBs. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About ten percent of the power supply hum, and ripple noise at a frequency less than 1MHz, will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to V_{AA}, typically with a 0.1µF ceramic capacitor. Low frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and V_{AA} pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

Analog Signal Interconnect

Locate the KDA0484 as close as possible to the output connectors to minimize noise pick-up and reflections caused by impedance mismatch.

The analog outputs are susceptible to cross-talk from digital lines; digital traces must not be routed under or adjacent to the analog output traces. To minimize high frequency power supply rejection, the video output signals should not overlay the analog power plane.

For optimum performance, analog video outputs should have a source load resistor value equal to the destination termination (using a clean, isolated ground return path). The load resistor connection between the video outputs and GND should be as close as possible to the KDA0484 to minimize reflections. Unused analog outputs should be connected to GND.

Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length-dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

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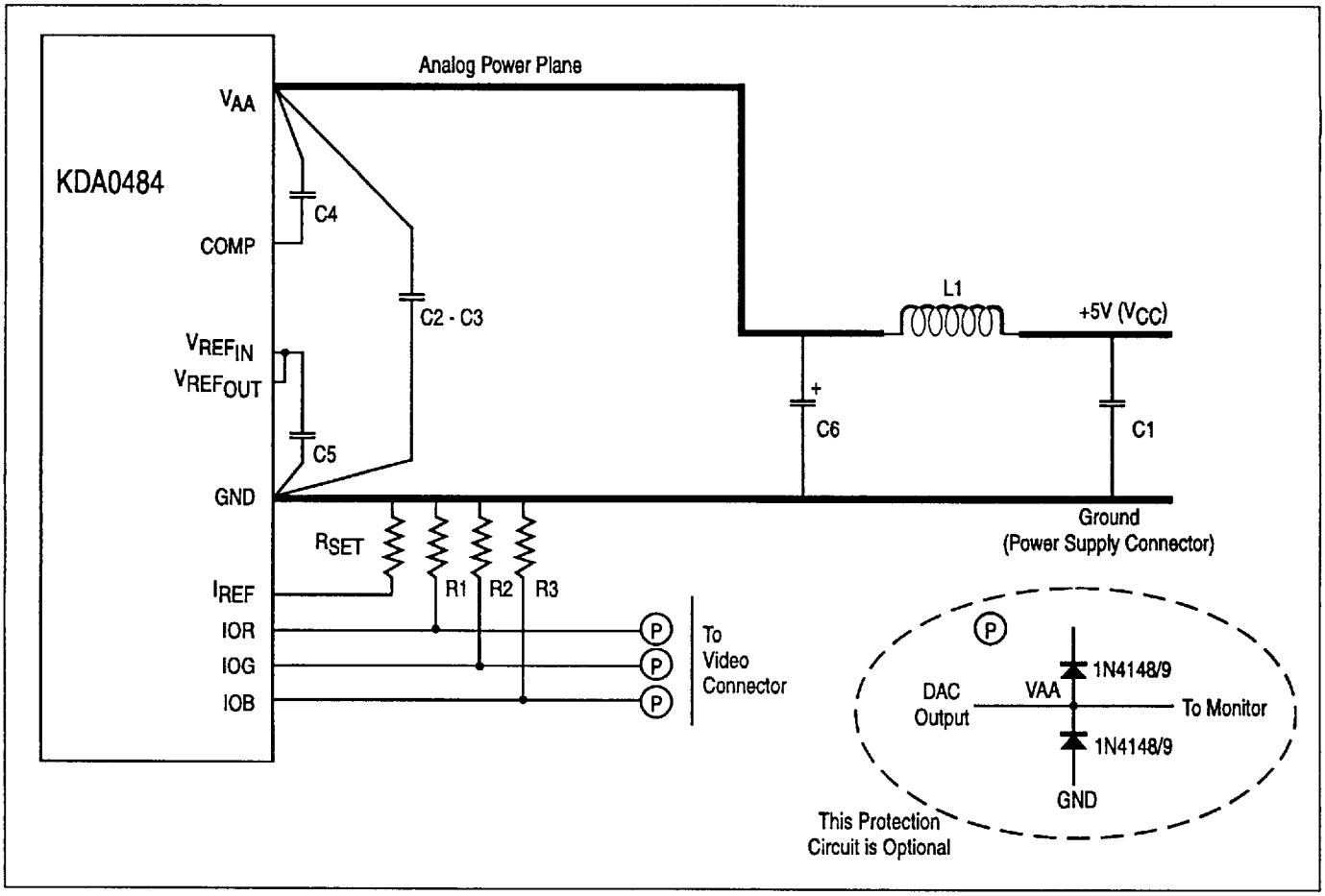
DESIGNING WITH THE KDA0484

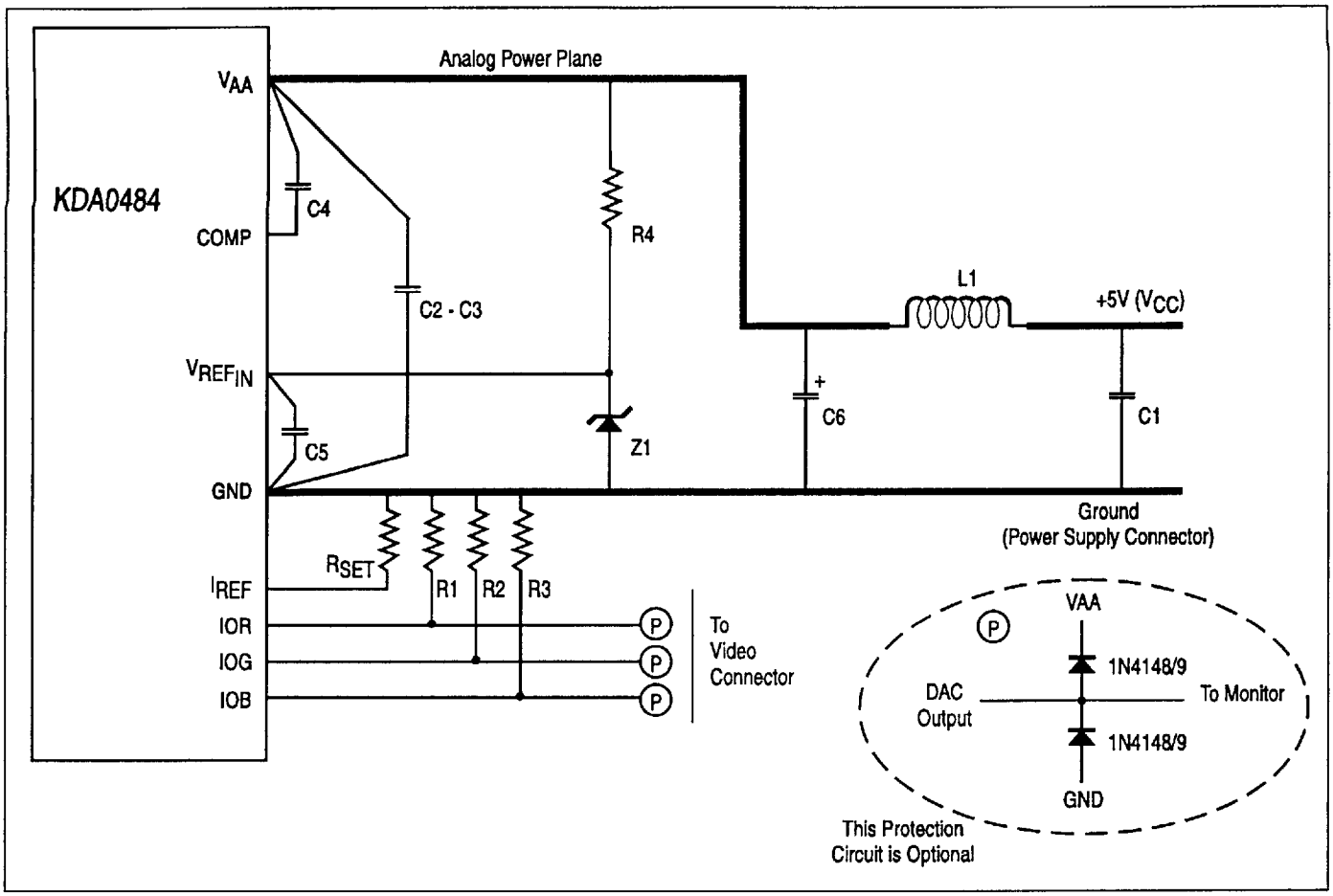


For operation above 75MHz, each group of V_{AA} and GND device pins must be separately decoupled (0.1µF and 0.01µF capacitors)

Location	Description
C1-C5	0.1µF ceramic capacitor
C6	10µF capacitor
L1	Ferrite bead
R1, R2, R3	75Ω 1% metal film resistor
R_{SET}	147Ω 1% metal film resistor

Figure 11: Typical Connection Diagram And Parts List (Internal Voltage Reference)

DESIGNING WITH THE KDA0484



For operation above 75MHz, each group of V_{AA} and GND device pins must be separately decoupled (0.1µF and 0.01µF capacitors)

Location	Description
C1-C5	0.1µF ceramic capacitor
C6	10µF capacitor
L1	Ferrite bead
R1, R2, R3	75Ω 1% metal film resistor
R_{SET}	147Ω 1% metal film resistor
R4	1kΩ 5% metal film resistor
Z1	1.2V voltage reference

Figure 12: Typical Connection Diagram And Parts List (External Voltage Reference)

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DESIGNING WITH THE KDA0484

Analog Output Protection

The KDA0484 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors. *Before connecting or disconnecting the monitor, be sure that power is turned off.*

The diode protection circuit in Figures 11 and 12 and can prevent latch-up under severe discharge conditions without adversely degrading analog transition times.

Digital Signal Interconnect

Isolate the digital inputs to the KDA0484 as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs is caused by excessive edge rates (<3ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feed-through noise is proportional to the digital edge rates. Lower speed applications will benefit from using lower speed logic (3ns to 5ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one-fourth the signal edge time, ringing, overshoot, and undershoot may occur, which will generate noise onto the analog outputs. Line termination or line length reduction is the solution. For example, logic edge rates of 2ns require line lengths of less than four inches without use of termination.

Ringing may be reduced by dampening the line with a series resistor (22Ω to 300Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise and fall time), with dampening resistors, and minimizing coupling through PC board capacitance by routing the digital signals 90° to any analog signal.

Clock driver power pins must be properly decoupled to minimize transients. In designs with parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not to the analog power and ground planes.

Microprocessor Control Signal Interfacing

The KDA0484 uses the RD*, WR*, and RS lines to determine which microprocessor accesses will take place. Glitches or ringing on any of these lines may cause improper microprocessor operation. When a VGA controller with edge rate control is used on these lines, a series termination is not necessary. In a non-VGA controller application, or in applications where the microprocessor control signals are daisy-chained, a series termination, pull-down resistors, or additional capacitance to ground should be used to prevent glitches that could cause improper microprocessor accesses.

Clock Interfacing

The KDA0484 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 10Ω to 68Ω, placed at the pixel clock driver, may be used; or a parallel termination may be used at the pixel clock input to the RAM DAC. A parallel termination of 220Ω to V_{CC} and 330Ω to ground will provide a Thevenin equivalent of a 110Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

ESD and Latch-Up

ESD-sensitive handling procedures are required to prevent device damage. Latch-up can be prevented by ensuring that all V_{AA} pins are at the same potential and that the V_{AA} supply voltage is applied before the signal pin voltages. Correct power-up sequence ensures that signal pin voltage will not exceed the power supply voltage by more than +0.5V.

DESIGNING WITH THE KDA0484

Parameter	Symbol	Min.	Typ.	Max.	Units
Power Supply	V_{AA}	4.75	5.00	5.25	V
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Voltage Reference Configuration	V_{REF}				
Reference Voltage		1.112	1.235	1.359	V

Table 21: Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
V_{AA} (Measured to GND)				7.0	V
Voltage On Any Signal Pin (*NOTE 1*)		GND-0.5		V_{AA} +0.5	V
Analog Output Short Circuit (duration to any power supply or common)	ISC		indefinite		
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TV_{SOL}			220	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5V, or more than -0.5V below ground, can induce destructive latch-up.

Table 22: Absolute Maximum Ratings

Model Number	Speed	Package	T_A Range
KDA0484L-85	85MHz	84-pin Plastic J-Lead	0°C to +70°C
KDA0484L-76	75MHz	84-pin Plastic J-Lead	0°C to +70°C

Table 23: Ordering Information

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PACKAGE DIMENSIONS

84-Pin PLCC Package