

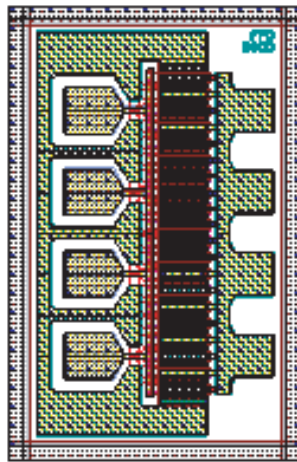


## Product Description

The FPD3000 is an AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT), featuring a  $0.25\mu\text{m} \times 3000\mu\text{m}$  Schottky barrier gate, defined by high-resolution stepper-based photolithography. The recessed gate structure minimizes parasitics to optimize performance. The epitaxial structure and processing have been optimized for reliable high-power applications. The FPD3000 is also available in the low-cost plastic SOT89 package.

### Optimum Technology Matching® Applied

- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ InGaP HBT
- ☐ SiGe BiCMOS
- ☐ Si BiCMOS
- ☐ SiGe HBT
- ☒ GaAs pHEMT
- ☐ Si CMOS
- ☐ Si BJT
- ☐ GaN HEMT
- ☐ InP HBT
- ☐ RF MEMS
- ☐ LDMOS



## Features

- 32.5dBm Linear Output Power at 12GHz
- 6.5dB Power Gain at 12GHz
- 8dB Max Stable Gain at 12GHz
- 42dBm  $O_{IP3}$
- 30% Power-Added Efficiency

## Applications

- Narrowband and Broadband High-Performance Amplifiers
- SATCOM Uplink Transmitters
- PCS/Cellular Low-Voltage High-Efficiency Output Amplifiers
- Medium-Haul Digital Radio Transmitters

| Parameter                                          | Specification |      |      | Unit | Condition                                                                                       |
|----------------------------------------------------|---------------|------|------|------|-------------------------------------------------------------------------------------------------|
|                                                    | Min.          | Typ. | Max. |      |                                                                                                 |
| Electrical Specifications                          |               |      |      |      |                                                                                                 |
| P <sub>1dB</sub> Gain Compression                  | 31.5          | 32.5 |      | dBm  | V <sub>DS</sub> =8V, I <sub>DS</sub> =50% I <sub>DSS</sub>                                      |
| Maximum Stable Gain (S21/S12)                      | 7.0           | 8.0  |      | dB   | V <sub>DS</sub> =8V, I <sub>DS</sub> =50% I <sub>DSS</sub>                                      |
| Power Gain at P <sub>1dB</sub> (G <sub>1dB</sub> ) | 6.0           | 6.5  |      | dB   | V <sub>DS</sub> =8V, I <sub>DS</sub> =50% I <sub>DSS</sub>                                      |
| Power-Added Efficiency (PAE)                       |               | 30   |      | %    | V <sub>DS</sub> =8V, I <sub>DS</sub> =50% I <sub>DSS</sub> , P <sub>OUT</sub> =P <sub>1dB</sub> |
| OIP <sub>3</sub>                                   |               | 42   |      | dBm  | V <sub>DS</sub> =8V, I <sub>DS</sub> =50% I <sub>DSS</sub>                                      |
|                                                    |               | 44   |      | dBm  | Matched for optimal power, tuned for best IP <sub>3</sub>                                       |
| Saturated Drain-Source Current (I <sub>DSS</sub> ) | 750           | 930  | 1100 | mA   | V <sub>DS</sub> =1.3V, V <sub>GS</sub> =0V                                                      |
| Maximum Drain-Source Current (I <sub>MAX</sub> )   |               | 1.5  |      | A    | V <sub>DS</sub> =1.3V, V <sub>GS</sub> ≈+1V                                                     |
| Transconductance (G <sub>M</sub> )                 |               | 800  |      | ms   | V <sub>DS</sub> =1.3V, V <sub>GS</sub> =0 V                                                     |
| Gate-Source Leakage Current (I <sub>GSO</sub> )    |               | 10   |      | μA   | V <sub>GS</sub> = -5V                                                                           |
| Pinch-Off Voltage (V <sub>p</sub> )                |               | 1.0  |      | V    | V <sub>DS</sub> =1.3V, I <sub>DS</sub> =3mA                                                     |
| Gate-Source Breakdown Voltage (V <sub>BDS</sub> )  | 12.0          | 14.0 |      | V    | I <sub>GS</sub> =3mA                                                                            |
| Gate-Drain Breakdown Voltage (V <sub>BGD</sub> )   | 14.5          | 16.0 |      | V    | I <sub>GD</sub> =3mA                                                                            |
| Thermal Resistivity (θJC)                          |               | 20   |      | °C/W | V <sub>DS</sub> >6V                                                                             |

Note:  $T_{AMBIENT}=22^{\circ}C$ , RF specifications measured at  $f=12GHz$  using CW signal.

## Absolute Maximum Ratings<sup>1</sup>

| Parameter                                                                       | Rating     | Unit |
|---------------------------------------------------------------------------------|------------|------|
| Drain-Source Voltage ( $V_{DS}$ )<br>( $-3V < V_{GS} < -0.5V$ ) <sup>2</sup>    | 10         | V    |
| Gate-Source Voltage ( $V_{GS}$ )<br>( $0V < V_{DS} < +8V$ )                     | -3         | V    |
| Drain-Source Current ( $I_{DS}$ )<br>(For $V_{DS} < 2V$ )                       | $I_{DSS}$  |      |
| Gate Current ( $I_G$ )<br>(Forward or reverse current)                          | 25         | mA   |
| RF Input Power ( $P_{IN}$ )<br>(Under any acceptable bias state)                | 600        | mW   |
| Channel Operating Temperature ( $T_{CH}$ )<br>(Under any acceptable bias state) | 175        | °C   |
| Storage Temperature ( $T_{STG}$ )<br>(Non-Operating Storage)                    | -65 to 150 | °C   |
| Total Power Dissipation ( $P_{TOT}$ ) <sup>3, 4, 5</sup>                        | 7.3        | W    |
| Simultaneous Combination of Limits <sup>6</sup><br>(2 or more max. limits)      | 80         | %    |

Notes:

<sup>1</sup> $T_{AMBIENT} = 22^\circ\text{C}$  unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device.

<sup>2</sup>Operating at absolute maximum  $V_D$  continuously is not recommended. If operation at 10V is considered then  $I_{DS}$  must be reduced in order to keep the part within its thermal power dissipation limits. Therefore  $V_{GS}$  is restricted to  $< -0.5V$ .

<sup>3</sup>Total Power Dissipation to be de-rated as follows above  $22^\circ\text{C}$ :  $P_{TOT} = 7.3 - (0.05W/^\circ\text{C}) \times T_{HS}$ , where  $T_{HS}$  = heatsink or ambient temperature above  $22^\circ\text{C}$ .

Example: For a  $85^\circ\text{C}$  carrier temperature:  $P_{TOT} = 7.3 - (0.05 \times (85 - 22)) = 4.2W$

<sup>4</sup>Total Power Dissipation ( $P_{TOT}$ ) defined as  $(P_{DC} + P_{IN}) - P_{OUT}$ , where  $P_{DC}$ : DC Bias Power,  $P_{IN}$ : RF Input Power,  $P_{OUT}$ : RF Output Power.

<sup>5</sup>Users should avoid exceeding 80% of 2 or more Limits simultaneously.

<sup>6</sup>Thermal Resistivity specification assumes a Au/Sn eutectic die attach onto an Au-plated copper heatsink or rib.



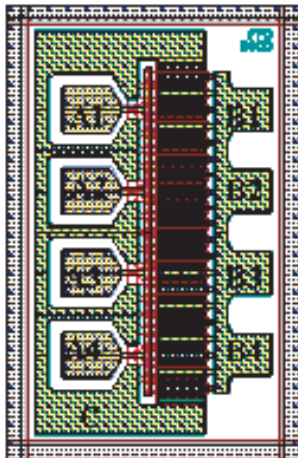
**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

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## Pad Layout



| Pad | Description | Pin Coordinates ( $\mu\text{m}$ ) |
|-----|-------------|-----------------------------------|
| A1  | Gate Pad    | 125, 625                          |
| A2  | Gate Pad    | 125, 475                          |
| A3  | Gate Pad    | 125, 325                          |
| A4  | Gate Pad    | 125, 175                          |
| B1  | Drain Pad   | 375, 625                          |
| B2  | Drain Pad   | 375, 475                          |
| B3  | Drain Pad   | 375, 325                          |
| B4  | Drain Pad   | 375, 175                          |
| C   | Source Pad  |                                   |

Note: Coordinates are referenced from the bottom left hand corner of the die to the center of the bond pad opening.

| Die Size ( $\mu\text{m}$ ) | Die Thickness ( $\mu\text{m}$ ) | Min. Bond Pad Opening ( $\mu\text{m} \times \mu\text{m}$ ) |
|----------------------------|---------------------------------|------------------------------------------------------------|
| 470x830                    | 75                              | 68x77                                                      |

## Preferred Assembly Instructions

GaAs devices are fragile and should be handled with great care. Specially designed collets should be used where possible.

The back of the die is metallized and the recommended mounting method is by the use of conductive epoxy. Epoxy should be applied to the attachment surface uniformly and sparingly to avoid encroachment of epoxy onto the top face of the die. Ideally it should not exceed half the chip height. For automated dispense Ablestick LMISR4 is recommended and for manual dispense Ablestick 84-1 LMI or 84-1 LMIT are recommended. These should be cured at a temperature of 150 °C for one hour in an oven especially set aside for epoxy curing only. If possible the curing oven should be flushed with dry nitrogen. The gold-tin (80% Au 20% Sn) eutectic die attach has a melting point of approximately 280 °C but the absolute temperature being used depends on the leadframe material used and the particular application. The maximum time at used should be kept to a minimum.

This part has gold (Au) bond pads requiring the use of gold (99.99% pure) bondwire. It is recommended that 25.4mm diameter gold wire be used. Recommended lead bond technique is thermocompression wedge bonding with 0.001" (25µm) diameter wire. Bond force, time stage temperature and ultrasonics are all critical parameters and the settings are dependent on the setup and application being used. Ultrasonic or thermosonic bonding is not recommended.

Bonds should be made from the die first and then to the mounting substrate or package. The physical length of the bondwires should be minimized especially when making RF or ground connections.

## Handling Precautions



To avoid damage to the devices, care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing.

## ESD/MSL Rating

These devices should be treated as Class 0 (0V to 250V) using the human body model as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263. This is an unpackaged part and therefore no MSL rating applies.

## Application Notes and Design Data

Application Notes and design data including S-parameters and device model are available on request from [www.rfmd.com](http://www.rfmd.com).

## Reliability

An MTTF of 4.2 million hours at a channel temperature of 150 °C is achieved for the process used to manufacture this device.

## Disclaimers

This product is not designed for use in any space-based or life-sustaining/supporting equipment.

## Ordering Information

| Delivery Quantity   | Ordering Code |
|---------------------|---------------|
| Full Pack (100)     | FPD3000-000   |
| Small Quantity (25) | FPD3000-000SQ |
| Sample Quantity (3) | FPD3000-000S3 |

