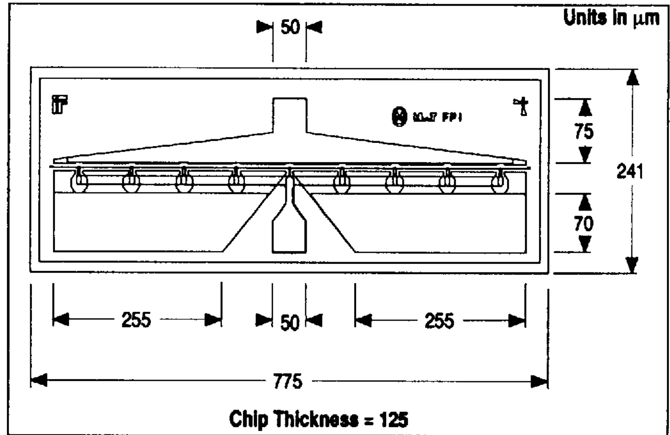
MICROWAVE TECHNOLOGY

MwT-1
12 GHz High Gain GaAs FET



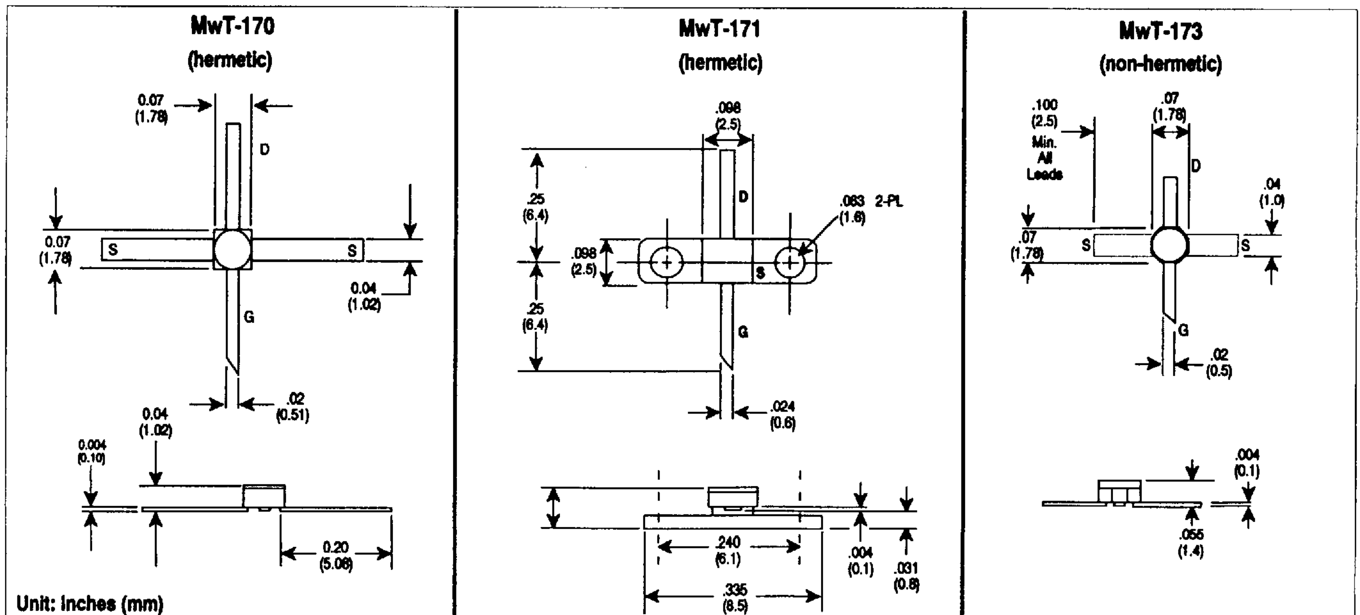
- **10 dB GAIN AT 12 GHz**
- **EXCELLENT FOR FEEDBACK AMPLIFIER APPLICATIONS 100 MHz TO 12 GHz**
- **0.3 MICRON REFRACTORY METAL/GOLD GATE**
- **630 MICRON GATE WIDTH**
- **CHOICE OF CHIP AND THREE PACKAGE TYPES**

DESCRIPTION

The MwT-1 is a GaAs MESFET device whose nominal quarter-micron gate length and 630 micron gate width make it ideally suited to applications requiring high-gain in the 100 MHz to 12 GHz frequency range. The straight gate geometry of the MwT-1 makes it equally effective for either wideband (ex. 2 to 6 GHz) or narrow-band applications (ex. 2.4 to 2.5 GHz). The chip is produced using MwT's reliable metal system and all devices are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for durability with no degradation in performance. Designers can use MwT's unique BIN selection feature to choose devices from narrow Idss ranges, insuring consistent circuit operation.

RF SPECIFICATIONS AT Ta = 25°C

				MwT-1 SG MwT-170 SG MwT-171SG MwT-173 SG			MwT-1 HG MwT-170 HG MwT-171HG MwT-173 HG		
SYMBOL	**PARAMETERS AND CONDITIONS**	**FREQ**	**UNITS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**
SSG	Small Signal Gain VDS=5.0V IDS=0.6 x IDSS	12 GHz	dB	9.0	9.5		9.0	10.0	
P1dB	Output Power at 1dB Compression VDS=5.0V IDS=0.6 x IDSS	12 GHz	dBm	21.0	22.0		23.0	24.0	
NFopt	Optimum Noise Figure VDS = 3.0 V IDS = 30 mA	12 GHz	dB		2.2	2.5		2.0	2.3
GA	Gain @ Opt. NF VDS = 3.0 V IDS = 30 mA	12 GHz	dB		7.0			7.0	
IDSS	Recommended IDSS Range for Optimum P1dB		mA		80- 160			120- 210	



DC SPECIFICATIONS AT Ta = 25 °C

SYMBOL	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
Idss	Saturated Drain Current Vds=4.0 V VGS=0.0 V	mA	60		240
Gm	Transconductance Vds=4.0 V VGS=0.0 V	mS	90	120	
Vp	Pinch-off Voltage Vds=3.0 V IDS=4.0 mA	V		-2.0	-5.0
BVGSO	Gate-to-Source Breakdown Voltage Igs=-1.0 mA	V	-5.0	-10.0	
BVGDO	Gate-to-Drain Breakdown Voltage Igd=-1.0 mA	V	-6.0	-10.0	
Rth	Thermal Resistance* MwT-1, MwT-171 MwT-170, -173	°C/W			80 180*

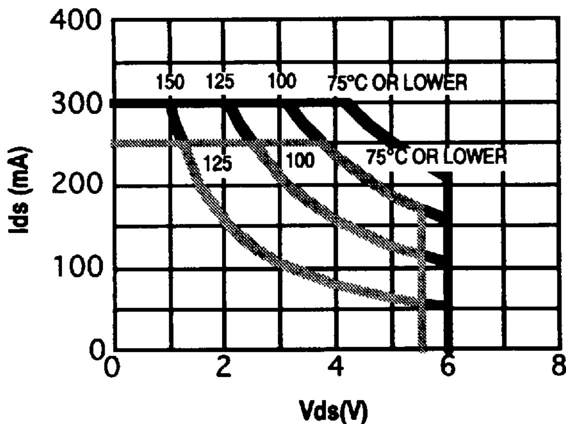
* Overall Rth depends on case mounting

MAXIMUM RATINGS AT Ta = 25 ° C

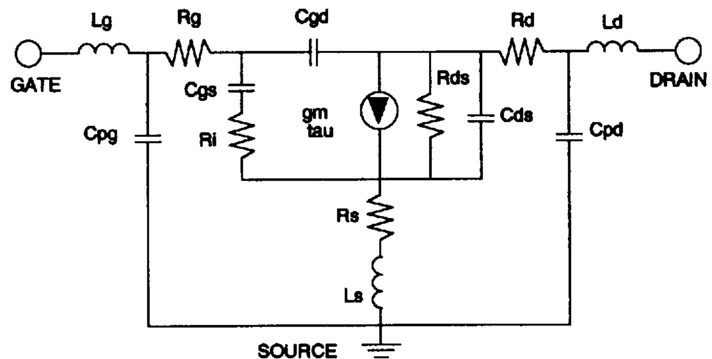
SYMBOL	PARAMETER	UNITS	CONT MAX[1]	ABSOLUTE MAX[2]
VDS	Drain to Source Voltage	V	See Safe Operating Limits	
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	200	300

NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goals.
2. Exceeding any one of these limits may cause permanent damage.

SAFE OPERATING LIMITS vs. Case Temperature



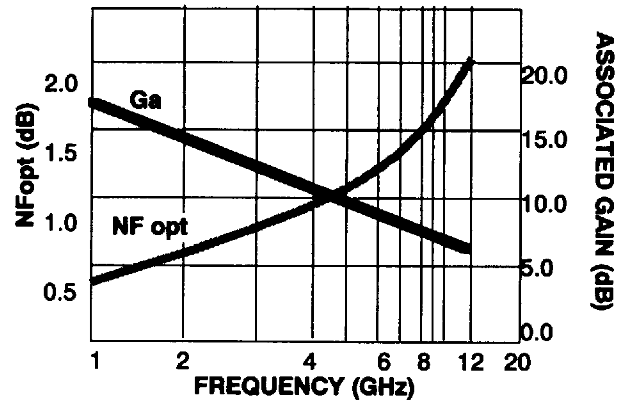
DEVICE EQUIVALENT CIRCUIT MODEL



PARAMETER		VALUE
Gate Bond Wire Inductance	Lg	.20 nH
Gate Pad Capacitance	Cpg	.09 pF
Gate Resistance	Rg	0.83 Ω
Gate-Source Capacitance	Cgs	.64 pF
Channel Resistance	Ri	4.11 Ω
Gate-Drain Capacitance	Cgd	.06 pF
Transconductance	gm	130 mS
Transit time	tau	2 psec

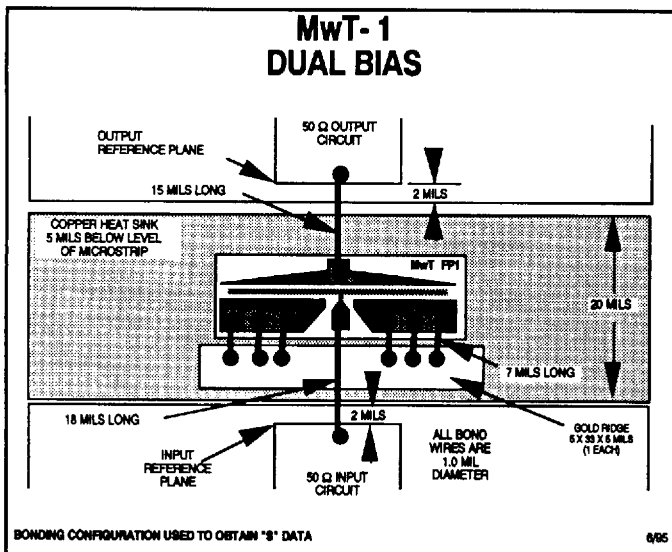
PARAMETER		VALUE
Source Resistance	Rs	1.88 Ω
Source Inductance	Ls	.04 nH
Drain-Source Resistance	Rds	90 Ω
Drain-Source Capacitance	Cds	.001 pF
Drain Resistance	Rd	2.90 Ω
Drain Pad Capacitance	Cpd	.145 pF
Drain Inductance	Ld	.32 nH

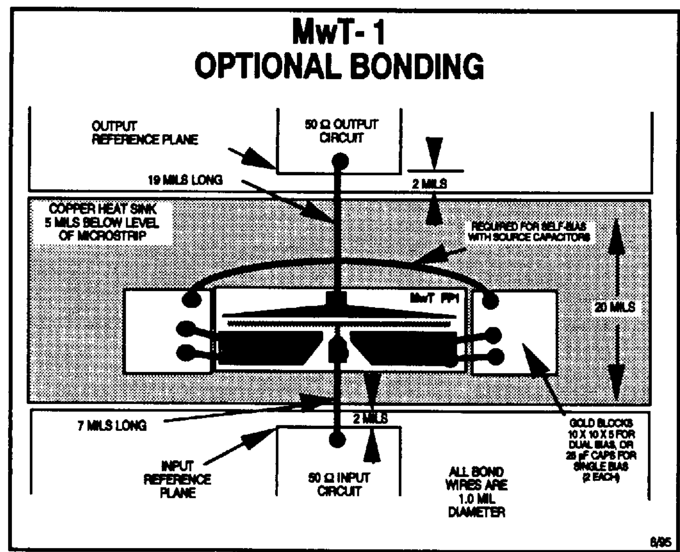
FREQUENCY GHz	NF MIN dB	GAMMA OPT MAG	GAMMA OPT ANGLE	Rn/50
1.00	.45	.885	32	1.27
2.00	.65	.722	61	.50
4.00	.95	.591	110	.24
6.00	1.25	.610	139	.17
8.00	1.52	.656	157	.14
12.00	1.88	.733	176	.11



RECOMMENDED ASSEMBLY CONFIGURATION

Shown below is the assembly and bonding configuration used for S-Parameter measurements of the MwT-1 chip. This configuration is recommended for optimum performance. For single-bias applications the gold blocks may be replaced by capacitors. An additional interconnecting bond would then be required. Contact MwT for additional applications information.





BIN SELECTION

Every MwT-1 wafer has been probed for Idss and the data stored on computer disk. Customers may select from Idss values in any of 18 current bins, as shown below, to insure consistent performance in their circuit. The shaded bins are typically available in smaller quantity and caution is advised before designing these bins into high production applications. MwT's "Smart Wafer Picker" reads the stored Idss Data from the disk and devices from customer selected bins are quickly and automatically picked from the wafer and loaded into shipping containers.

BIN#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
IDSS (mA)	60-70	70-80	80-90	90-100	100-110	110-120	120-130	130-140	140-150	150-160	160-170	170-180	180-190	190-200	200-210	210-220	220-230	230-240

BIN ACCURACY

Due to the effects of temperature, dc loading and probe tip varnishing, the IDSS from the "on wafer" probing of any MwT device may differ after it has been attached to a proper heat sink and tested in an RF or DC circuit.

Because of the aforementioned effects, the IDSS distribution may deviate as much as +/- 1 bin within the range identified on the label of each die shipping container, and +/- 2 bins within the selected range.

TYPICAL COMMON SOURCE SCATTERING PARAMETERS

MwT-1 CHIP: VDS = 5.0 V, IDS = 0.6 IDSS = 80 mA

FREQUENCY (GHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1000	.95	-31.7	6.68	156.4	.029	73.2	.45	-16.3
2000	.88	-58.8	5.86	137.2	.050	61.3	.41	-30.1
3000	.84	-82.5	5.18	120.6	.066	51.8	.36	-42.0
4000	.79	-102.2	4.46	106.4	.075	45.6	.31	-51.5
5000	.76	-117.9	3.88	94.6	.081	43.5	.27	-59.9
6000	.74	-130.4	3.42	84.6	.087	40.4	.24	-69.4
7000	.72	-141.5	3.04	75.2	.092	39.3	.22	-79.0
8000	.71	-150.8	2.71	66.9	.096	37.9	.20	-90.5
9000	.71	-158.6	2.46	60.0	.099	37.1	.18	-103.8
10000	.71	-165.7	2.28	53.1	.099	37.5	.17	-118.3
12000	.72	-179.1	2.01	38.9	.110	40.5	.19	-146.8
14000	.73	166.8	1.75	23.5	.134	38.8	.24	-171.1
16000	.75	154.3	1.50	10.9	.149	32.8	.32	168.8
18000	.80	144.3	1.32	-1.4	.163	29.5	.39	154.0
20000	.85	135.2	1.15	-13.4	.178	25.6	.48	140.2

MwT-170SG: VDS = 5.0 V, IDS = 0.6 IDSS = 80 mA

FREQUENCY (GHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1.00	.92	-46.0	6.56	142.1	.03	60.2	.41	-31.3
2.00	.78	-77.6	5.11	115.9	.05	45.0	.43	-48.4
3.00	.69	-100.8	4.19	97.2	.06	35.6	.41	-57.3
4.00	.62	-125.5	3.73	80.8	.07	30.0	.38	-64.8
5.00	.57	-156.0	3.47	64.6	.08	25.1	.29	-73.0
6.00	.61	174.2	3.25	47.1	.09	17.9	.23	-92.2
7.00	.69	149.3	3.01	29.9	.08	5.3	.17	-128.9
8.00	.81	130.5	2.80	14.7	.08	1.5	.20	-173.6
9.00	.86	116.6	2.57	-3.3	.09	4.8	.29	172.6
10.00	.82	106.4	2.28	-18.7	.12	-9.9	.39	172.0
11.00	.84	97.2	2.11	-33.8	.11	-32.0	.49	165.1
12.00	.86	79.6	2.01	-51.4	.10	-46.9	.55	154.6

MwT-171: VDS = 5.0 V, IDS = 0.6 IDSS = 100 mA

FREQUENCY (GHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1.00	.94	-54.2	7.55	141.6	.03	57.0	.42	-37.8
2.00	.86	-93.0	5.80	113.3	.05	34.8	.37	-63.8
3.00	.81	-118.1	4.54	93.5	.06	21.0	.36	-80.6
4.00	.77	-135.6	3.73	77.8	.06	8.5	.34	-91.0
5.00	.77	-149.5	3.34	63.7	.06	4.2	.37	-99.5
6.00	.76	-165.3	3.07	48.7	.07	-6.5	.36	-109.9
7.00	.76	177.1	2.98	32.2	.07	-17.4	.35	-120.2
8.00	.77	155.3	2.84	14.9	.08	-30.7	.30	-136.0
9.00	.78	132.8	2.69	-2.7	.08	-43.6	.24	-152.7
10.00	.80	112.4	2.58	-20.7	.09	-52.3	.20	-174.6
11.00	.83	94.1	2.44	-38.3	.10	-60.0	.20	162.0
12.00	.83	77.0	2.27	-56.1	.10	-74.0	.24	142.1
14.00	.76	43.8	2.02	-91.3	.11	-92.2	.24	121.1
16.00	.65	1.4	1.66	-132.3	.14	-118.5	.11	97.2
18.00	.59	-41.4	1.38	-168.6	.20	-132.8	.07	-46.4

MwT-173SG: VDS = 5.0 V, IDS = 0.6 IDSS = 80 mA

FREQUENCY (GHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1.00	.91	-49.9	7.18	143.3	.04	62.6	.46	-28.4
2.00	.79	-86.8	5.72	116.6	.05	47.2	.41	-46.6
3.00	.70	-115.3	4.74	96.3	.07	38.8	.38	-60.1
4.00	.61	-145.3	4.07	77.4	.09	27.2	.32	-69.1
5.00	.57	-177.6	3.71	60.6	.08	20.4	.27	-75.3
6.00	.64	148.3	3.32	39.7	.09	14.3	.21	-99.5
7.00	.73	120.8	2.81	21.5	.09	5.2	.15	-138.6
8.00	.83	103.0	2.43	6.4	.09	-0.2	.17	-176.9
9.00	.82	90.9	1.96	-8.9	.09	-6.6	.23	163.8
10.00	.84	85.3	1.68	-20.1	.10	-16.7	.30	154.5
11.00	.87	79.9	1.51	-29.7	.08	-26.0	.36	148.5
12.00	.89	71.5	1.43	-40.8	.08	-22.5	.39	143.2

DEVICE HANDLING PROCEDURE

1) Open package in clean room environment only.
2) GaAs FETs are sensitive to electrostatic discharge. Precautions should be taken in handling, die attachment, and bonding to assure that Maximum Ratings are not exceeded as a result of electrical discharge.
3) Chips have been cleaned and are ready for die attachment. DO NOT attempt to re-clean.
4) Assembly should be performed with parts no hotter than 300° C. All circuit components (such as resistors and capacitors) should be assembled completely before the FET is die attached. Assembly should be performed as quickly as possible. In general, no chip should be left at 300°C for over 2 minutes.
5) Die attach with clean AuSn alloy under forming gas at 280 to 300° C. Scrub chip down with tweezers. Thermal resistance is critically dependent on this operation.
6) Thermasonic wedge bonding is recommended. A .0015 in. bond flat wedge at 125 to 150° C should be used with a heater stage temperature of 200 to 225° C. Apply 15 to 20 grams of bond force to .001 in. diameter gold wire with an elongation of 2 to 5%.
7) Store in a clean, dry, inert environment such as nitrogen at room temperature.
8) CAUTION: Handling of chips other than as specified above may cause permanent damage.

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