54F/74F395

4-Bit Cascadable Shift Register With 3-State Outputs

Description

The 'F395 is a 4-bit Shift Register with serial and parallel synchronous operating modes and four 3-state buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is HIGH, data is loaded from the Parallel Data inputs (D_0-D_3) into the register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). When PE is LOW, the data at the Serial Data input (D_s) is loaded into the Q_0 flip-flop, and the data in the register is shifted one bit to the right in the direction (Q_0-Q_1-Q_2-Q_3) synchronous with the negative clock transition. The PE and Data inputs are fully edge-triggered and must be stable only one setup prior to the HIGH-to-LOW transition of the clock.

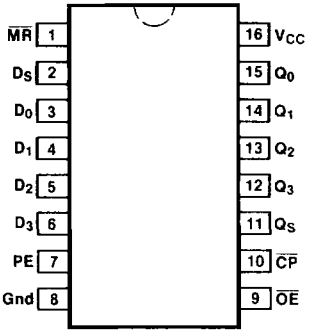
The Master Reset ($\overline{MR}$) is an asynchronous Active LOW input. When LOW, the $\overline{MR}$ overrides the clock and all other inputs and clears the register.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, or large capacitive loads. The Active LOW Output Enable ($\overline{OE}$) controls all four 3-state buffers independent of the register operation. The data in the register appears at the outputs when $\overline{OE}$ is LOW. The outputs are in the high impedance (OFF) state, which means they will neither drive nor load the bus when $\overline{OE}$ is HIGH. The output from the last stage is brought out separately. This output (Q_s) is tied to the Serial Data input (D_s) of the next register for serial expansion applications. The Q_s output is not affected by the 3-state buffer operation.

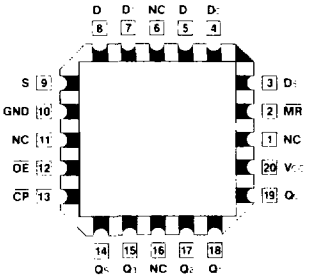
- **4-Bit Parallel Load Shift Register**
- **Independent 3-State Buffer Outputs**
- **Separate Q_s Output for Serial Expansion**
- **Asynchronous Master Reset**

Ordering Code: See Section 5

Connection Diagrams

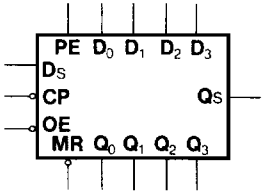


Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Logic Symbol



Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0, D_1, D_2, D_3	Data Inputs	0.5/0.375
D_s	Serial Data Input	0.5/0.375
PE	Enable Input	0.5/0.375
$\overline{MR}$	Master Reset (Active LOW)	0.5/0.375
$\overline{OE}$	Output Enable (Active LOW)	0.5/0.375
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0.5/0.375
Q_s	Serial Expansion Output	25/12.5
Q_0, Q_1, Q_2, Q_3	Data Outputs	75/15 (12.5)

Mode Select-Function Tables

Register Operating Modes	Inputs					Outputs			
	$\overline{MR}$	$\overline{CP}$	PE	D_s	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	L	X	X	X	X	L	L	L	L
Shift Right	H	↓	l	l	X	L	q_0	q_1	q_2
	H	↓	l	h	X	H	q_0	q_1	q_2
Parallel Load	H	↓	h	X	l	L	L	L	L
	H	↓	h	X	h	H	H	H	H

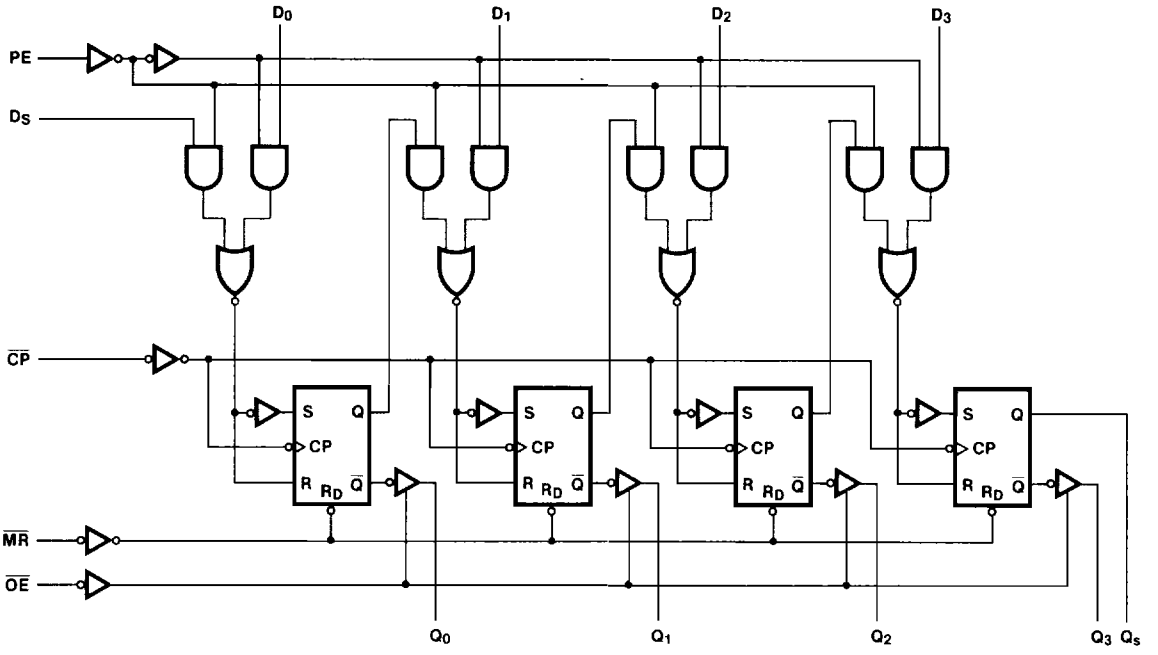
3-State Buffer Operating Modes	Inputs		Outputs	
	$\overline{OE}$	Q_n(Register)	Q_0, Q_1, Q_2, Q_3	Q_s
Read	L	L	L	L
	L	H	H	H
Disable Buffers	H	L	Z	L
	H	H	Z	H

H = HIGH Voltage Level
L = LOW Voltage Level
q_n = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock Transition
X = Immaterial
Z = High Impedance
↓ = HIGH-to-LOW transition

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current				mA	V_{CC} = Max

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0$ V $C_L = 50$ pF			54F T_A, V_{CC} = Mil $C_L = 50$ pF		74F T_A, V_{CC} = Com $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	105							MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay Clock to Buffer Outputs		7.0 7.0						ns	3-1 3-8
t_{PLH} t_{PHL}	Propagation Delay Clock to Q_s Output		7.0 7.0						ns	3-1 3-8
t_{PHL}	Propagation Delay $\overline{MR}$ to Output		12.0						ns	3-1 3-9
t_{PZH} t_{PZL}	Enable Time		11.5 7.5						ns	3-1, 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time		7.0 5.5						ns	3-1, 3-12 3-13

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\,V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Data to Clock	4.0 4.0			ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Data to Clock	0 0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW PE to Clock	8.0 8.0			ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW PE to Clock	0 0				
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse Width HIGH or LOW	5.0 5.0			ns	3-8
$t_w(H)$ $t_w(L)$	$\overline{MR}$ Pulse Width HIGH or LOW	5.0 5.0			ns	3-9
t_{rec}	Recovery Time, $\overline{MR}$ to Clock	7.0			ns	3-11