Preliminary Data Sheet
February 1997

microelectronics group

Lucent Technologies
Bell Labs Innovations

T5504 - - 1MC2 Quad PCM Codec with Filters

Features

- +5 V only
- Low-power, latch-up-free CMOS technology
  - — 37 mW/channel typical operating power dissipation
  - — 1 mW/channel typical powerdown dissipation
- 4.096 MHz master clock frequency
- On-chip sample and hold, autozero, and precision voltage reference
- Differential architecture for high noise immunity and power supply rejection
- 4.096 MHz data rate time-slotted PCM interface
- Meets or exceeds D3/D4 (as per Lucent PUB43801) and ITU-T G.711—G.714 requirements
- Operating temperature range: 0 °C to 70 °C
- A-law companding

Description

The T5504 - - 1MC2 device is a single-chip, four-channel A-law PCM codec with filters. This integrated circuit provides analog-to-digital and digital-to-analog conversion. It provides the transmit and receive filtering necessary to interface a voice telephone circuit to a time-division multiplexed system. This device is packaged in a 28-pin PLCC.

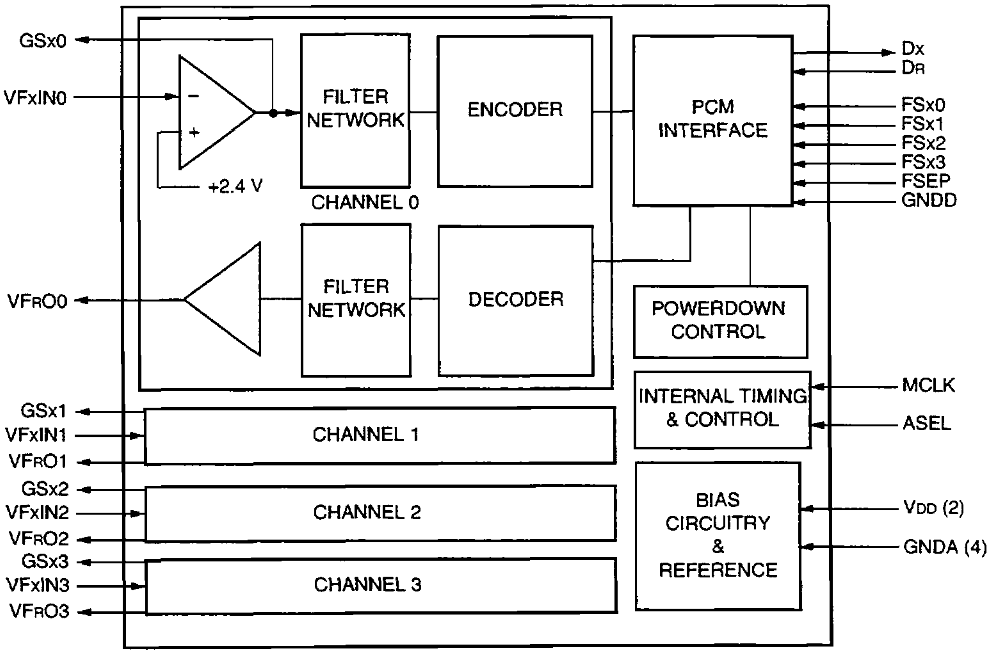

Figure 1. Block Diagram

Functional Description

Four channels of PCM data input and output are passed through only two ports, Dx and DR, so some type of time-slot assignment is necessary. The scheme used here is to utilize a timing mode of 64 time slots corresponding to a master clock frequency of 4.096 MHz. Each device has four transmit frame sync (FSx) inputs, one for each channel. During a single 125 µs frame, each transmit frame sync input is supplied a single pulse. The timing of the pulse indicates the beginning of the time slot during which the data for that channel is clocked out of the device. During a frame, transmit frame sync pulses must be separated from each other by one or more time slots. A channel is placed in a standby (low-power) mode if its FSx input has been low for 500 µs.

There is a single frame sync separation input (FSEP). The number of negative clock edges minus one that occurs while FSEP is high is the delay (in clock periods) that is placed between the rising edge of a transmit frame sign bit and the falling edge used by the receiver to sample the sign bit. There must always be a pulse on the FSEP input since this input provides the 8 kHz signal required to maintain internal timing. If the FSEP pulse is one clock period or less, the device makes the transmit edges and receive sampling edges one half clock period apart. The entire device is placed in a powerdown mode if FSEP remains low for 500 µs.

Time slot zero is defined as starting on the first rising MCLK edge after FSEP = 1 is detected by a negative MCLK edge. FSxN for time slot zero nominally starts on the MCLK positive edge following the negative edge that detects FSEP. FSxN for other time slots are multiples of eight MCLKs after FSxN for time slot zero.

The frequency of the master clock must be 4.096 MHz. Internal circuitry determines the master clock frequency during the powerup reset interval.

Powerdown is not guaranteed if MCLK is lost unless the device is already in the powerdown mode due to FSEP low for at least 500 µs.

The analog input section in Figure 2 includes an on-chip op amp that is used in conjunction with external, user-supplied resistors to vary encoder passband gain. The load impedance to ground at the GSx outputs should be greater than 10 kΩ in parallel with less than 50 pF. The input signal at VFxIN should be ac coupled. For best performance, the maximum gain of this op amp should be limited to 20 dB or less.

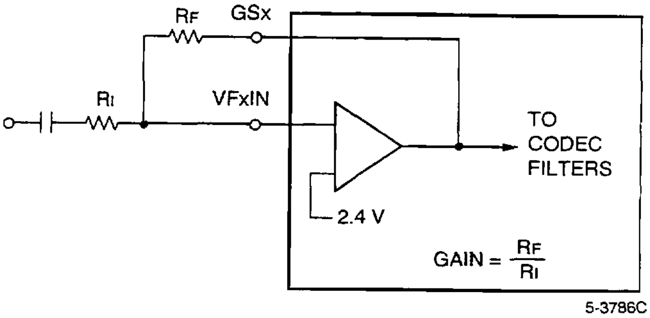

Figure 2. Typical Analog Input Section

Pin Information

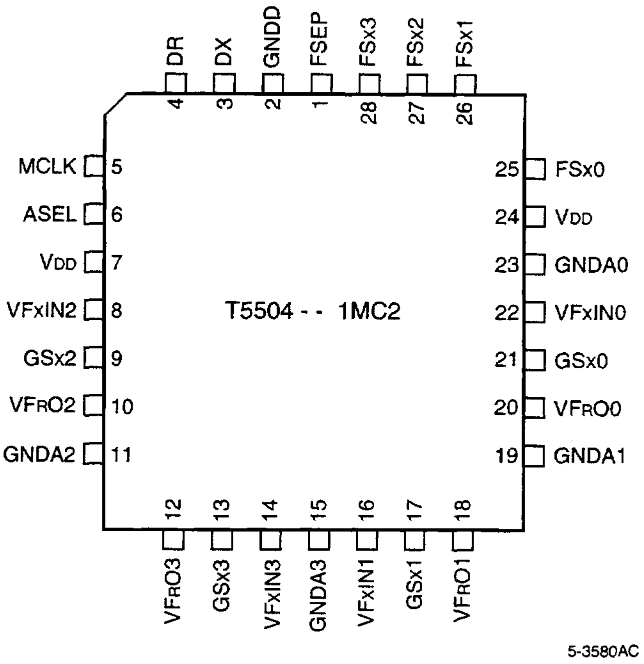

Figure 3. Pin Diagram

Pin Information (continued)

Table 1. Pin Descriptions

Symbol	Pin	Type*	Name/Function
VFxIN3 VFxIN2 VFxIN1 VFxIN0	14 8 16 22	I	**Voice Frequency Transmitter Input.** Analog inverting input to the uncommitted operational amplifier at the transmit filter input. Connect the signal to be digitized to this pin through a resistor RI (see Figure 2).
GSx3 GSx2 GSx1 GSx0	13 9 17 21	O	**Gain Set for Transmitter.** Output of the transmit uncommitted operational amplifier. The pin is the input to the transmit differential filters. Connect the pin to its corresponding VFxIN through a resistor RF (see Figure 2).
VFRO3 VFRO2 VFRO1 VFRO0	12 10 18 20	O	**Voice Frequency Receiver Output.** This pin can drive 2000 Ω (or greater) loads.
VDD[1:0]	7, 24	—	**+5 V Analog Power Supplies.** Both pins must be connected on the circuit board. Each pin should be bypassed to ground with at least 0.1 µF of capacitance as close to the device as possible.
GNDA3 GNDA2 GNDA1 GNDA0	15 11 19 23	—	**Analog Grounds.** All ground pins must be connected on the circuit board.
DR	4	I	**Receive PCM Data Input.** The data on this pin is shifted into the device on the falling edges of MCLK. Data is only entered for valid time slots as defined by the relationship of the pulses on the FSx inputs and the pulse on the FSEP input.
Dx	3	O	**Transmit PCM Data Output.** This pin remains in the high-impedance state except during active transmit time slots. An active transmit time slot is defined as one in which a pulse is present on one of the FSx inputs. Data is shifted out on the rising edge of MCLK.
MCLK	5	I	**Master Clock Input.** The frequency must be 4.096 MHz. This clock serves as the bit clock for all PCM data transfer. A 40% to 60% duty cycle is required.
GNDD	2	—	**Digital Ground.** Ground connection for the digital circuitry of the T5504 - - 1MC2. All ground pins must be connected on the circuit board.
FSx3 FSx2 FSx1 FSx0	28 27 26 25	I^d	**Transmit Frame Sync.** This signal is an edge trigger and must be high for a minimum of one MCLK cycle. This signal must be derived from MCLK. The division ratio is 1:512 (FSx:MCLK). Each FSx input must have a pulse present at the start of the desired active output time slot. Pulses on the various FSx inputs must be separated by one or more integer multiples of time slots. An internal pull-down device is included on each FSx.
ASEL	6	I^d	**A-Law Select.** This pin must be tied to VDD for A-law operation.
FSEP	1	I	**Frame Sync Separation.** The pulse width of this 8 kHz signal defines the timing offset between the transmit and receive frames. Internally generated receive frame sync pulses are delayed from the corresponding transmit frame sync pulse rising edge by one less than the FSEP pulse width in negative MCLK edges. If the pulse width is one MCLK period or less, the transmit and receive frame sync are made coincident. Loss of FSEP causes the device to powerdown. At the master clock frequency of 4.096 MHz, delays of 511 clock pulses are not allowed. Timing relationships between FSEP, FSxN , and time slot zero are given in Figures 5—6.

* I^d indicates that pull-down device is included on this lead.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature Range	T_{stg}	–55	150	°C
Power Supply Voltage	V_{DD}	—	6.5	V
Voltage on Any Pin with Respect to Ground	—	–0.5	0.5 + V_{DD}	V
Maximum Power Dissipation (package limit)	P_{DISS}	—	600	mW

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies Microelectronics Group employs a human-body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

HBM ESD Threshold Voltage	
Device	**Rating**
T5504 - - 1MC2	>2000 V

Electrical Characteristics

Specifications apply for T_A = 0 °C to 70 °C, V_{DD} = 5 V ± 5%, MCLK = 4.096 MHz, and GND = 0 V, unless otherwise noted.

dc Characteristics

Table 2. Digital Interface

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	All digital inputs	—	—	0.8	V
Input High Voltage	V_{IH}	All digital inputs	2.0	—	—	V
Output Low Voltage	V_{OL}	Dx, I_L = 3.2 mA	—	—	0.4	V
Output High Voltage	V_{OH}	Dx, I_L = –3.2 mA	2.4	—	—	V
		Dx, I_L = –320 µA	3.5	—	—	V
Input Current, Pins without Pull-down	I_I	Any digital input GND < V_{IN} < V_{DD}	–10	—	10	µA
Input Current, Pins with Pull-down	I_I	Any digital input GND < V_{IN} < V_{DD}	—	—	150	µA
Output Current in High-impedance State	I_{OZ}	Dx	–30	—	30	µA
Input Capacitance	C_I	—	—	—	5	pF

Electrical Characteristics (continued)

dc Characteristics (continued)

Table 3. Power Dissipation

Power measurements are made at MCLK = 4.096 MHz, outputs unloaded.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Powerdown Current	I_{DDO}	MCLK present, FSx[3:0] = 0.4 V, FSEP = 0.4 V	—	0.2	1	mA
Powerup Current	I_{DD1}	MCLK, FSx[3:0], FSEP present	—	30	50	mA
Standby Current	I_{DDS}	MCLK, FSEP present; FSx[3:0] = 0.4 V	—	6	10	mA

Transmission Characteristics

Table 4. Analog Interface

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Resistance, VFxIN	R_{VFXI}	0.25 V < VFxI < 4.75 V	1.0	—	—	MΩ
Input Leakage Current, VFxIN	I_{BVFXI}	0.25 V < VFxI < 4.75 V	—	—	2.4	µA
dc Open-loop Voltage Gain, GSx	A_{VOL}	—	5000	—	—	—
Open-loop Unity Gain Bandwidth, GSx	fo	—	1	3	—	MHz
Load Capacitance, GSx	CL_{X1}	—	—	—	50	pF
Load Resistance, GSx	RL_{X1}	—	10	—	—	kΩ
Input Voltage, VFxIN	V_{IX}	Relative to ground	2.3	2.4	2.5	V
Load Resistance, VFRO	RL_{VFrO}	—	2000	—	—	Ω
Load Capacitance, VFRO	CL_{VFrO}	—	—	—	100	pF
Output Resistance, VFRO	RO_{VFrO}	0 dBm0, 1020 Hz PCM code applied to DR	—	—	20	Ω
		Partial powerdown FSx = 0 for channel under test	3000	—	10000	Ω
Output Voltage, VFRO	V_{OR}	Alternating ± zero PCM code applied to DR	2.25	2.35	2.5	V
Output Voltage, VFRO, Standby	VO_{RPD}	FSX[3:0] = 0.4 V, FSEP = active, no load	2.15	2.4	2.65	V
Output Leakage Current, VFRO, Powerdown	IO_{VFRO}	FSEP = 0.4 V	–30	—	30	µA
Output Voltage Swing, VFRO	V_{SWR}	RL = 2000 Ω	3.2	—	—	V_{PP}

Transmission Characteristics (continued)

ac Transmission Characteristics

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave; the input amplifier is set for a gain of 4 (12 dB). The digital input is a PCM bit stream equivalent to that obtained by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. The output level is sin(x)/x-corrected.

Table 5. Absolute Gain

T_A = 25 °C, V_{DD} = 5.0 V, except as noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Encoder Absolute Gain	EmW	Signal input of 0.194 Vrms (–12 dBm0), 1020 Hz	–0.25	—	0.25	dBm0
Encoder Absolute Gain Variation	ΔEmWT	Signal input of 0.194 Vrms (–12 dBm0), 1020 Hz, temp 0 °C to 70 °C	–0.03	—	0.03	dB
Encoder Absolute Gain Variation	ΔEmWV	Signal input of 0.194 Vrms (–12 dBm0), 1020 Hz, V_{DD} = 5 V ± 5%	–0.03	—	0.03	dB
Decoder Absolute Gain	DmW	PCM input of 0.775 Vrms, 1020 Hz, RL = 10 kΩ	–0.25	—	0.25	dBm0
Decoder Absolute Gain Variation	ΔDmWT	PCM input of 0.775 Vrms, 1020 Hz, RL = 10 kΩ, temp 0 °C to 70 °C	–0.03	—	0.03	dB
Decoder Absolute Gain Variation	ΔDmWV	PCM input of 0.775 Vrms, 1020 Hz, RL = 10 kΩ, V_{DD} = 5 V ± 5%	–0.03	—	0.03	dB

Table 6. Gain Tracking

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit Gain Tracking Error Sinusoidal Input A-Law	GT_X	+3 dBm0 to –40 dBm0 –40 dBm0 to –50 dBm0	–0.25 –0.60	— —	0.25 0.60	dB dB
Receive Gain Tracking Error Sinusoidal Input A-Law	GT_R	+3 dBm0 to –40 dBm0 –40 dBm0 to –50 dBm0	–0.25 –0.60	— —	0.25 0.60	dB dB

Table 7. Distortion

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit Signal to Distortion	SD_X	A-law 3 dBm0 ≤ VF_XI ≤ –30 dBm0	35	—	—	dB
		A-law –30 dBm0 ≤ VF_XI ≤ –40 dBm0	29	—	—	dB
		A-law –40 dBm0 ≤ VF_XI ≤ –45 dBm0	25	—	—	dB
Receive Signal to Distortion	SD_R	A-law 3 dBm0 ≤ VF_RO ≤ –30 dBm0	35	—	—	dB
		A-law –30 dBm0 ≤ VF_RO ≤ –40 dBm0	29	—	—	dB
		A-law –40 dBm0 ≤ VF_RO ≤ –45 dBm0	25	—	—	dB
Single Frequency Distortion, Transmit	SFD_X	200 Hz—3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz	—	—	–38	dBm0
Single Frequency Distortion, Receive	SFD_R	200 Hz—3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz	—	—	–40	dBm0
Intermodulation Distortion	IMD	Transmit or receive, two frequencies in the range (300 Hz—3400 Hz) at –6 dBm0	—	—	–42	dBm0

Transmission Characteristics (continued)

ac Transmission Characteristics (continued)

Table 8. Envelope Delay Distortion

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Tx Delay, Absolute*	DXA	f = 1600 Hz	—	—	175 to 425	µs
Tx Delay, Relative to 1600 Hz	DXR	f = 500 Hz—600 Hz	—	—	220	µs
		f = 600 Hz—800 Hz	—	—	145	µs
		f = 800 Hz—1000 Hz	—	—	75	µs
		f = 1000 Hz—1600 Hz	—	—	40	µs
		f = 1600 Hz—2600 Hz	—	—	75	µs
		f = 2600 Hz—2800 Hz	—	—	105	µs
		f = 2800 Hz—3000 Hz	—	—	155	µs
Rx Delay, Absolute*	DRA	f = 1600 Hz	—	—	150 to 405	µs
Rx Delay, Relative to 1600 Hz	DRR	f = 500 Hz—1000 Hz	–40	—	—	µs
		f = 1000 Hz—1600 Hz	–30	—	—	µs
		f = 1600 Hz—2600 Hz	—	—	90	µs
		f = 2600 Hz—2800 Hz	—	—	125	µs
		f = 2800 Hz—3000 Hz	—	—	175	µs
Round Trip Delay, Absolute*	DRTA	Any time slot/channel to f = 1600 Hz	—	—	325 to 650	µs

* Varies as a function of time slots chosen.

Overload Compression

Figure 4 shows the region of operation for encoder signal levels above the reference input power (0 dBm0).

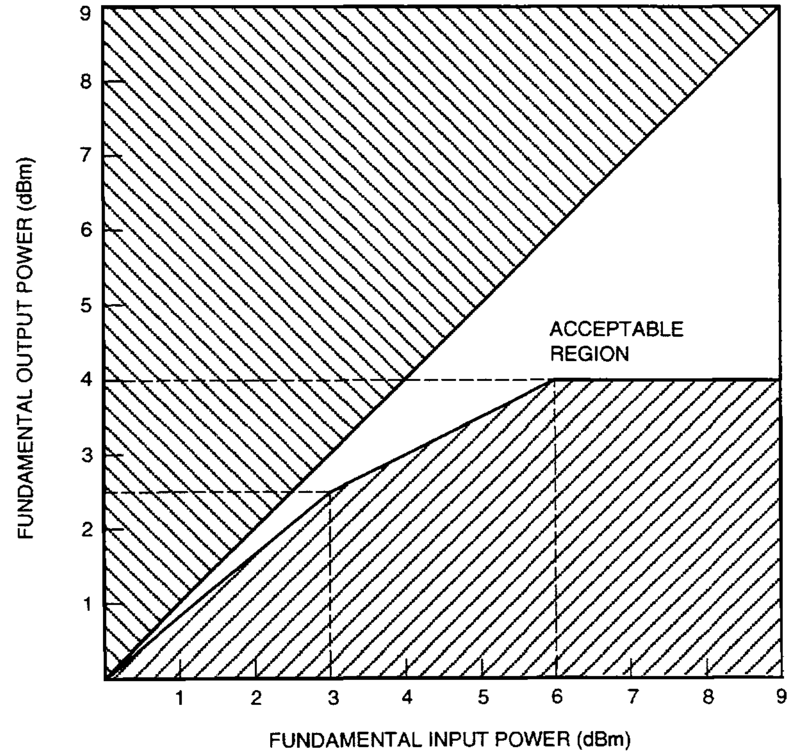

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Figure 4. Overload Compression

Transmission Characteristics (continued)

ac Transmission Characteristics (continued)

Table 9. Noise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit Noise A-Law	NXP	Input amplifier gain = 4 (12 dB)	—	—	–68	dBm0p
Receive Noise A-Law	NRP	PCM code is A-law positive one.	—	—	–75	dBm0p
Noise, Single Frequency f = 0 kHz—100 kHz	NRS	VFxIN = 0 Vrms, measurement at VFRO, DR = Dx	—	—	–53	dBm0
Power Supply Rejection Transmit	PSRx	VDD = 5.0 Vdc + 100 mVrms:				
		f = 0 kHz—4 kHz	36	—	—	dB
		f = 4 kHz—50 kHz	30	—	—	dB
Power Supply Rejection Receive	PSRx	PCM code is positive one LSB. VDD = 5.0 Vdc + 100 mVrms:				
		f = 0 kHz—4 kHz	36	—	—	dB
		f = 4 kHz—25 kHz	40	—	—	dB
		f = 25 kHz—50 kHz	30	—	—	dB
Spurious Out-of-Band Signals at VFRO Relative to Input	SOS	0 dBm0, 300 Hz—3400 Hz input PCM code applied:				
		4600 Hz—7600 Hz	—	—	–30	dB
		7600 Hz—8400 Hz	—	—	–40	dB
		8400 Hz—50 kHz	—	—	–30	dB

Table 10. Receive Gain Relative to Gain at 1.02 kHz

Frequency (Hz)	Min	Typ	Max	Unit
Below 3000	–0.35	±0.04	0.35	dB
3140	–0.75	±0.04	0.20	dB
3380	–0.885	–0.58	0.010	dB
3860	—	–10.7	–9.4	dB
4600 and above	—	—	–28	dB

Table 11. Transmit Gain Relative to Gain at 1.02 kHz

Frequency (Hz)	Min	Typ	Max	Unit
16.67	—	–50	–30	dB
40	—	–34	–26	dB
50	—	–36	–30	dB
60	—	–50	–30	dB
200	–1.8	–0.5	0	dB
300 to 3000	–0.35	±0.04	0.35	dB
3140	–0.75	±0.04	0.20	dB
3380	–0.885	–0.58	0.010	dB
3860	—	–10.7	–9.4	dB
4600 and above	—	—	–32	dB

Transmission Characteristics (continued)

ac Transmission Characteristics (continued)

Table 12. Interchannel Crosstalk (Between Channels) RF = TBD (See Note.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit to Receive Crosstalk 0 dBm0 Transmit Levels	CTXX-RY	f = 300 Hz—3400 Hz idle PCM code for channel under test; 0 dBm0 into any other single channel VFxIN	—	—	–75	dB
Receive to Transmit Crosstalk 0 dBm0 Receive Levels	CTRX-XY	f = 300 Hz—3400 Hz VFxIN = 0 Vrms for channel under test; 0 dBm0 code level on any other single channel DR	—	—	–75	dB
Transmit to Transmit Crosstalk 0 dBm0 Transmit Levels	CTXX-XY	f = 300 Hz—3400 Hz 0 dBm0 applied to any single channel VFxIN except channel under test, which has VFxIN = 0 Vrms	—	—	–75	dB
Receive to Receive Crosstalk 0 dBm0 Receive Levels	CTRX-RY	f = 300 Hz—3400 Hz 0 dBm0 code level on any single channel DR except channel under test which has idle code applied	—	—	–75	dB

Table 13. Intrachannel Crosstalk (Within Channels) RF = TBD (See Note.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit to Receive Crosstalk 0 dBm0 Transmit Levels	CTXX-RX	f = 300 Hz—3400 Hz idle PCM code for channel under test; 0 dBm0 into VFxIN	—	—	–65	dB
Receive to Transmit Crosstalk 0 dBm0 Receive Levels	CTRX-XX	f = 300 Hz—3400 Hz VFxIN = 0 Vrms for channel under test; 0 dBm0 code level on DR	—	—	–65	dB

Note: For Tables 12 and 13, crosstalk into the transmit channels (VFxIN) can be significantly affected by parasitic capacitive feeds from GSx and VFRO outputs. PWB layouts should be arranged to keep these parasitics low. The resistor value of RF (from GSx to VFxIN) should also be kept as low as possible (while maintaining the load on GSx above 10 kΩ per Table 4) to minimize crosstalk.

Timing Characteristics

Table 14. Clock Section (See Figures 5 and 6.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tMCHMCL1	Clock Pulse Width	—	97	—	—	ns
tCDC	Duty Cycle, MC	—	40	—	60	%
tMCH1MCH2 tMCL2MCL1	Clock Rise and Fall Time	—	0	—	15	ns

Table 15. Transmit Section (See Figure 5.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tFSHDV	Data Enabled on TS Entry	0 < CLOAD < 100 pF	0	—	80	ns
tMCHDV1	Data Delay from FSx	0 < CLOAD < 100 pF	0	—	60	ns
tMCHDZ[1]	Data Float on TS Exit	CLOAD = 0	0	—	30	ns
tFSHMCL	Frame-sync Delay High	—	50	—	195	ns
tFSLMCL	Frame-sync Delay Low	—	50	—	195	ns

[1] Timing parameter tMCHDZ is referenced to a high-impedance state.

Timing Characteristics (continued)

Table 16. Receive Section (See Figure 6.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
tDVMCL	Receive Data Setup	—	30	—	—	ns
tMCLDV	Receive Data Hold	—	15	—	—	ns
tSPHMCL	Frame Separation Delay High	—	50	—	195	ns
tSPLMCL	Frame Separation Delay Low	—	50	—	195	ns

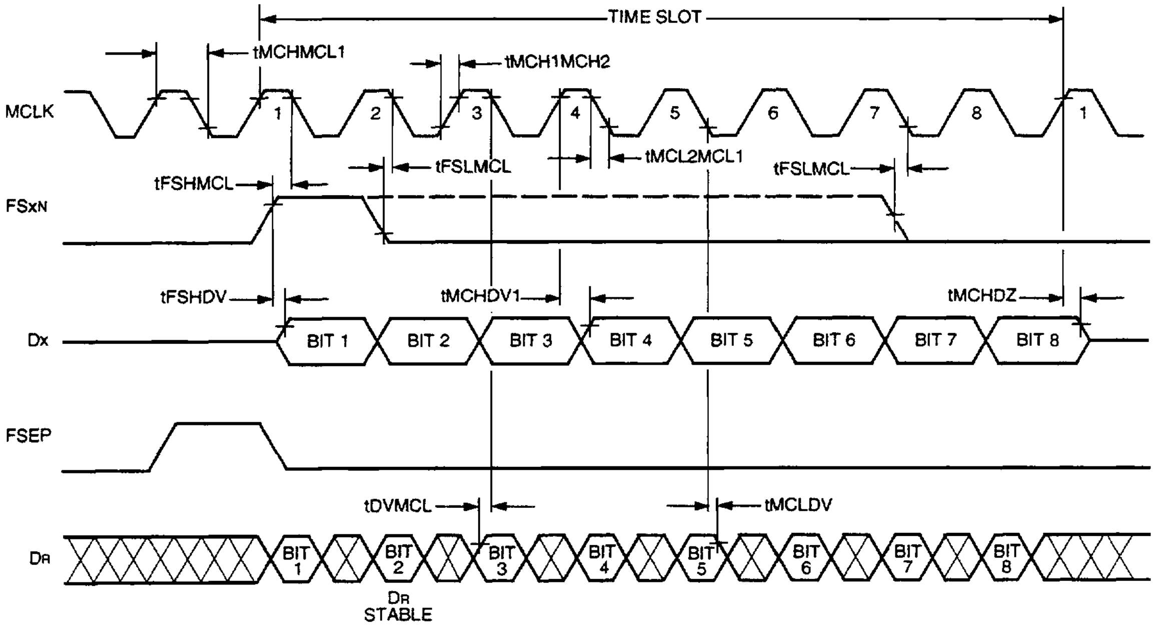

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Figure 5. T5504 - - 1MC2 Transmit and Receive Timing, FSEP = 1 MCLK

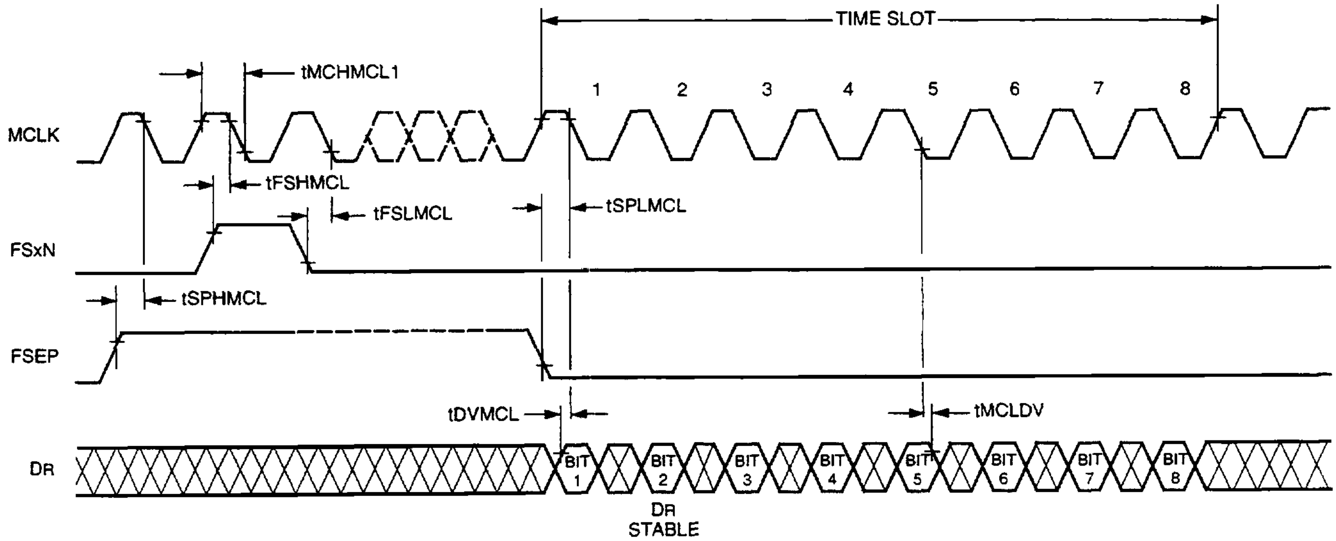

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Figure 6. T5504 - - 1MC2 Receive Timing, FSEP > 1 MCLK

Timing Characteristics (continued)

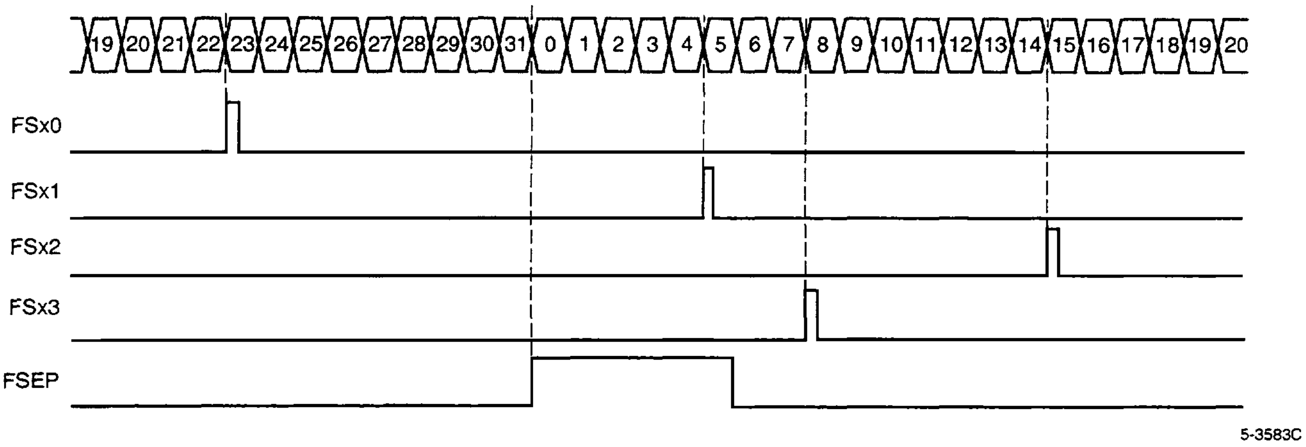


Figure 7. Typical Frame Sync Timing, FSEP = 1 MCLK

Applications

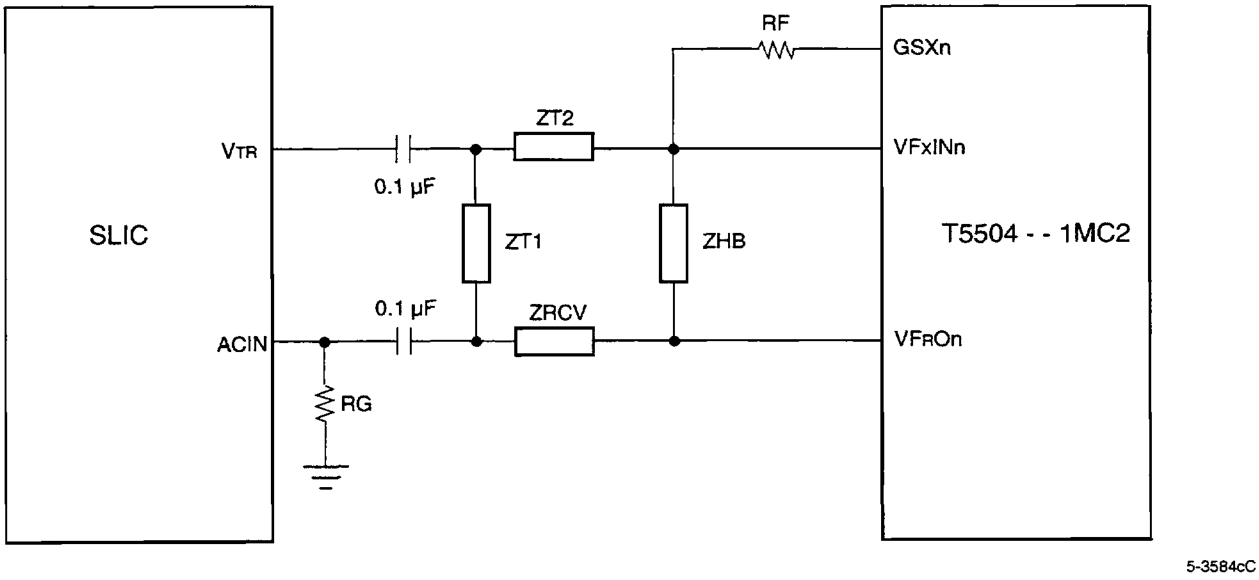
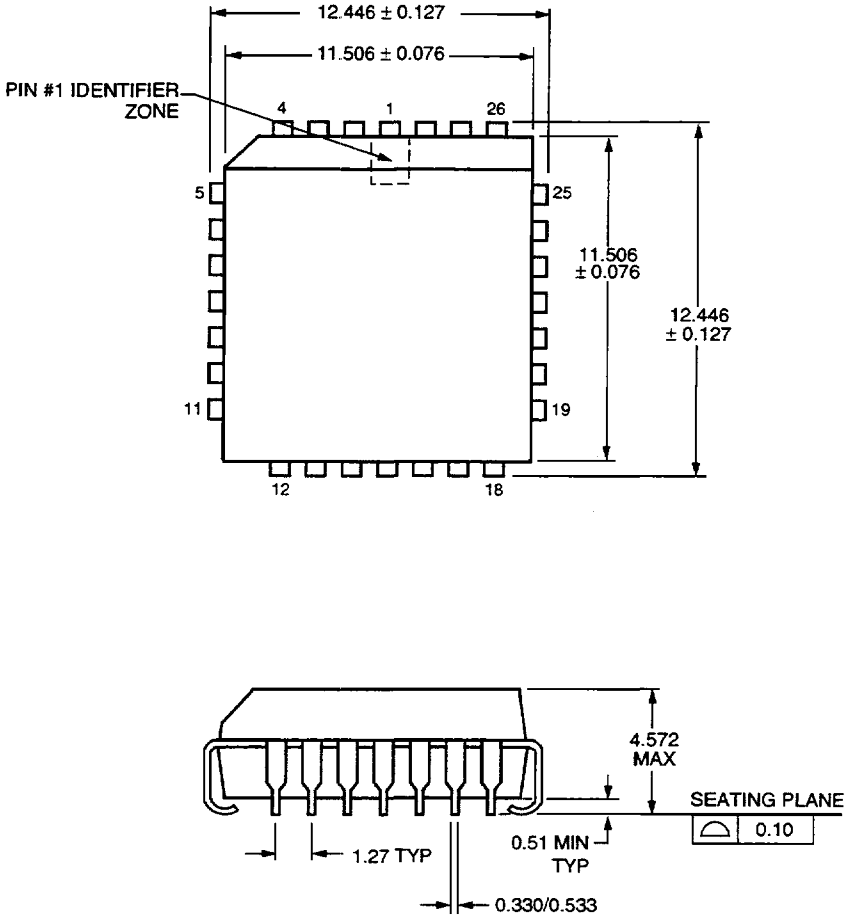


Figure 8. Typical T5504 - - 1MC2/SLIC Interconnection

Outline Diagrams

28-Pin PLCC

Controlling dimensions are in inches.



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Ordering Information

Device Code	Package	Temperature
T5504 - - 1MC2	28-Pin PLCC	0 °C to 70 °C

For additional information, contact your Microelectronics Group Account Manager or the following:
INTERNET: **http://www.lucent.com/micro**
U.S.A.: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18103
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February 1997
DS97-139ALC (Replaces DS96-220ALC)

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