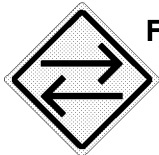


10BASE-T Ethernet Transceiver With On Chip Filters and Digital Interface

PRELIMINARY

February 20, 1997

SEEQ Full Duplex Designation



Full Duplex

Symbol identifies product as Full Duplex device.

Features

- **Integrated 10BASE-T Transceiver With Output Waveshaping And On Chip Filters**
- **Few External Components**
- **Flexible Digital Hub Interface: Clocked or Nonclocked, Single Ended or Differential**
- **Meets All Applicable IEEE 802.3 and 10BASE-T Standards**
- **Jitter Attenuation On Digital Input**
- **Parallel Status Port**
- **Many User Features And Options**
 - Full Duplex Mode
 - Autopolarity
 - Smart Squelch
 - Adjustable Transmit Level
 - Link Disable
- **Receive Data Valid Output**
- **Status Outputs**
 - Link
 - Jabber
- **20 Pin PLCC**

Note: Check for latest Data Sheet revision before starting any designs.

Call SEEQ Technology (510) 226-2915.

— or —

SEEQ Data Sheets are now on the Web, access SEEQ Home Page www.seeq.com.

Description

The 83C96 is a highly integrated analog interface IC for twisted pair Ethernet applications (10BASE-T).

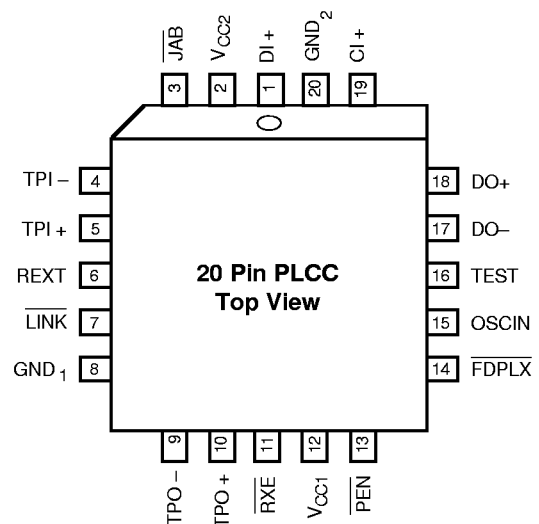
The device consists of transmit waveshaping circuitry, transmit filter, twisted pair line driver, receive filter, twisted pair receiver, and a flexible digital interface to an external hub or another device.

The addition of internal output waveshaping circuitry and on-chip filters eliminates the need for external filters and common mode chokes normally required in 10BASE-T applications.

The 83C96 is ideal as a media interface for 10BASE-T hubs and can also be used for adapter cards.

The 83C96 is implemented in CMOS technology.

Pin Configuration



Pin Description

| Pin No. | Name | I/O | Description |
|---------|------------------|---------------|--|
| 1 | DI+ | O | Digital Transmit Output. This pin transmits receive TP data. |
| 2 | V _{CC2} | -- | Positive Supply. 5V ± 5% |
| 3 | JAB | O Pullup | Jabber Detect output. This pin consists of an open drain output transistor with a resistor pullup. The pin is a Jabber Detect output and can drive an LED. $\overline{\text{JAB}} = 1$ Output Jabber Not Detected $\overline{\text{JAB}} = 0$ Output Jabber Detected |
| 4 | TPI- | I | Twisted Pair Receive Input, Negative |
| 5 | TPI+ | I | Twisted Pair Receive Input, Positive |
| 6 | REXT | -- | Transmit Current Set. An external resistor connected between this pin and GND will set the output current supplied on TPO+, TPO-. |
| 7 | LINK | I/O Pullup | Link Status Output and Link Disable Input. This pin consists of an open drain output transistor with a resistor pullup. To disable the link test function, tie the pin to GND. Otherwise, the pin is a Link Detect output, can drive an LED, and blinks when asserted $\overline{\text{LINK}} = 1$ Output Link Pulse Not Detected $\overline{\text{LINK}} = 0$ Output Link Pulse Detected $\overline{\text{LINK}} = \text{GND}$ Input Disable Link Pulse |
| 8 | GND ₁ | -- | Negative Supply. 0V |
| 9 | TPO- | O | Twisted Pair Transmit Output, Negative |
| 10 | TPO+ | O | Twisted Pair Transmit Output, Positive |
| 11 | RXE | O | Receive Data Valid Output $\overline{\text{RXE}} = 1$ No Receive Data $\overline{\text{RXE}} = 0$ Receive Data Valid |
| 12 | V _{CC1} | -- | Positive Supply. 5V ± 5% |
| 13 | PEN | I Pulldown | Port Enable Input. This pin enables the twisted pair transmitter. $\overline{\text{PEN}} = 1$ TP Transmitter Disabled $\overline{\text{PEN}} = 0$ TP Transmitter Enabled |
| 14 | FDPLX | I Pullup | Full Duplex Enable Input with a resistor pullup. To force the device into the Full Duplex Mode, tie this pin to GND. $\overline{\text{FDPLX}} = 1$ Half Duplex Mode $\overline{\text{FDPLX}} = 0$ Full Duplex Mode Enabled |

Pin Description (continued)

| PinNo. | Name | I/O | Description |
|--------|------------------|---------------|--|
| 15 | OSCIN | I | Clock oscillator input. There must be either a 20 MHz crystal or a 20 MHz clock tied between this pin and GND. |
| 16 | TEST | I Pulldown | Test input. Reserved for factory test. Leave floating or tie to GND. |
| 17 | DO- | I | Digital Receive Input, Negative. This pin also selects the receive digital interface mode. DO- = 1 DO+ is single ended, clocked DO- = 0 DO+ is single ended, nonclocked DO- = Data DO± is differential, nonclocked |
| 18 | DO+ | I | Digital Receive Input, Positive. |
| 19 | CI+ | O | Digital Collision Output. |
| 20 | GND ₂ | -- | Negative Supply. 0 V |

Functional Description**General**

The 83C96 has five main sections: digital transmitter, digital receiver, twisted pair transmitter, twisted pair receiver, and miscellaneous.

The digital receiver receives incoming Manchester encoded data from an external hub controller or another device and converts the data to internal digital levels.

The data then goes to the twisted pair transmitter. The TP transmitter is composed of special circuitry to remove excess jitter, a waveform generator that preshapes the output, a filter to remove high frequency components, and an output driver to drive the 100 ohm twisted pair cable. In addition, the transmitter generates link pulses, start of idle pulses (SOI), and detects the jabber condition.

The twisted pair receiver receives incoming Manchester encoded data from the twisted pair cable, removes high frequency noise from the input, determines if the input signal is a valid packet, and then converts the data from twisted pair levels to internal digital levels. The twisted pair receiver also detects link pulses, detects start of idle (SOI) pulses, detects and corrects for reverse polarity on the twisted pair inputs, and implements a squelch algorithm to reject invalid signals.

The output of the twisted pair receiver then goes to the digital transmitter which drives the data to an external hub controller or another device. There is a second digital transmitter for collision.

The miscellaneous blocks are the crystal oscillator, collision detect circuitry, digital select inputs, and digital status outputs.

Each block plus the operating modes are described in more detail in the following sections. A block diagram of the 83C96 is shown in Figure 1.

Twisted Pair Transmitter**TP Transmit**

The transmitter consists of a jitter attenuator, waveform generator, and line driver.

The jitter attenuator is designed to reduce the jitter that was present on the digital receive input. The jitter attenuation factor is typically 0.2, that is, only 20% of the jitter that is present on the digital input propagates to the twisted pair output. This block also synchronizes the digital receiver data transitions to the waveform generator clock.

The purpose of the waveform generator is to preshape the transmit output pulse. The waveform generator consists of a ROM, DAC, clock generator, and filter. The DAC generates a stair-stepped representation of the desired output waveform. The stair-stepped DAC output then goes through a second order low pass filter in order to "smooth" the DAC output and remove any high frequency component. The DAC values are determined from the

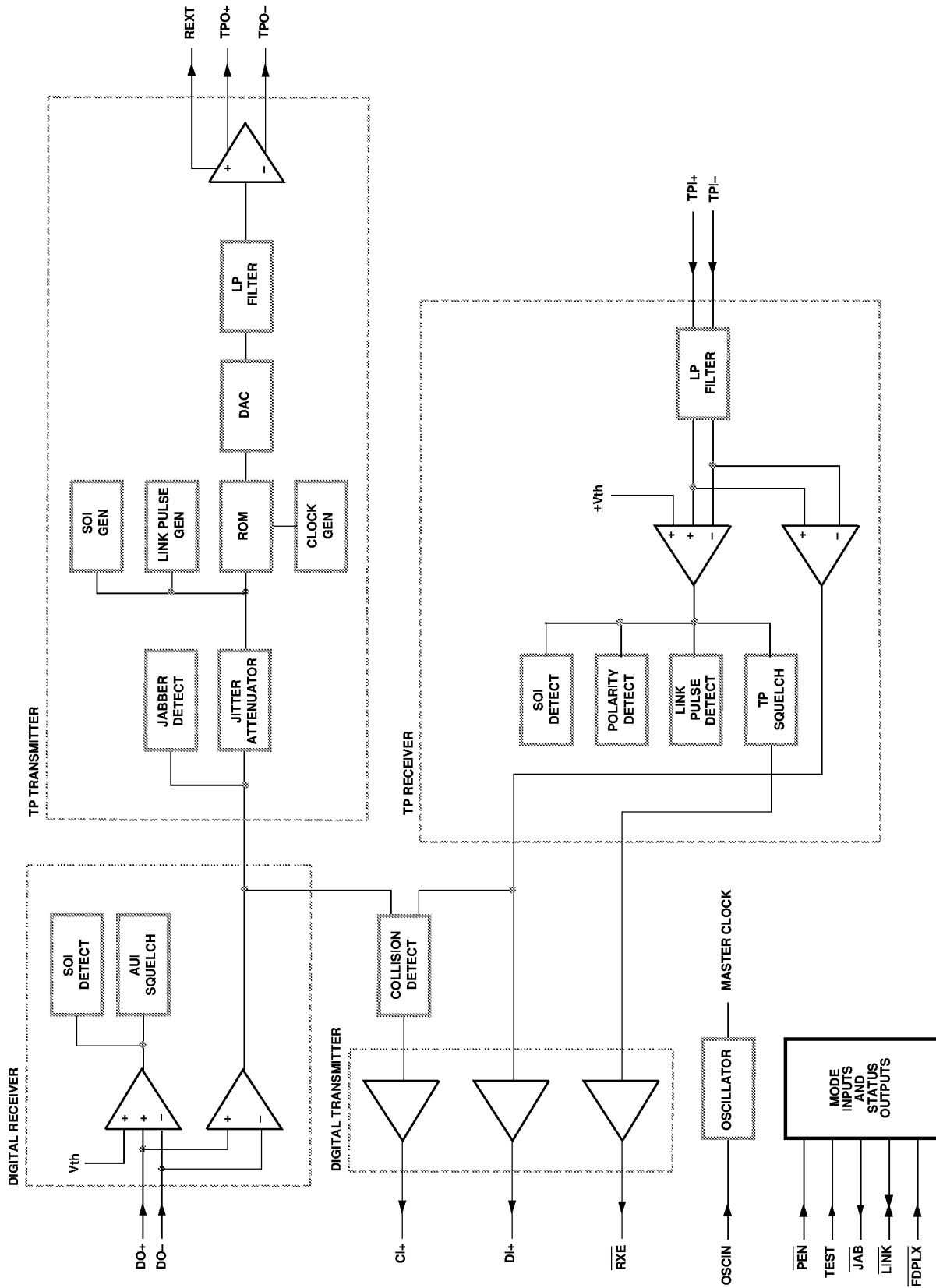


Figure 1. 83C96 Block Diagram

ROM addresses; the ROM addresses are chosen to shape the pulse to the desired template and are clocked into the DAC at high speed by the clock generator. In this way, the waveform generator preshapes the output waveform transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3 Section 14 and also shown in Figure 2.

The waveshaper replaces and eliminates external filters on the TP transmit output.

The line driver converts the preshaped and smoothed waveform to a current output that can drive the twisted pair cable directly without any external filters.

The 83C96 has special circuitry to reduce common mode noise on the twisted pair output. Common mode chokes may not be needed to meet emissions requirements in most applications.

During the idle period, no output signal is transmitted on TPO_{\pm} (except link pulse), but the current sources still remain active, thus eliminating glitches at the beginning and end of packet.

TP Receiver

TP Receive

The TP receiver is intended to receive input signals from the twisted pair cable that reside inside the template shown in Figure 3.

The TPI_{\pm} inputs are internally biased to $VCC/3$ by internal 10K bias resistors. The TPI_{\pm} inputs pass through a 3rd order low pass filter designed to eliminate high frequency noise on the input.

The receive filter output then goes to two different types of receive comparators, threshold and zero crossing. The threshold comparator determines whether the signal is valid, and the zero crossing comparator is used to sense the actual data transitions once the signal is determined to be valid data. The output of the threshold comparator is used for squelch, link pulse detect, SOI detect, and reverse polarity detect. Each of these are described in separate sections. The output of the zero crossing comparator goes to the digital transmitter.

TP Squelch

The threshold comparator compares the TPI_{\pm} inputs against fixed positive and negative thresholds, called squelch levels. The output from the threshold comparators goes to a receive squelch circuit which determines if the receive input data is valid. If the data is invalid, the receiver is in the squelched state. If the input voltage exceeds the squelch levels for three bit times with alternating polarity within a 100 - 250 ns interval, the data is considered to be valid and the receiver now enters into the unsquelch state. In the unsquelch state, the receive threshold level is reduced by approximately 30% for noise immunity reasons and is called the unsquelch level. While in the unsquelch state, the receive squelch circuit looks for SOI (Start Of Idle) pulse at the end of a packet. When the SOI signal is detected, the receive squelch is turned on again. The receiver meets the squelch requirements defined in IEEE 802.3 Section 14.

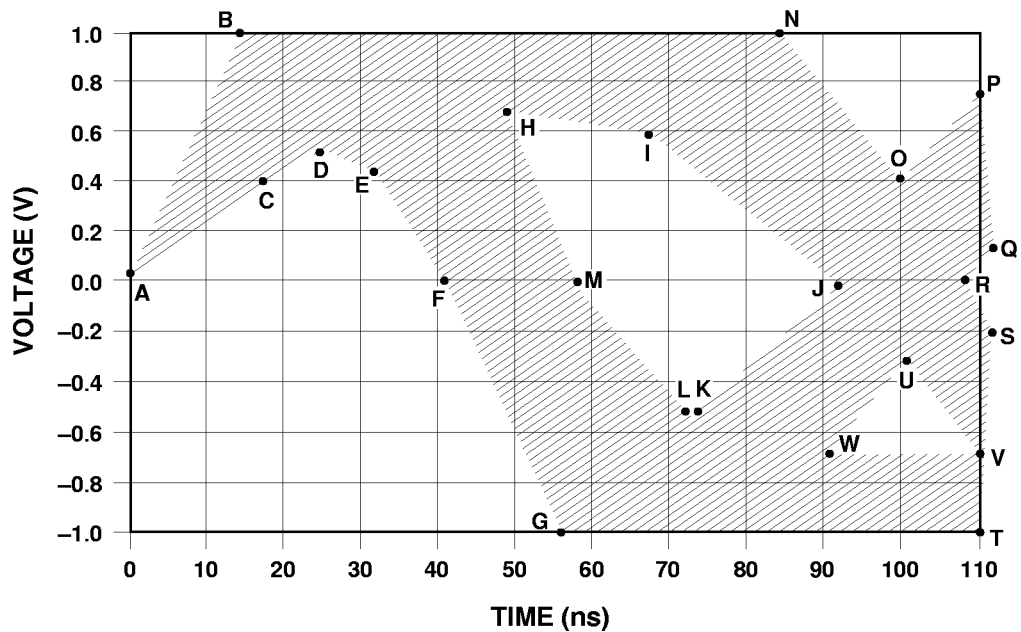


Figure 2. Twisted Pair Output Voltage Template with IEEE 802.3 Line Model.

Voltage Template Values for Figure 2

| Reference | Time (ns) Internal MAU | Voltage (V) |
|-----------|---------------------------|-------------|
| A | 0 | 0 |
| B | 15 | 1.0 |
| C | 15 | 0.4 |
| D | 25 | 0.55 |
| E | 32 | 0.45 |
| F | 39 | 0 |
| G | 57 | -1.0 |
| H | 48 | 0.7 |
| I | 67 | 0.6 |
| J | 89 | 0 |
| K | 74 | -0.55 |
| L | 73 | -0.55 |
| M | 61 | 0 |
| N | 85 | 1.0 |
| O | 100 | 0.4 |
| P | 110 | 0.75 |
| Q | 111 | 0.15 |
| R | 111 | 0 |
| S | 111 | -0.15 |
| T | 110 | -1.0 |
| U | 100 | -0.3 |
| V | 110 | -0.7 |
| W | 90 | -0.7 |

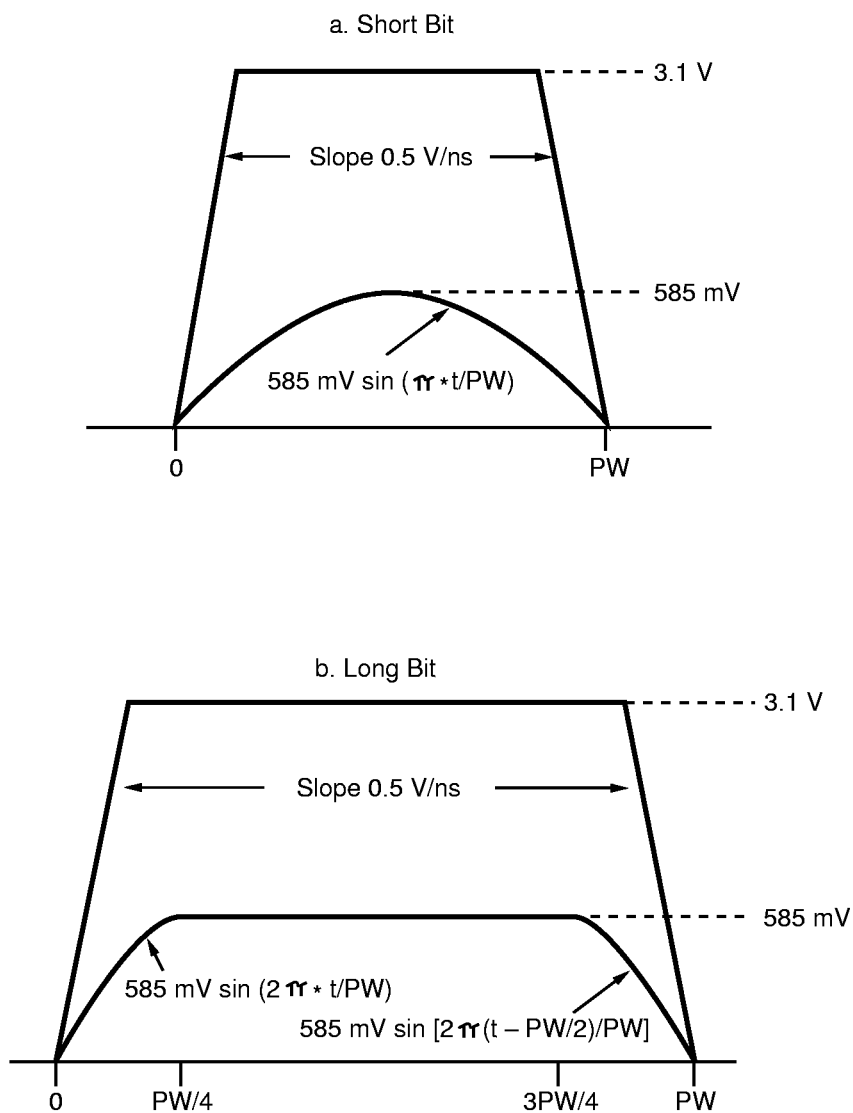


Figure 3. TP Receive Input Differential Voltage Template

Digital Transmitter

The digital transmitter consists of three digital output drivers: data, data valid and collision. The data output on pin $DI+$ contains a digital representation of the TP receive data. The data valid output on \overline{RXE} contains an active low signal that is asserted when the TP receive data is considered valid by the TP squelch circuit. The collision output on $CI+$ contains a 10 MHz square wave that is asserted when the collision condition is detected. The digital transmitter outputs are not affected by the receive interface mode selection.

Digital Receiver

The digital receive has three possible interface modes to an external hub controller or another device: differential, single ended non-clocked, and single ended clocked. The selection of the digital receiver interface mode is done with the pin $DO-$ as shown in Table 1.

Table 1. Digital Receiver Interface Mode Select

| Interface Mode | $DO+$ | $DO-$ |
|-------------------------|-------|-----------------|
| Differential | Data+ | Data- |
| Single Ended Nonclocked | Data | Tie To GND |
| Single Ended Clocked | Data | Tie To V_{CC} |

The differential interface mode is automatically sensed when there are transitions on both $DO+$ and $DO-$ data input pins. In this mode, data is inputted as differential digital signals on $DO+$ and $DO-$. The input voltage trip level on $DO\pm$ is set to zero volts, differential.

The single ended, non-clocked interface mode is selected by tying $DO-$ to GND and applying data to $DO+$. In this mode, data is inputted as a single ended signal on $DO+$. The input voltage trip level on $DO+$ is set to $V_{CC}/2$.

The single ended, clocked interface mode is selected by tying $DO-$ to VCC and applying data to $DO+$. In this mode, data is inputted as a single ended signal on $DO+$ and is clocked in on rising edges of the $OSCIN$ input clock. The input voltage trip level on $DO+$ is set to normal TTL levels.

In both the differential and single ended, nonclocked interface modes, the input data pulse width on $DO\pm$ must be at least 20 ns to be considered a valid data pulse.

SOI (Start of Idle)

The SOI pulse is a positive pulse inserted at the end of every transmitted packet to indicate the end of transmission and the start of idle.

Both the TP and digital transmitters must generate SOI pulses. The TP transmitted SOI output pulse is shaped by the transmit waveshaper to meet the pulse template requirements specified in IEEE 802.3 Section 14 and shown in Figure 4.

The receiver detects the SOI pulse by sensing missing data transition. Once the SOI pulse is detected, the device goes into the idle state.

Link Integrity

The TP transmitter generates link pulses during idle to indicate that the network link is intact. The transmitted link pulses are single positive pulses sent out at 8-24 ms intervals and are preshaped by the transmit waveform generator to meet the pulse template specified in IEEE 802.3 Section 14 and shown in Figure 5.

The TP receiver monitors the $TPI\pm$ pins continuously for valid data and link pulse activity. If neither data nor link pulses are detected, the 83C96 enters the Link Fail State, the TP transmit and digital transmit functions are disabled. For the device to exit the Link Fail State, three consecutive link pulses or one valid data packet need to be detected on the $TPI\pm$ inputs.

\overline{LINK} is an input/output pin that can be configured to be either a link pulse detect output or a link pulse disable input. This pin consists of an open drain output transistor with a resistor pullup. If the pin is tied to GND, the pin is configured as an input and the link pulse detect function is disabled. If the pin is not tied to GND, the pin is configured as an output and indicates that link pulses are being detected when it is driven low. This pin can drive an LED from VCC or it can drive another digital input.

Collision

Collision occurs whenever transmit and receive occur simultaneously on $TPO\pm$ outputs and $TPI\pm$ inputs. Collision is indicated on the 83C96 by transmitting a 10 MHz signal on the collision digital transmitter output, $CI+$. The 10Mhz collision signal is also asserted on $CI+$ when the jabber condition has been detected and when the SQE test is performed. Collision function is disabled if the device is in the Link Fail State.

Signal Quality Error (SQE)

The SQE test is disabled in the 83C96. Please refer to the 83C95 or 83C97 Data Sheets if this function is required.

Jabber

Jabber condition occurs when the transmit packet exceeds its maximum allowable length. When jabber is detected, the transmit outputs on TPO_{\pm} are forced to the idle state, collision is asserted, and \overline{JAB} is asserted.

\overline{JAB} is an output pin for jabber detection. This pin consists of an open drain output transistor with a resistor pullup.

This pin can drive an LED from VCC or it can drive another digital input.

Receive Polarity Correction

The polarity of the signal on the twisted pair receive input pins, TPI_{\pm} , is continuously monitored. If either 3 consecutive SOI or 3 consecutive link pulses indicate incorrect polarity on TPI_{\pm} , the polarity is internally determined to be incorrect. The 83C96 automatically corrects a detected reverse polarity condition.

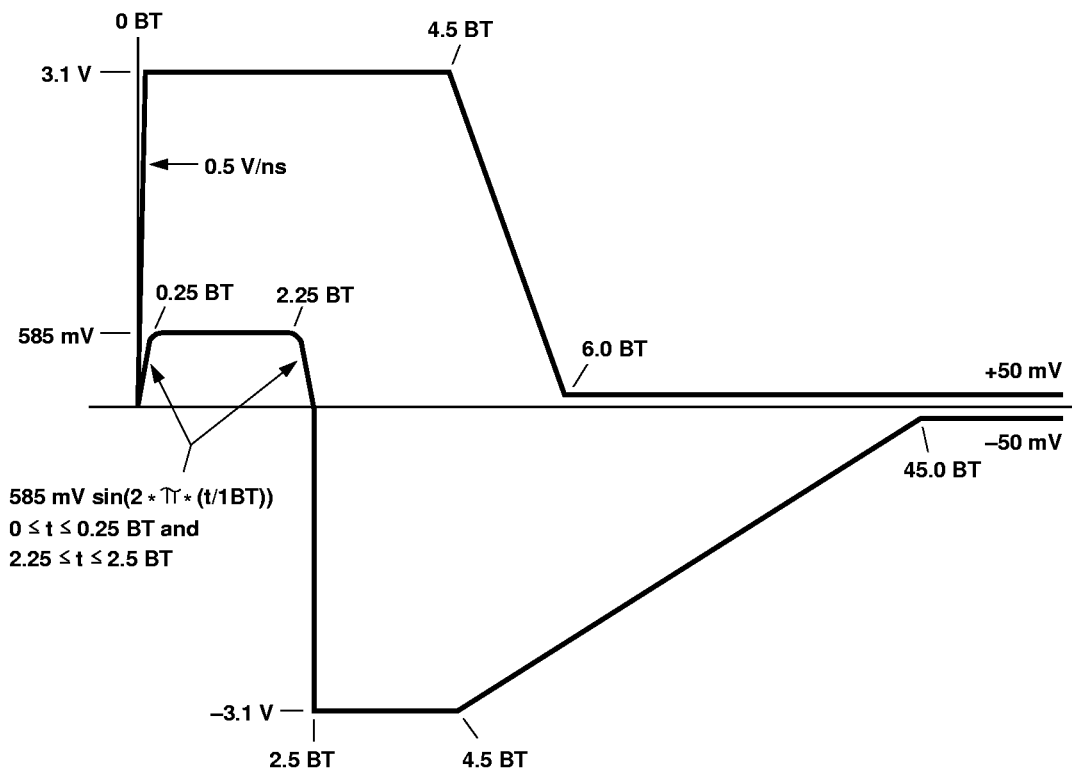


Figure 4. TP Transmit SOI Pulse Voltage Template

Full Duplex Mode

The 83C96 can be configured for full duplex mode. When the device is in the full duplex mode, transmission and reception can occur simultaneously because collision is disabled, and internal loopback is disabled.

The device can be forced into the full duplex mode. \overline{FDPLX} is a full duplex mode enable input. If the pin is tied to GND, the pin is configured as an input and full duplex mode is enabled. If the pin is left floating or connected to logic "1" the part goes into half duplex.

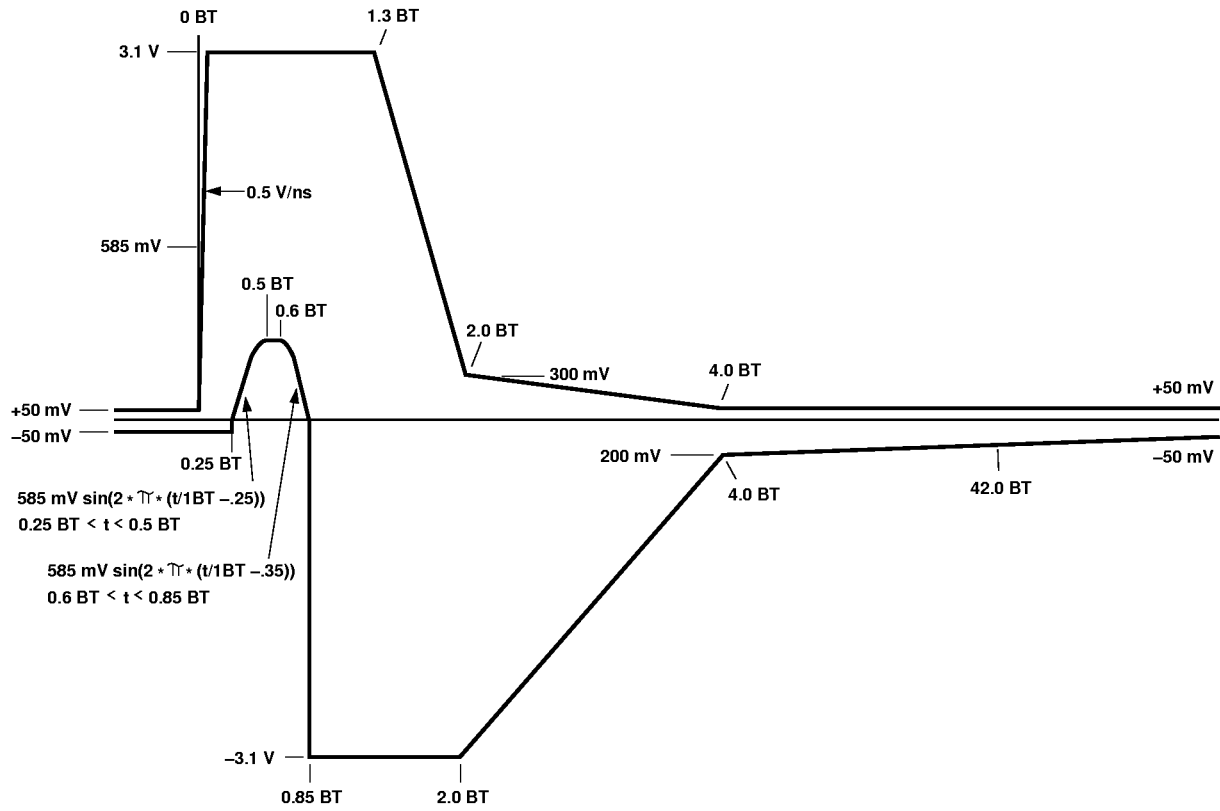


Figure 5. Transmit Link Pulse Voltage Template

APPLICATION INFORMATION

A typical example of the 83C96 in a hub application is shown in Figure 7. The device can also be used in other Ethernet applications provided that the interface to the device is digital.

TP Transmit Interface

The interface between the TP outputs on TPO± and the twisted pair cable requires a transformer and two resistors as shown in Figures 7.

The transformer for the TP transmitter is a 2:1 CT type. Sources for the TP interface transformer are listed in Table 2.

Table 2. TP Transformer Sources

| Vendor | Part Number | Telephone |
|---------------------------|--------------|----------------|
| Valor | PT4152 | (619) 537-2500 |
| Coilcraft | Q4430-A | (708) 639-6400 |
| PCA | EPE6047S | (818) 892-0761 |
| Bel Hybrids and Magnetics | A553-1084-01 | (201) 432-0463 |
| FEE Fil-Mag | 23Z435 | (619) 569-6577 |
| NANO Pulse | 000-6115-00 | (714) 529-2600 |

Two external 200 ohm 1% resistors are needed between VCC and TPO± to provide a 100 ohm termination impedance when looking back through the transformer from the twisted pair cable. This is shown in Figure 7.

The 83C96 has special circuitry to reduce common mode noise on the twisted pair output. Common mode chokes may not be needed to meet emissions requirements in most applications and have been eliminated from the application schematic in Figure 7.

To minimize noise pickup, the loading on TPO± should be minimized and both outputs should always be loaded equally.

TP Receive Interface

Receive data is typically transformer coupled into the receive inputs on TPI± and terminated with an external resistor as shown in Figure 7.

The receiver requires a 1:1 transformer. Sources for the TP interface transformer are listed in Table 2.

The receive input needs to be terminated with 98 ohms in order to meet input impedance requirements of IEEE

802.3 Section 14. Notice that in Figures 8, the receive input has this input termination resistor broken up into two 48.7 ohm 1% resistors with a 0.1 μF capacitor tied between the center points and GND. The optional 0.1 μF capacitor is needed if the device is required to meet the receive common mode input AC voltage specification in IEEE 802.3 Section 14. This capacitor attenuates common mode input noise. If the capacitor is not needed, then the two termination resistors can be combined into one 97.6 ohm 1% resistor across TPI±.

In order to minimize noise pickup into the receive path, loading on TPI± should be minimized and both inputs should be loaded equally.

TP Transmit Output Current Set

The TPO± output current level is set by an external resistor tied between REXT and GND. The output current is determined by the following equation:

$$I_{OUT} = (10K/R_{EXT}) * 50mA$$

R_{EXT} should be a 1% resistor in order to meet IEEE 802.3 specified levels.

The value of R_{EXT} should be ideally set to 10K to meet the templates and levels specified in Section 14 of IEEE 802.3. However, since the output is a current source, capacitive and inductive loading can reduce the output voltage level from the ideal. Thus, in actual application, it might be necessary to adjust the value of this resistor to compensate for the loading involved.

Keep the bias resistor as close to the REXT and GND pins as possible in order to reduce noise pickup into the transmitter.

Digital Transmitter Interface

The data on DI+ digital transmitter output is the digital representation of the data received on the TP receive inputs. The internal data path has been carefully laid out to minimize jitter on the data output. To keep the jitter low, the external parasitic load on DI+ should be kept to a minimum.

Since the data on DI+ is Manchester encoded, an external hub controller or other device can look at activity on DI+ to sense beginning of packet and detect SOI to sense end of packet. An alternative way to determine beginning and end of packet is to use the digital output, RXE. RXE is asserted at beginning of packet and deasserted at the end

of packet. Using RXE eliminates external circuitry needed to determine start and end of packet, and hence, when the data is valid.

Digital Receive Interface

The digital receiver has three interface types in order to offer a flexible digital interface to a hub controller or another device. The three different modes, as described in the Digital Receiver section, are differential, single ended clocked, and single ended non-clocked. The first two interface types, differential and single ended clocked, provide low jitter methods of transferring data from an external hub controller or other device to the 83C96. The last interface type, single ended non-clocked, is offered because of its simplicity even though it has higher jitter.

The differential interface mode is useful when complementary digital signals are available to the 83C96 on DO± from an external device. The internal data transition is detected when the difference between the DO+ and DO− input voltages crosses zero. This scheme eliminates the data jitter caused by unequal rise and fall times on the digital inputs.

Some external hub controllers or other devices might have only a single ended digital output signal for the data input on DO+. The single ended clocked interface mode allows the single ended digital input to be clocked into the device on the rising edge of a 20 MHz clock applied to OSCIN. Since the data on DO+ is clocked in on OSCIN rising edges, data jitter associated with the DO+ width variations and rise/fall times is eliminated.

The single ended non-clocked interface mode is the simplest interface mode on the 83C96. It has only a single digital input on DO+. Data presented on DO+ propagates directly through the device. This mode is the simplest but has greater jitter because the pulse width jitter and rise/fall time variations can directly propagate through to the TP transmit output. To reduce jitter on the input DO+, the input trip level is set at VCC/2, and a jitter attenuation circuit was placed inside the TP transmitter which reduces the input jitter by 80%, typically.

Oscillator

The 83C96 requires a 20Mhz reference frequency for internal signal generation. This 20Mhz reference frequency can be generated by either connecting an external crystal or an external clock between OSCIN and GND.

If the crystal oscillator is used, it needs only an external crystal. No other external capacitors or other components are required. The crystal must have the characteristics shown in Table 3. The crystal must be placed as close as possible to OSCIN and GND, keeping parasitics to a minimum.

Table 3. Crystal Specifications

| Parameter | Spec |
|------------------------------|-------------------|
| Type | Parallel Resonant |
| Frequency | 20 Mhz +/- 0.01% |
| Equivalent Series Resistance | 25 ohms max |
| Load Capacitance | 18 pF typ |
| Case Capacitance | 7 pF max |
| Power Dissipation | 1 mW max |

Power Supply Decoupling

There are two V_{CC} 's on the 83C96 (V_{CC1} and V_{CC2}) and two GND's (GND_1 and GND_2).

V_{CC1} and V_{CC2} should be connected together as close as possible to the device with a large V_{CC} plane.

GND_1 and GND_2 should also be connected together as close as possible to the device with a large ground plane.

A $0.1 \mu F$ decoupling capacitor should be connected between V_{CC1} and GND_1 as close as possible to the device pins, preferably within 0.5". The same should be repeated for V_{CC2} and GND_2 .

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limits beyond which may cause permanent damage to the device or affect device reliability. All voltages are specified with respect to GND_1 , GND_2 unless otherwise specified.

| | |
|---|--------------------------|
| V_{CC1} , V_{CC2} Supply Voltage | -0.3V to 6V |
| All Inputs and Outputs with Respect to GND | -0.3V to $V_{CC} + 0.3V$ |
| Package Power Dissipation | 1 Watt @ 70°C |
| Storage Temperature | -65° to +150°C |
| Temperature Under Bias | -10° to 80°C |
| Max. Lead Temperature (Soldering, 10 Sec) | 260°C |
| Max. Body Temperature (Soldering, 30 Sec) | 220°C |

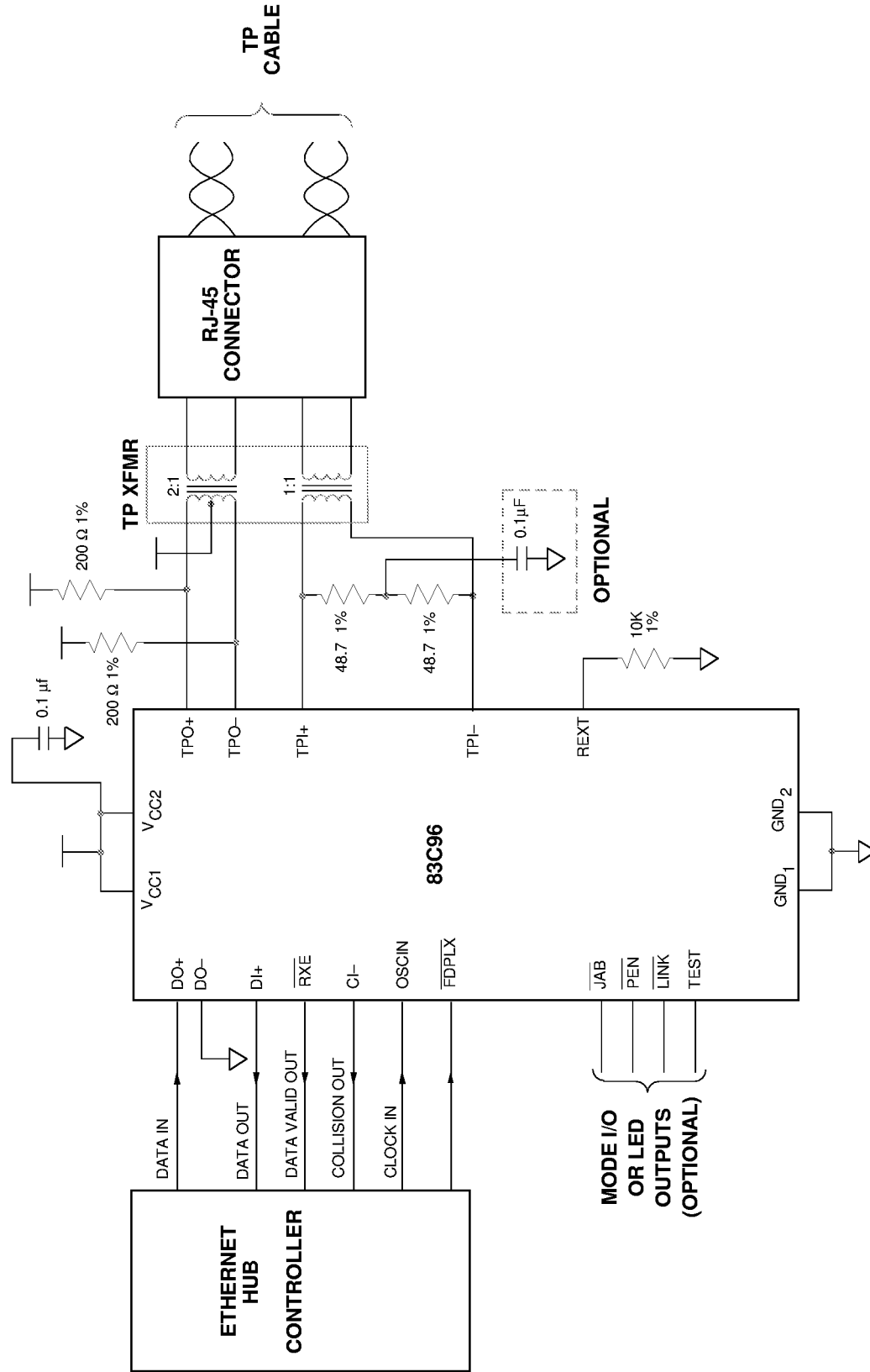


Figure 7. Hub Schematic Using 83C96

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all test conditions are as follows:

1. $T = 0 - 70^{\circ}\text{C}$
2. $V_{\text{CC}} = 5\text{V} \pm 5\%$
3. $20\text{ Mhz} \pm 0.01\%$
4. $\text{REXT} = 10\text{K} \pm 1\%$, no load

| SYM | PARAMETER | LIMIT | | | UNIT | CONDITIONS |
|-----------------|--------------------------------|-------|-----|------|---------------|--|
| | | MIN | TYP | MAX | | |
| V_{IL} | Input Low Voltage | | | 0.8 | Volt | All Except OSCIN, DO+ in Single Ended Nonclocked Mode |
| | | | | 1.5 | Volt | OSCIN |
| | | | | 2.0 | Volt | DO+ in Single Ended Nonclocked Mode |
| V_{IH} | Input High Voltage | 2.0 | | | Volt | All Except OSCIN, DO+ in Single Ended Nonclocked Mode |
| | | 3.5 | | | Volt | OSCIN |
| | | 3.0 | | | Volt | DO+ in Single Ended Nonclocked Mode |
| I_{IL} | Input Low Current | | | -1 | μA | $V_{\text{IN}} = \text{GND}$ $\overline{\text{PEN}}, \overline{\text{TEST}}, \text{DO}\pm$ |
| | | -15 | | -50 | μA | $V_{\text{IN}} = \text{GND}$ $\overline{\text{LINK}}, \overline{\text{FDPLX}}$ |
| | | | | -300 | μA | $V_{\text{IN}} = \text{GND}$ OSCIN |
| I_{IH} | Input High Current | | | 1 | μA | $V_{\text{IN}} = V_{\text{CC}}$ $\overline{\text{FDPLX}}, \text{DO}\pm, \overline{\text{LINK}}$ |
| | | 15 | | 50 | μA | $V_{\text{IN}} = V_{\text{CC}}$ $\overline{\text{PEN}}, \overline{\text{TEST}}$ |
| | | | | 300 | μA | $V_{\text{IN}} = V_{\text{CC}}$ OSCIN |
| V_{OL} | Output Low Voltage | | | 0.4 | Volt | $I_{\text{OL}} = -2.0\text{ mA}$ $\overline{\text{RXE}}, \text{CI+}, \text{DI+}$ |
| | | | | 1.2 | Volt | $I_{\text{OL}} = -10\text{ mA}$ $\overline{\text{JAB}}, \overline{\text{LINK}}$ |
| V_{OH} | Output High Voltage | 4.0 | | | Volt | $I_{\text{OH}} = 2\text{ mA}$ $\text{CI+}, \text{DI+}, \overline{\text{RXE}}$ |
| | | 2.4 | | | Volt | $I_{\text{OH}} = 15\ \mu\text{A}$ $\overline{\text{LINK}}, \overline{\text{JAB}}$ |
| C_{IN} | Input Capacitance | | 5.0 | | pF | |
| I_{CC} | V_{CC} Supply Current | | | 150 | mA | Transmitting |

TWISTED PAIR CHARACTERISTICS TRANSMIT

Unless otherwise noted, all test conditions are as follows:

1. $T = 0 - 70^{\circ}\text{C}$
2. $V_{\text{CC}} = 5\text{V} \pm 5\%$
3. $20\text{ Mhz} \pm 0.01\%$
4. $\text{REXT} = 10\text{K} \pm 1\%$, no load
5. 50 OHM LOAD FROM TPO \pm TO V_{CC}

| SYM | PARAMETER | LIMIT | | | UNIT | CONDITIONS |
|-------------------|--|--------------|------|----------|-------|--|
| | | MIN | TYP | MAX | | |
| T _{OV} | TPO \pm Differential Output Voltage | 2.2 | 2.5 | 2.8 | V pk | |
| T _{OVT} | TPO \pm Differential Output Voltage Template | See Figure 2 | | | | |
| T _{SOI} | TPO \pm SOI Output Voltage Template | See Figure 4 | | | | |
| T _{LPT} | TPO \pm Link Pulse Output Voltage Template | See Figure 5 | | | | |
| T _{OIV} | TPO \pm Differential Output Idle Voltage | | | ± 50 | mV | Measured on Secondary Side of XFMR on Figure 7. |
| T _{OIA} | TPO \pm Output Current | 44 | 50 | 56 | mA pk | |
| T _{OIR} | TPO \pm Output Current Adjustment Range | 44 | 50 | 60 | mA pk | $V_{\text{CC}} = 5\text{V}$ Adjustable with REXT |
| T _{REXT} | External Bias Resistor | 8K | | 10K | ohm | 10K Recommended |
| T _{CMA} | TPO \pm Common Mode AC Output Voltage | | 10 | 50 | mV pk | |
| T _{HD} | TPO \pm Harmonic Distortion | | | -27 | dB | All 1's Output |
| T _{OR} | TPO \pm Output Resistance | | 10 K | | Ohm | |
| T _{OC} | TPO \pm Output Capacitance | | 15 | | pF | |

TWISTED PAIR CHARACTERISTICS RECEIVE

Unless otherwise noted, all test conditions are as follows:

1. T = 0 – 70°C
2. V_{CC} = 5V ±5%
3. 20 Mhz ±0.01%
4. REXT = 10K ±1%, no load
5. 10 MHz sinewave on TPI±

| SYM | PARAMETER | LIMIT | | | UNIT | CONDITIONS |
|------------------|--|-----------------------------|--------------------|-----------------------------|-------|------------|
| | | MIN | TYP | MAX | | |
| R _{ST} | TPI± Squelch Threshold | 310 | | 540 | mV pk | |
| R _{UT} | TPI± Unsquelch Threshold | 190 | | 330 | mV pk | |
| R _{ZT} | TPI± Zero Cross Switching Threshold | | | ±20 | mV pk | |
| R _{OCV} | TPI± Input Open Circuit Voltage | V _{CC} /3 -0.25 | V _{CC} /3 | V _{CC} /3 +0.25 | Volt | |
| R _{CMR} | TPI± Input Common Mode Voltage Range | V _{CC} /3 -1.0 | | V _{CC} /3 +1.0 | Volt | |
| R _{DR} | TPI± Input Differential Voltage Range | 0.540 | | V _{CC} | V pk | |
| R _{CRR} | TPI± Input Common Mode Rejection Ratio | | | -20 | dB | 0 – 10 Mhz |
| R _{IR} | TPI± Input Resistance | 5K | | | ohm | |
| R _{IC} | TPI± Input Capacitance | | 10 | | pF | |

AC TEST TIMING CONDITIONS

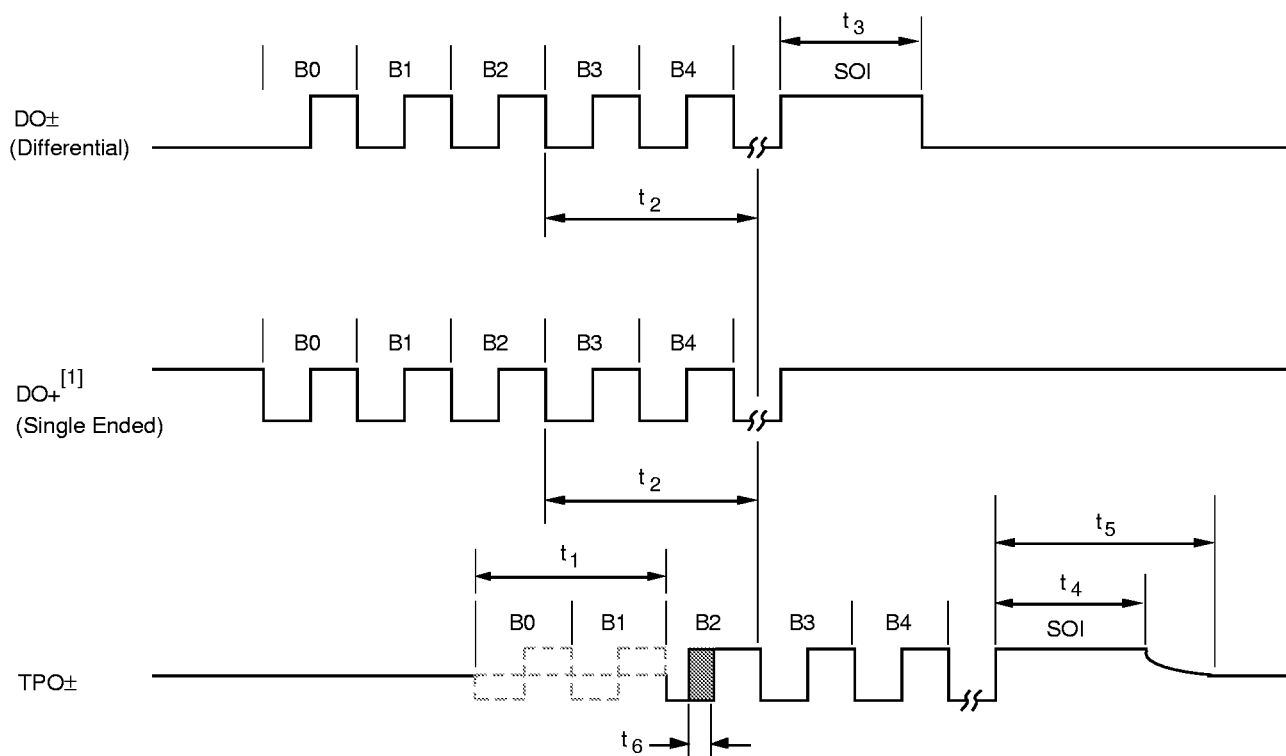
Unless otherwise noted, all test conditions are as follows:

1. $T = 0 - 70^{\circ}\text{C}$
2. $V_{\text{CC}} = 5\text{V} \pm 5\%$
3. $20\text{ Mhz} \pm 0.01\%$
4. $\text{REXT} = 10\text{K} \pm 1\%$, no load
5. Input conditions:
All Inputs: $t_r, t_f \leq 10\text{ ns}, 20 - 80\%$
6. Output Loading
TPO \pm : 50 Ohms To V_{CC} On Each Output, 10 pF
Open Drain Digital Outputs: 1K Pullup, 50 pF
All Other Digital Outputs: 50pF
7. Measurement Points:
TPO \pm , TPI \pm : 0v During Data, $\pm 0.30\text{V}$ at start/end of packet
DO \pm : 0v (Differential Interface)
1.5 Volts (Single Ended Clocked Interface)
2.5 Volts (Single Ended Non-Clocked Interface)
DI+, CI+ 2.5 Volts
All other inputs and outputs: 1.5 Volts

TRANSMIT TIMING CHARACTERISTICS

Refer To Figure 8 For Timing Diagram

| SYM | PARAMETER | LIMIT | | | UNIT | CONDITIONS |
|-------|--|-------|-----|-----------|------|---|
| | | MIN | TYP | MAX | | |
| t_1 | DO \pm or DO+ to TPO \pm Bit Loss | | | 2.0 | BT | |
| t_2 | DO \pm or DO+ to TPO \pm Propagation Delay | | | 200 | ns | |
| t_3 | DO \pm SOI Pulse Width Required For Idle Detection | 150 | | 200 | ns | |
| t_4 | TPO \pm SOI Pulse Width To 0.3V Point | 225 | | 325 | ns | See Figure 4. Measure TPO \pm from last zero crossing to 0.3V point |
| t_5 | TPO \pm SOI Pulse Width To 50 mV Point | | | 4500 | ns | See Figure 4. Measure TPO \pm from last zero crossing to 50 mV point |
| t_6 | TPO \pm Output Jitter | | | ± 8.0 | ns | |



Notes: 1. DO- = GND for Non-Clock Mode.
 DO- = Vcc for Clock Mode.

Figure 8. Transmit Section Timing

RECEIVE SECTION TIMING CHARACTERISTICS

Refer To Figure 9 For Timing Diagram

| SYM | PARAMETER | LIMIT | | | UNIT | CONDITIONS |
|----------|--|-------|-----|-------|------|--|
| | | MIN | TYP | MAX | | |
| t_{21} | TPI± To DI+ Bit Loss | | | 5.0 | BT | |
| t_{22} | TPI± to DI+ Propagation Delay | | | 200 | ns | |
| t_{23} | TPI± SOI Pulse Width Required For Idle Detection | 150 | | 200 | ns | Measure TPI± from last zero crossing to 0.3V Point |
| t_{25} | DI+ Output Jitter | | | ± 1.5 | ns | |
| t_{26} | TPI± to $\overline{\text{RXE}}$ Assert | | | 500 | ns | |
| t_{27} | DI+ Stop to $\overline{\text{RXE}}$ Deassert | | | 250 | ns | |

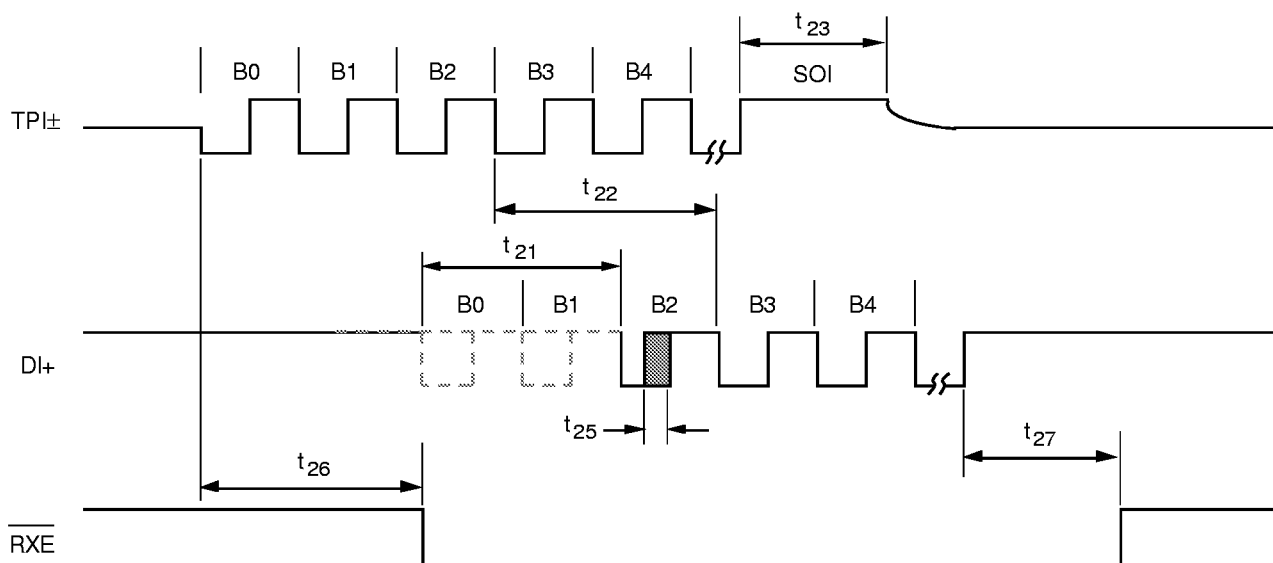


Figure 9. Receive Section Timing

COLLISION TIMING CHARACTERISTICS

Refer To Figure 10 For Timing Diagram

| SYM | PARAMETER | LIMIT | | | UNIT | CONDITIONS |
|----------|---|-------|-----|-------|------|------------|
| | | MIN | TYP | MAX | | |
| t_{31} | Collision Start To Cl+ Assert Delay | | | 600 | ns | |
| t_{33} | Collision Start To End Of Loopback On DI+ | | | 600 | ns | |
| t_{34} | Collision Start To Start Of Receive Data On DI+ | | | 700 | ns | |
| t_{35} | Cl+ Cycle Time | 99.9 | 100 | 100.1 | ns | |
| t_{36} | Cl+ Low Or High Time | 45 | 50 | 55 | ns | |
| t_{37} | Collision Stop To Cl+ Deassert | | | 600 | ns | |
| t_{39} | Collision Stop To End Of Receive Data On DI+ | | | 600 | ns | |
| t_{40} | Collision Stop To Start Of Loopback On DI+ | | | 700 | ns | |

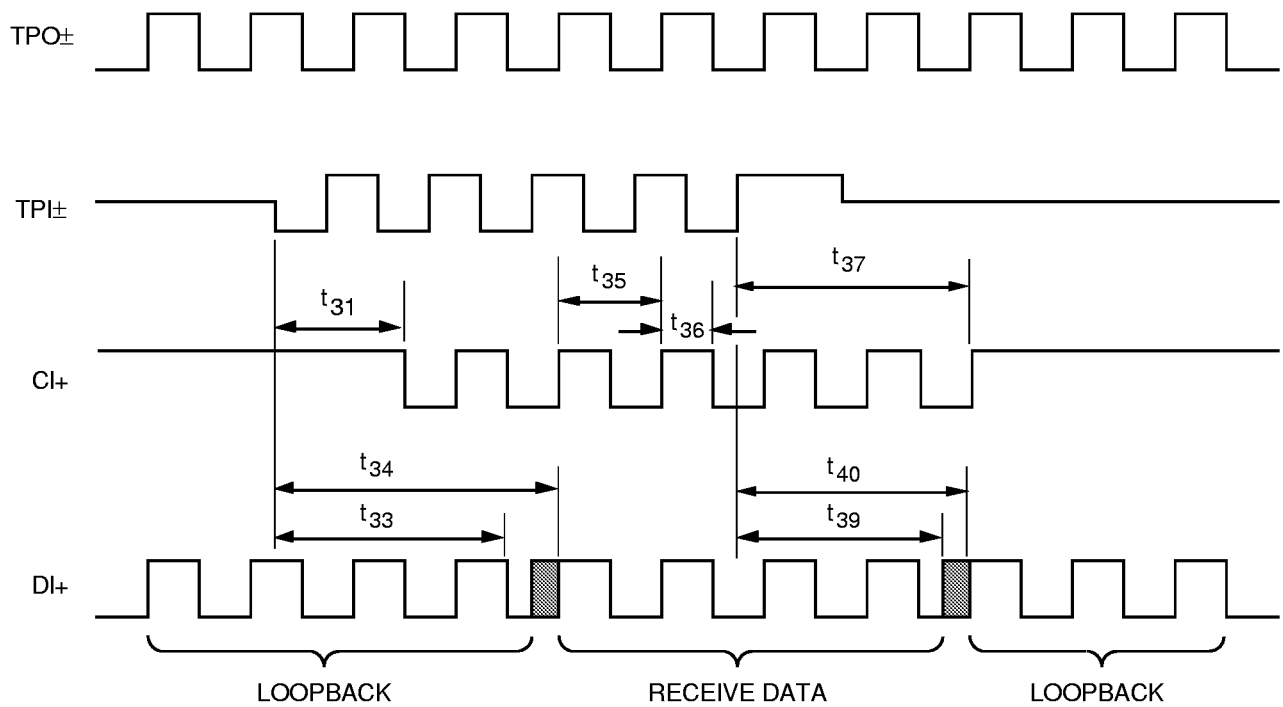


Figure 10. Collision Timing

LINK PULSE TIMING CHARACTERISTICS

Refer To Figure 12 For Timing Diagram

| Sym. | Parameter | Limit | | | Unit | Conditions |
|-----------------|--|-------|-----|-----|-------------|-----------------------------|
| | | Min | Typ | Max | | |
| t ₆₁ | Transmit Link Pulse Width | 100 | | 150 | ns | See Figure 5 |
| t ₆₂ | Transmit Link Pulse Period | 8 | | 24 | ms | |
| t ₆₅ | Receive Link Pulse Width Required For Detection | 50 | | | ns | |
| t ₆₆ | Receive Link Pulse Minimum Period Required For Detection | 2 | | 7 | ms | Link_Test_Min |
| t ₆₇ | Receive Link Pulse Maximum Period Required For Detection | 50 | | 150 | ms | Link_Loss and Link_Test_Max |
| t ₇₁ | Receive Link Pulse Assert | 2 | 3 | 10 | Link Pulses | |

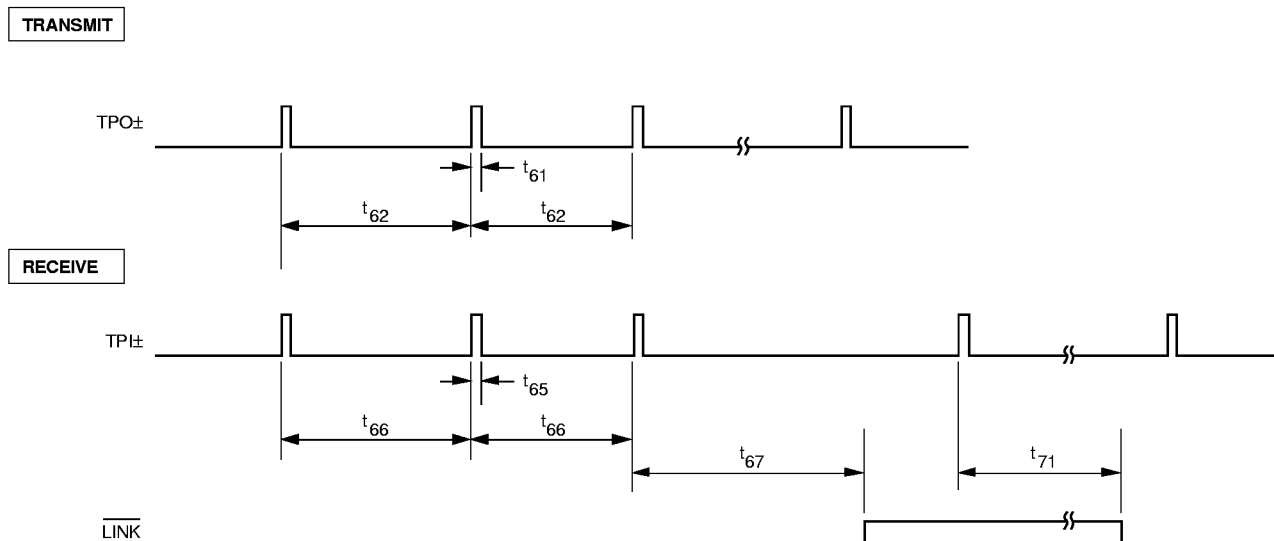


Figure 12. Link Pulse Timing

JABBER TIMING CHARACTERISTICS

Refer To Figure 13 For Timing Diagram

| SYM | PARAMETER | LIMIT | | | UNIT | CONDITIONS |
|----------|--------------------------|-------|-----|-----|------|------------|
| | | MIN | TYP | MAX | | |
| t_{81} | Jabber Activation Time | 20 | | 50 | ms | |
| t_{82} | Jabber Deactivation Time | 250 | | 750 | ms | |

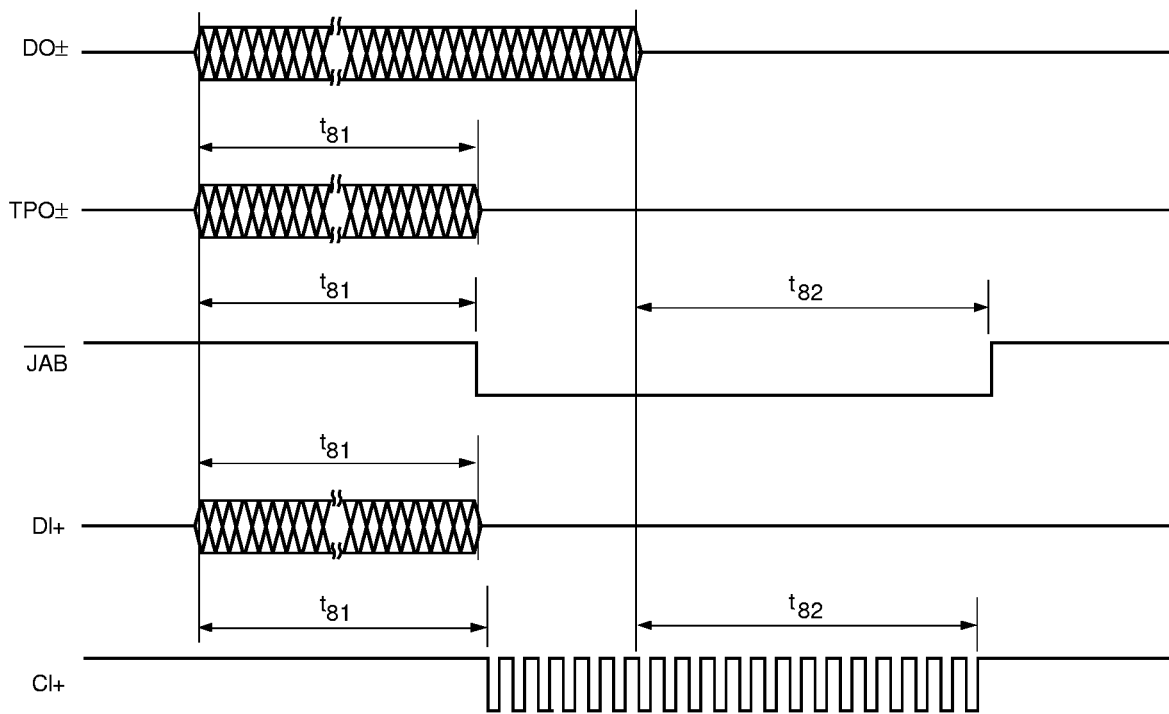


Figure 13. Jabber Timing

Revision History

1/22/97

- Page 2, Pin Description;

- Pin 3 (I/O) has changed from I/O Pullup to O Pullup.
- Pin 14 (I/O) has been changed from I/O Pullup to I Pullup.
- Pin 14 (Description) has been changed to;

Full Duplex Enable Input with a resistor pullup. To force the device into the Full Duplex Mode, tie this pin to GND.

$\overline{\text{FDPLX}} = 1$ Half Duplex Mode
 $\overline{\text{FDPLX}} = 0$ Full Duplex Mode Enabled

Page 4, Figure 1. 83C96 Block Diagram;

- Mode Inputs and Status Outputs, $\overline{\text{JAB/ADPLX}}$ Input/Output has been changed to, $\overline{\text{JAB}}$ Output. Test has been changed from Output to Input, $\overline{\text{FDPLX}}$ has been changed from Input/Output to Input.

Page 5, Beginning on Page 5 new pagination has occurred.

Page 6, Change to Figure 2, Alphabetic references have been added to illustration.

- Voltage Template Values Table for Figure 2. has been added.

Page 9, Section Jabber, paragraph 2, ... $\overline{\text{JAB/ADPLX}}$ is an input/output... has been changed to, $\overline{\text{JAB}}$ is an output pin for jabber detection. This pin consists of an open drain output transistor with a resistor pullup. This pin can drive an LED from VCC or it can drive another digital input.

Page 10, Section Full Duplex, paragraphs 2, and 3 have been changed and combined into one paragraph, paragraph now reads;

The device can be forced into the full duplex mode. $\overline{\text{FDPLX}}$ is a full duplex mode enable input. If the pin is tied to GND, the pin is configured as an input and full duplex mode is enabled. If the pin is left floating or connected to logic "1" the part goes into half duplex.

- Paragraph 4, ... $\overline{\text{JAB/ADPLX}}$ is an input/output... has been deleted.

Page 11, Section, TP Transmit Output Current Set, paragraph 3 ...For example, if... the IEEE levels., text has been deleted.

Page 13, Absolute Maximum Ratings,

- V_{CC1} , V_{CC2} Supply Voltage has been changed from -0.3V to 7V to -0.3V to 6V.
- Package Power Dissipation has been changed from 1 Watt @25°C to 1 Watt @ 70°C
- Operating Temperature -65°C to +125°C has been changed to Temperature Under Bias -10°C to +80°C.
- Max. Lead Temperature (Soldering, 10 Sec) has been changed from 250°C to 260°C.
- Max. Body Temperature (Soldering, 30 Sec) 220°C has been added.

Page 14, Figure 7. Hub Schematic Using 83C96;

- $\overline{\text{FDPLX}}$ output has been changed to $\overline{\text{FDPLX}}$ input, and Full Duplex Detect reference has been deleted.

Page 15, DC Electrical Characteristics

- I_{IL} Conditions, $V_{IN} = \text{GND}$, $\overline{\text{PEN}}$, $\overline{\text{TEST}}$, $\overline{\text{DO}\pm}$, Unit μA , Limit (Max) -1, has been added.
- I_{IL} Conditions $V_{IN} = \text{GND}$, $\overline{\text{JAB/ADPLX}}$, $\overline{\text{LINK}}$, $\overline{\text{FDPLX}}$ has been changed to $V_{IN} = \text{GND}$, $\overline{\text{LINK}}$, $\overline{\text{FDPLX}}$.
- I_{IH} Conditions $V_{IN} = V_{CC}$, $\overline{\text{FDPLX}}$, $\overline{\text{DO}\pm}$, $\overline{\text{LINK}}$, Unit μA , Limit (Max) 1 has been added.
- I_{IH} Conditions $V_{IN} = V_{CC}$, $\overline{\text{PEN}}$, $\overline{\text{TEST}}$ has been changed to $V_{IN} = V_{CC}$, $\overline{\text{PEN}}$, $\overline{\text{TEST}}$.
- V_{OL} Conditions $I_{OL} = -2.0 \text{ mA}$ has been changed to $I_{OL} = -2.0 \text{ mA}$ $\overline{\text{RXE}}$, CI+ , DI+ .
- V_{OL} Conditions $I_{OL} = -10 \text{ mA}$, $\overline{\text{LINK}}$, $\overline{\text{FDPLX}}$, $\overline{\text{JAB/ADPLX}}$ has been changed to $I_{OL} = -10 \text{ mA}$, $\overline{\text{JAB}}$, $\overline{\text{LINK}}$
- V_{OH} Conditions $I_{OL} = 8.0 \mu\text{A}$ All Except $\overline{\text{LINK}}$, $\overline{\text{FDPLX}}$, $\overline{\text{JAB/ADPLX}}$ has been changed to $I_{OH} = 2 \text{ mA}$ CI+ , DI+ , $\overline{\text{RXE}}$.
- V_{OH} Conditions $I_{OL} = 15 \mu\text{A}$ $\overline{\text{LINK}}$, $\overline{\text{FDPLX}}$, $\overline{\text{JAB/ADPLX}}$ has been changed to $I_{OH} = 15 \mu\text{A}$ $\overline{\text{LINK}}$, $\overline{\text{JAB}}$.

Revision History

1/22/97

Page 16, Twisted Pair Characteristics Transmit

- T_{OIR} Limit (Min) has been changed from 30 to 44.
- T_{OIR} Limit (Max) has been changed from 80 to 60.
- T_{REXT} has been added.

Page 17, Twisted Pair Characteristics Receive

- R_{DR} Limit (Min) has been changed from V_{SS} to 0.540.
- R_{DR} Unit has been changed from Volt to V pk.

Page 18, AC Test Timing Conditions

- t_1 Parameter has been changed from DO_{\pm} to TPO_{\pm} Bit Loss to DO_{\pm} or $DO+$ to TPO_{\pm} Bit Loss.
- t_2 Parameter has been changed from DO_{\pm} to TPO_{\pm} Propagation Delay to DO_{\pm} or $DO+$ to TPO_{\pm} Propagation Delay .

Page 19, Figure 8. Transmit Section Timing, timing $DO+$ (Single Ended) and Note .1, have been added, and timing TOP_{\pm} has changed.

Page 20, Receive Section Timing Characteristics;

- t_{24} has been deleted.
- t_{27} Parameter has been changed from TPI_{\pm} Stop to TXE Deassert to DI_{\pm} Stop to \overline{RXE} Deassert.
- Figure 9. Receive Section Timing, timing $DI+$ has been changed.

Page 21, Figure 10. Collision Timing, timing $CI+$ has been changed.

Page 22, Link Pulse Timing Characteristics,

- t_{63} , t_{64} , t_{68} , t_{69} , t_{70} , t_{72} , have been deleted.

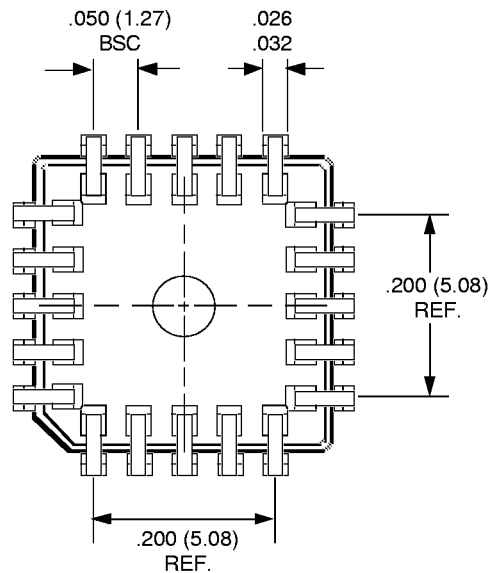
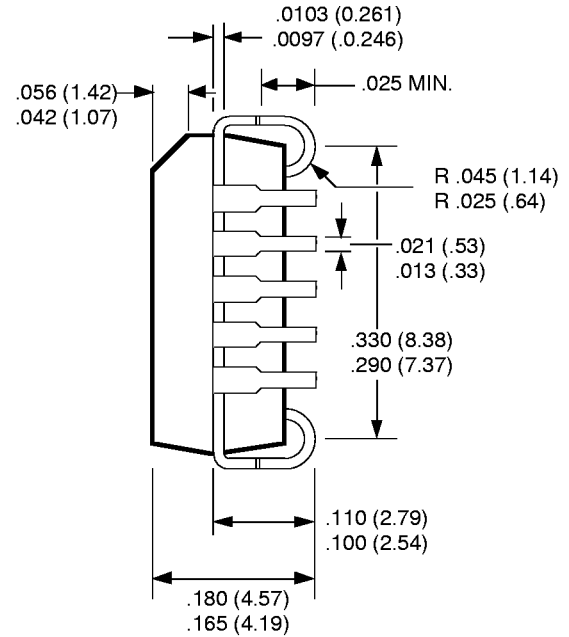
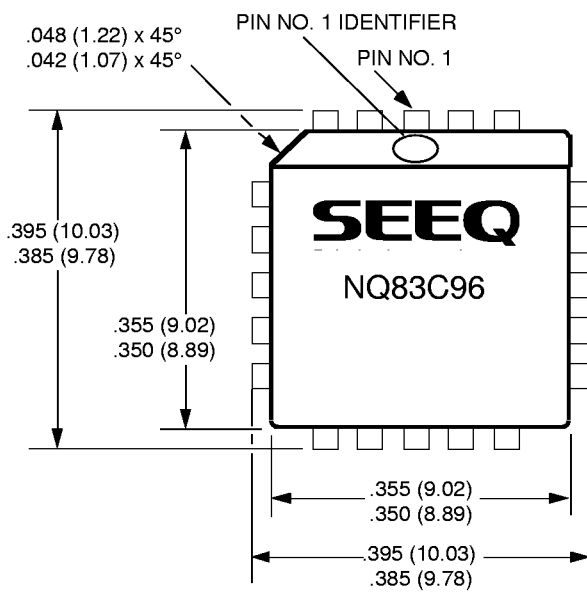
Page 23, Figure 12. Link Pulse Timing

- All references to t_{63} , t_{64} , t_{68} , t_{69} , t_{70} , t_{72} , have been deleted.
- $FDPLX$ has been deleted.

Page 28, Package Diagram has been added to the data sheet.

SURFACE MOUNT PACKAGES

20-PIN PLASTIC LEADED CHIP CARRIER



NOTES

1. All dimensions are in inches and (millimeters).
2. Dimensions do not include mold flash. Maximum allowable flash is .008 (.20).
3. Formed leads shall be planar with respect to one another, within 0.004 inches.