MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33385

Automotive Quad Low Side Driver

SILICON MONOLITHIC
INTEGRATED CIRCUIT

Advance Information

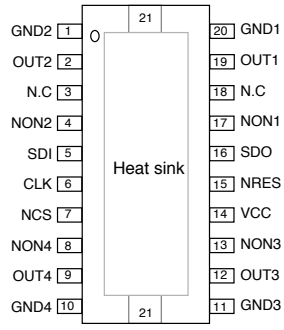
Automotive Quad Low Side Driver

HSOP20

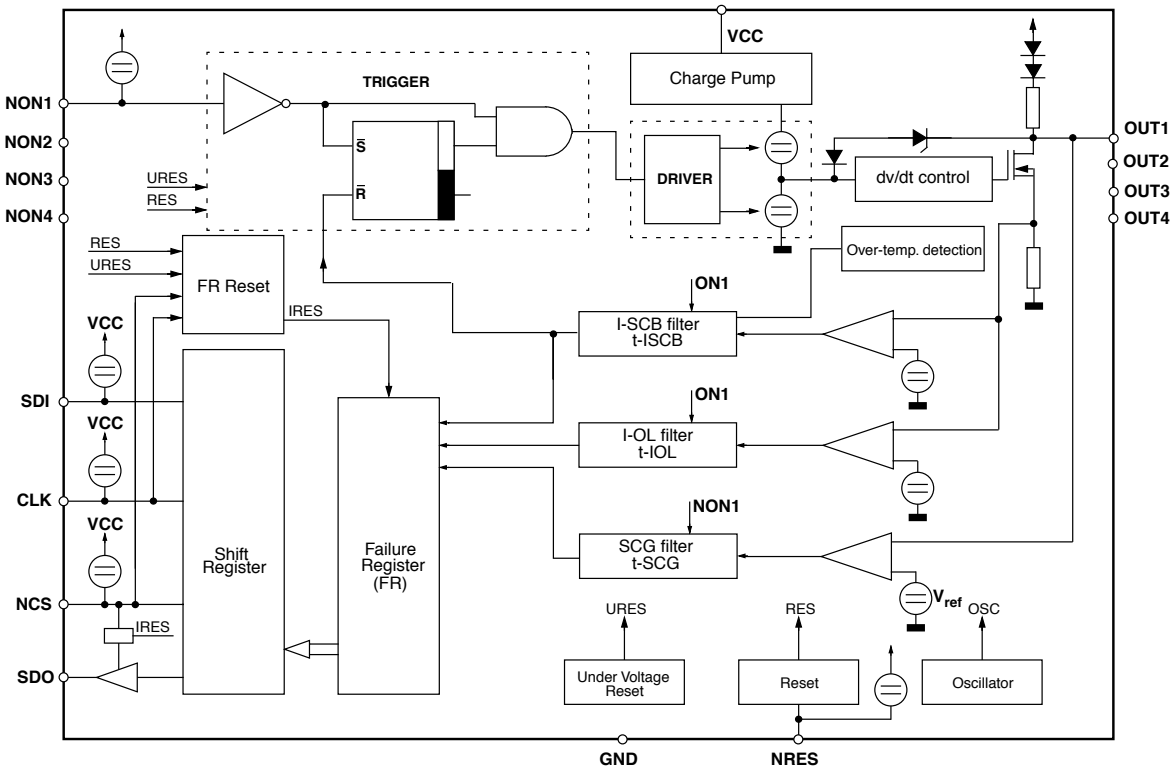
The MC33385 is a Quad Low Side Driver fully protected switch. This device is a general purpose Low Side Driver but has been especially designed to operate in engine management application as injector driver or automotive gear box. It is interfaced directly with a microcontroller for parallel control of the load and the individual output diagnostic is done through a SPI. The diagnostic logic recognizes 4 failure types at each output stage the overcurrent, the short to GND, the openload and the over-temperature.

- RDSON of 250mΩ per Output at 25°C
- Supplied from the main 5V Vcc
- Input CMOS Compatible
- Diagnostic through SPI
- Nominal Current of 2A per Output
- Current Limitation at 3A with Automatic Turn Off
- Output Internally Clamped at 50V typ for Inductive Load Drive
- Junction to Case Thermal Resistance of 4.4°C/W
- Individual Output over Temperature Shutdown

PIN ASSIGNMENT



Simplified Block Diagram



Date : 10/12/98
Rev 4.2

MAXIMUM RATINGS T_J = - 40°C up to 150°C

Ratings	Symbols	Min	Max	Unit
SUPPLY VOLTAGE				
Voltage Range	Vcc	- 0.3	7	V
OUTPUTS : 1...4				
Continuous Output Voltage (With no reverse current)	V_{out}	- 0.3	45	V
Continuous Current	I_{outc}		2.5	A
Peak Output Current	I_{outp}	- 10	I_{SCBmax}	A
Clamped Energy at the Switching OFF (See figure 6)	W_{OFF}		70	mJ for 1ms
INPUTS				
Input Voltage (Inputs)	V_{IN}	- 0.3	Vcc + 0.3	V
Input Protection Diode Current	I_{IN}	- 20	1	mA
OUTPUTS : SDO				
Input Voltage (Outputs)	V_o	- 0.3	Vcc + 0.3	V
Input Protection Diode Current	I_o	- 20	1	mA
THERMAL RATINGS				
Operating Junction Temperature	T_j	- 40	150	°C
Thermal Resistance : Junction-case (One powerstage in use)	R_{thjc}		4.5	K/W
Thermal Resistance : Junction-ambient (Device soldered on printed circuit board)	R_{thja}		50	K/W

RANGE OF FUNCTIONALITY T_{case} = - 40°C up to 125°C

Ratings	Symbols	Min	Max	Unit
SUPPLY VOLTAGE				
Supply Voltage Range	V_{cc}	4.5	5.5	V
JUNCTION TEMPERATURE				
Junction Temperature Continuous (Continuous)	T_{j1}	- 40	150	°C
Junction Temperature Dynamical (Time limited)	T_{j2}		185	°C
OUTPUT CURRENT				
Output Current Range	I_{out}		I_{SCBmax}	
RESET BEHAVIOUR				
Reset Changeable (at NRES-Pin)	V_{cc}	V_{ccRES}	5.5	V
Undervoltage Reset (Independent of NRES) Active for Vcc = 0V to VccPRO	V_{ccRES}	3.35	3.95	V
UNDERVOLTAGE PROTECTION				
Protection active for Vcc=0V to Vccpro	V_{ccPRO}	1.5	4.0	V
OVER TEMPERATURE				
Temperature Detection Threshold	T_{OFF}	155	185	°C

ELECTRICAL CHARACTERISTICS T_{CASE} = - 40° up to + 125°C and V_{CC} = 4.5V up to 5.5V

Parameters	Symbol	Min	Typ	Max	Unit
SUPPLY CURRENT					
Standby Current (without load) (NON1...NON4 = High Level) 5.15V ≥ V_{CC} 5.5V ≥ V_{CC}	 I_{ccSTB1} I_{ccSTB2}			 6 7	 mA mA
Operating Mode (For 5.15V ≥ V_{CC}) (Iout 1...4) = 2A	I_{ccOPM}			17	mA
ΔI_{cc} During Reverse Output Current (Iout = - 5A on one output)	ΔI_{cc}			100 50	mA mA
INPUTS					
NONx, NCS, CLK, NRES, SDI					
Low Threshold	VINL	-0.3		0.2*V_{cc}	V
High Threshold	VINH	0.7*Vcc		V_{cc} + 0.3	V
Hysteresis	V_{hyst}	0.85			V
Input Current (Vin = Vcc)	IIN			10	µA
Input Current (Vcc >VRES & 0V<VIN < 0.9*Vcc)	IIN	- 100		- 20	µA
Input Frequency (NON1 to NON4)	fIN	0		1000	Hz
SERIAL DATA OUTPUT					
High Output Level (ISDO = -2mA)	VSDOH	V_{cc} - 0.4			V
Low Output Level (ISDO = 3.2mA)	VSDOL			0.4	V
Tristate Leakage Current (NCS = HIGH, VSDO = 0V to Vcc)	ISDOL	- 10		10	µA
OUTPUTS (Out 1...4)					
Average Output Current	I_{outa}	2.5			A
Output Peak Current	I_{outp}	ISCBmax			A
Leakage Current 1 (NON = High, Vout = 25V, Vcc = 5V)	I_{outL1}			10	µA
Leakage Current 2 (NON = High, Vout = 16V, Vcc = 1V)	I_{outL2}			10	µA
Output Clamp Voltage (Iout = 1A)	V_{clp}	45	50	58	V
Matching Clamp Voltage (Between two outputs)	V_{clpm}	Vclp-1		Vclp+1	V
Clamped Energy at the Switching OFF (See graph 6)	W_{OFF}	50			mJ for 1ms
On Resistance (Iout = 2A, Tj = 150°C, NON = LOW)	RDSON			500	mΩ
Output Low Voltage Limitation (Iout = 150mA)	Voutlim	65		220	mV
Output Capacitance (Guaranteed by design)	Cout			350	pF
OUTPUTS TIMING					
Positive Output Voltage Ramp (with inductive load) Vout = 4V... 16V Vout = 16V... Vclp	 OVRp1 OVRp2	 2 3.5	 3 6	 5 10	 V/µs V/µs
Negative Output Voltage Ramp (25%... 75%)	OVRn	1.75	3	4	V/µs
Internal Switch-on-Time Charge Pump (NON = LOW... VGate = 0.9 * VBat)	t_{dCP}			40	µs
Turn ON Delay (NON = 50%, Vout = 0.9 * VBat)	t_{dON}	1	2.5	5	µs

ELECTRICAL CHARACTERISTICS T_{CASE} = - 40° up to + 125°C and V_{CC} = 4.5V up to 5.5V

Parameters	Symbol	Min	Typ	Max	Unit
Turn OFF Delay (NON = 50%, Vout = 0.1 * VBat) (NON = 50%, Vout = 4V)	 t_{dOFFa} t_{dOFFb}		 1 4.7	 3 7.5	 µs µs
Undervoltage Protection Max ON time after a output voltage ramp from 0V to 25V at V_{cc} = 0V...Vccpro	t_{rpON}			100	µs
Matching Turn ON Delay (NON = 50%, Vout = 0.9 * VBat)	t_{mON}	- 3		3	µs
Rise time Turn OFF (10% - 90% of V_{clp})	t_{rOFF}		8.5	12	
OUTPUTS REVERSE DIODE					
Reverse Output Current	I_{RD}	2,5			A
Reverse Peakcurrent (Note 1 and 2)	I_{RDP}	5			A
Reverse Voltage Drop - I_{out} = - 5A - I_{out} = - 2,5A	 V_{RD1} V_{RD2}	 1.0 0.85		 1.7 1.7	 V V
POWERSTAGE PROTECTION					
Short Current Limit	I_{SCB}	3.0		5	A
Short Circuit Delay Time	t_{SCB}	0.2		2	µs
V_{cc} Undervoltage	V_{ccmin}	3.35		3.95	V
DIAGNOSTIC					
Short to GND Threshold Voltage for $I_{OUT} \leq$ 2A	V_{REF}	0.390xVcc		0.435xVcc	V
Short to GND Filter Time	T_{SCG}	140		250	µs
Open Load Threshold Current	I_{OL}	10		50	mA
Open Load Filter Time	t_{OL}	140		250	µs
Pull-up Resistor	R_{OL}	2.0		8.0	kΩ
Temperature Detection Threshold	T_{OFF}	155		185	°C

NOTES 1&2: For t ≤ 2ms. Max. reverse current is limited to - 10A (for all outputs together)

SERIAL DIAGNOSTIC LINK : Load Capacitor at SDI and SDO = 100pF

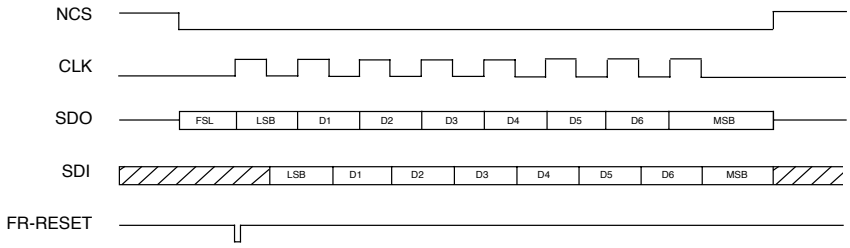
Clock Frequency (50% duty cycle)	fclk	3			MHz
Minimum Time CLK = HIGH	tclh	100			ns
Minimum Time CLK = LOW	tcll	100			ns
Propagation Delay (CLF Data at SDO valid)	tpcld			100	ns
NCS = LOW to Data at SDO Valid	tpcld			100	ns
CLK Low Before NCS Low (Setup time CLK to NCS change H/L)	tsclch	100			ns
CLK Change L/H after NCS = Low	thclcl	100			ns
SDI Input Set up Time (CLK change H/Lafter SDI data valid)	tscld	20			ns
SDI Input Hold Time (SDI data hold after CLK change H/L)	thcld			20	ns
CLK Low Before NCS High	tsclcl	150			ns
CLK High After NCS High	thclch	150			ns

ELECTRICAL CHARACTERISTICS T_{CASE} = - 40° up to + 125°C and V_{CC} = 4.5V up to 5.5V

Parameters	Symbol	Min	Typ	Max	Unit
NCSL/H ti Output Data Flout	tpchdz			100	ns
Capacitance at SDI, SDO, CLk, CS	tpcld			10	pF
NCS Filtertime (Pulses ≤ t_{fNCS} will be ignored)	t_{fNCS}	10		40	ns

DIAGNOSTIC REGISTER AND SPI TIMING

Figure 1 - Timing Diagram to Read the Diagnostic Register



NOTE : FR -RESET means Reset failure storage (internal signal)

Figure 2 - Diagnostic Failure Register Structure

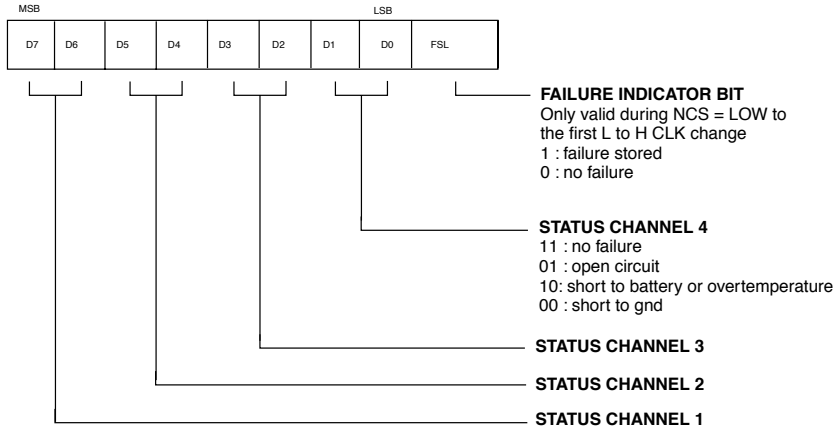


Figure 3 - Serial Interface Timing

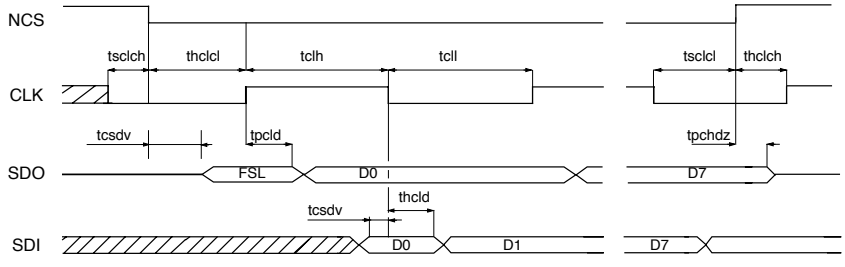


Figure 4 - Diagram to Short-Circuit to GNDFailure (SCG-Failure) Detection

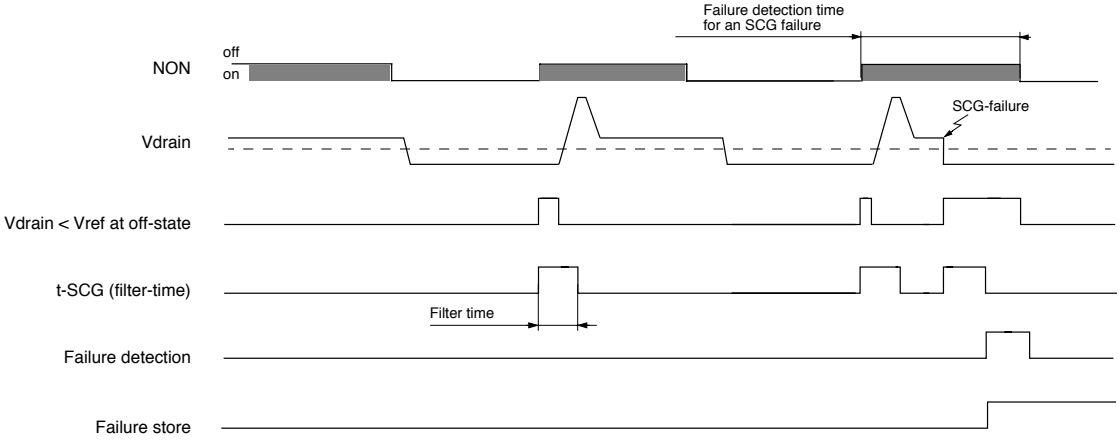


Figure 5 - Diagram to Open Load Failure (OL-Failure) Detection

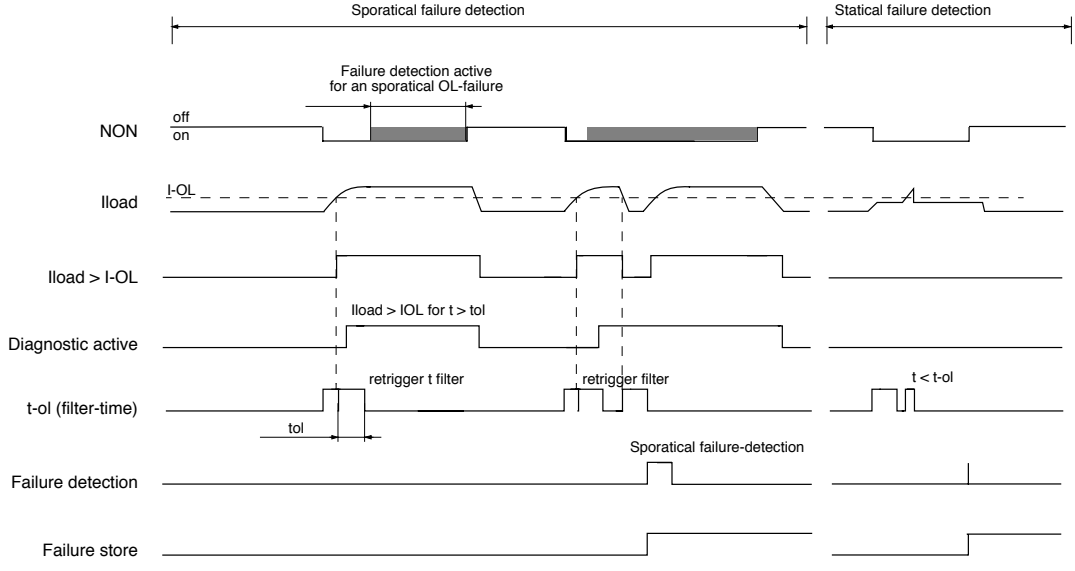
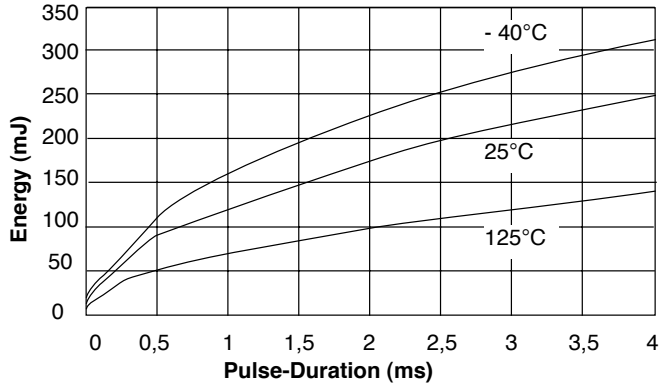


Figure 6 - Max Clamp- Energy Specification



DEVICE DESCRIPTION

Introduction

The device is a Quad Low Side Driver driven by four CMOS input stages. Each output power transistor is protected against short to V_{BAT} and by a zener clamp against overvoltage.

A diagnostic logic recognizes four failure types at the output stage : overcurrent, short to GND, open-load and overtemperature.

The failures are individually stored in a byte which can be read out via a serial interface (SPI).

Output Stage Control

Each of the four output stages is switched ON and OFF by an individual control line (NON-Input). The logic level of the control line is CMOS compatible. The output transistors are switched off when the inputs are not connected.

Power Transistors

Each of the four output stages has its own zenerclamp. This causes a voltage limitation at the power transistors when inductive loads are switched off. Drain voltage ramp occurring when output is switched on or off, is within defined limits. Output transistors can be connected in parallel to increase current capability. In this case, the associated inputs should be connected together.

Short-Circuit and Overtemperature Protection

If the output current increases above the short current limit for a time longer than t_{SCB} or if the temperature increases above T_{OFF} then the power transistor is immediately switched off. It remains switched off until the control signal on the NON-Input is switched off and on again.

Diagnostics

Following failures at the output stage are recognized :

Short -Circuit to V_{BAt} or overtemp..... = SCB (Highest priority)

Short -Circuit to GND..... = SCG

Open Load..... = OL (Lowest priority)

The SCB failure is recognized by an overcurrent (current above the short current limit) or an overtemperature.

If the current through the output stage is lower than the IOL-reference, after a filter time an OL failure will be recognized. This measurement is active while the powerstage is switched on.

The SCG failure will recognize when the drain voltage is lower than the OL reference limit, while the output stage is switched off. All four outputs have an independent overtemperature detection and shutdown. All failures are stored in individual registers.

They can be read by the microprocessor via the serial interface. There is no failure detected if the powerstage control time is shorter than the filter time.

Diagnostic Interface

The communication between the microprocessor and the failure register runs via the SPI link. If there is a failure stored in the failure register, the first bit of the shift register is set to a high level. With the H/L change on the NCS pin the first bit of the diagnostic shift register will be transmitted to the SDO output. The SDO output is the serial output from the diagnostic shift register and it is tristated when the NCS pin is high. The CLK pin clocks the diagnostic shift register. New SDO data will appear on every rising edge of this pin and new SDI data will be latched on every CLK's falling edge into the shift register. With the first positive pulse of the CLK, the failure register will be cleared. There is no bus collision at a small spike at the NCS. The CLK is always LOW while the NCS-signal is changing.

Reset

There are two different reset functions realised :

Under voltage reset : as long as the V_{cc} voltage is lower than V_{CCRES}, the powerstages are switched off and the failure-register are reseted.

Reset pin : as long as the NRES-pin is low, following circuits are reseted :

- Powerstages
- Failure register

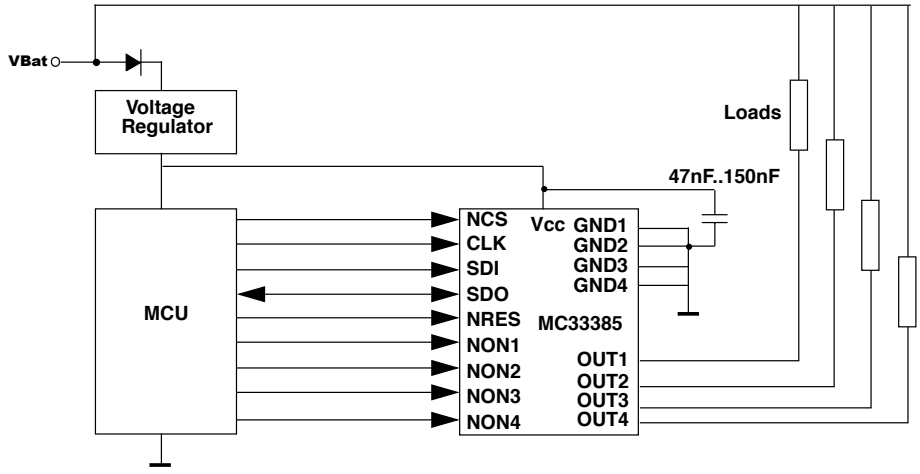
Undervoltage Protection

At low Vcc voltage, the device remains switched off even if there is a voltage ramp at the OUT pin.

This device is dedicated to automotive applications such as engine managements systems, automatic gear box... It interfaces between the microcontroller and the actuors of the system.

The loads can be only resistive or resistive and inductive such as injectors, EGR valves...etc... Following is an example of application schematic, see figure below.

Figure 7 - Typical Application



PINS FUNCTION DESCRIPTION

Pin No.	Function	Description
1	GND2	Ground 2
2	OUT2	Output Channel 2
3		NC
4	NON2	Input Control Signal for Channel 2
5	SDI	Serial Data Input
6	CLK	Clock Line for Serial Interface
7	NCS	Chip Select for Serial Interface
8	NON4	Input Control Signal for Channel 4
9	OUT4	Output Channel 4
10	GND4	Ground 4
11	GND3	Ground 3
12	OUT3	Output Channel 3
13	NON3	Input Control Signal for Channel 3
14	Vcc	5V Power Supply
15	NRES	Reset Input
16	SDO	Data Output of Serial Interface
17	NON1	Input Control Signal Channel 1
18		NC
19	OUT1	Output Channel 1
20	GND1	Ground 1
	Case	Connected to the PCB Ground for Thermal Purposes

Figure 8 - Standby Current versus Temperature

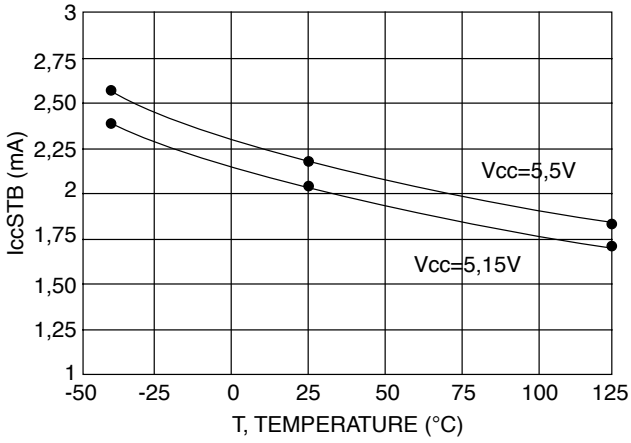


Figure 9 - Operating Mode Current versus Temperature

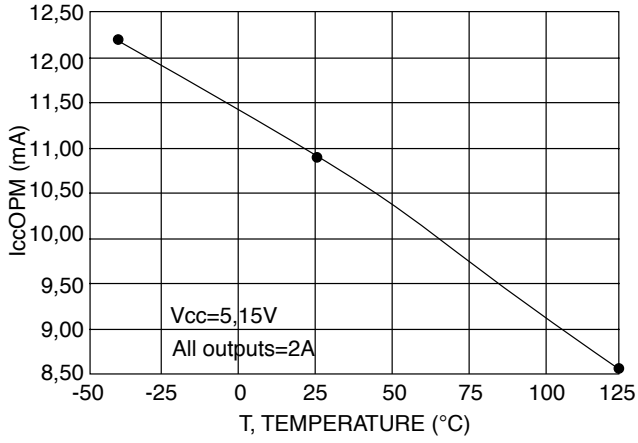


Figure 10 - Low Threshold Input Voltage versus Temperature

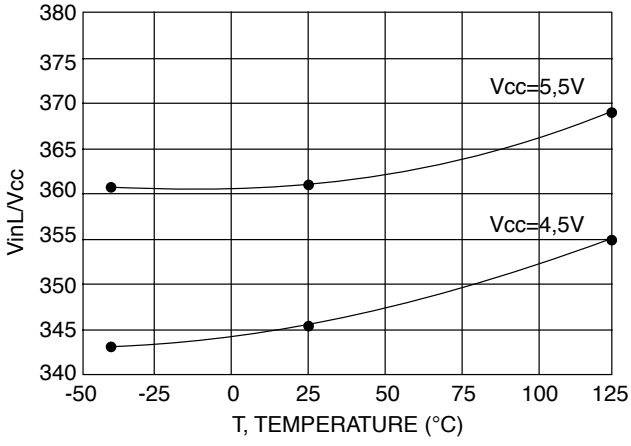


Figure 11 - High Threshold Input Voltage versus Temperature

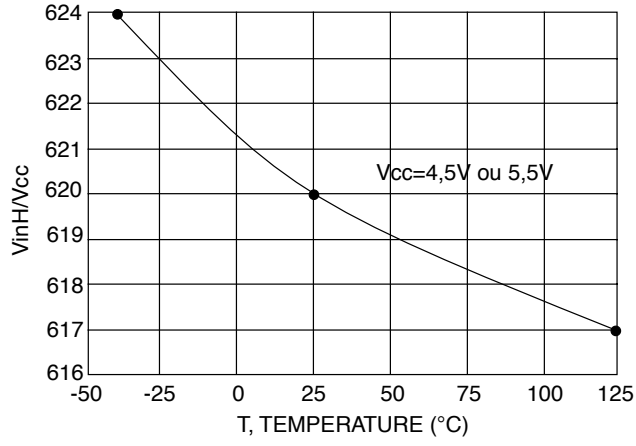


Figure 12 - Output Clamp Voltage versus Temperature

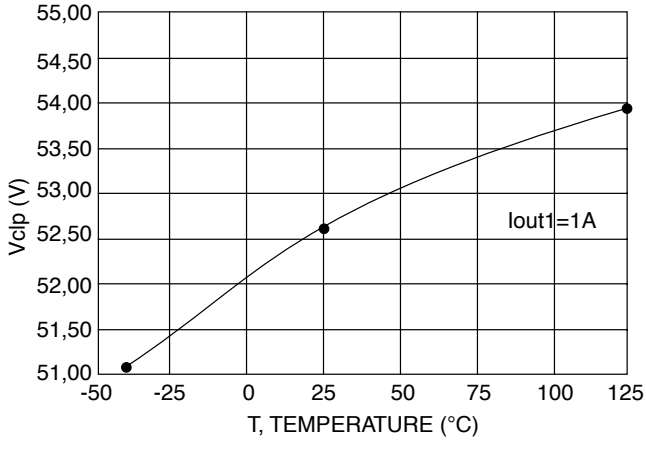


Figure 13 - Rdson versus Temperature

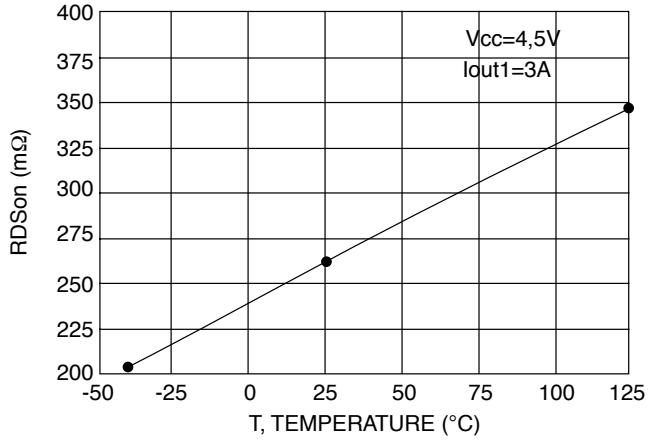


Figure 14 - Open Load versus Temperature

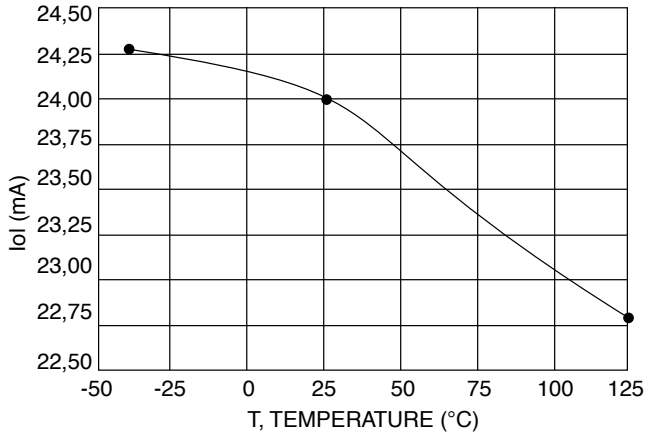


Figure 15 - Vcc Undervoltage versus Temperature

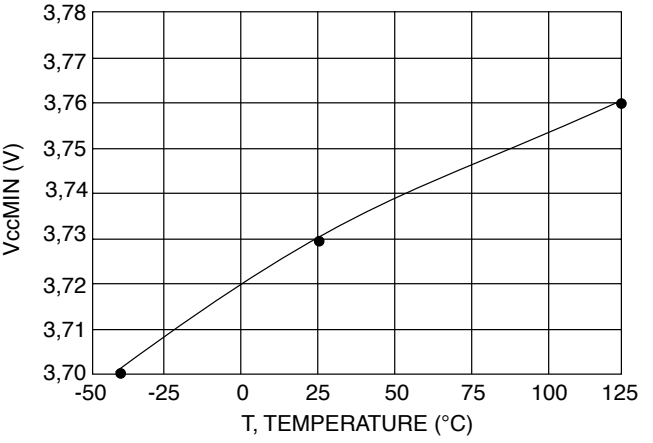


Figure 16 - Short Current Limit versus Temperature

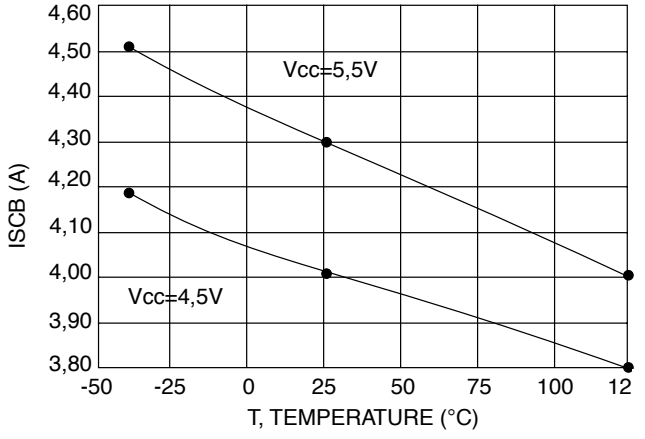


Figure 17 - Inductive Switching

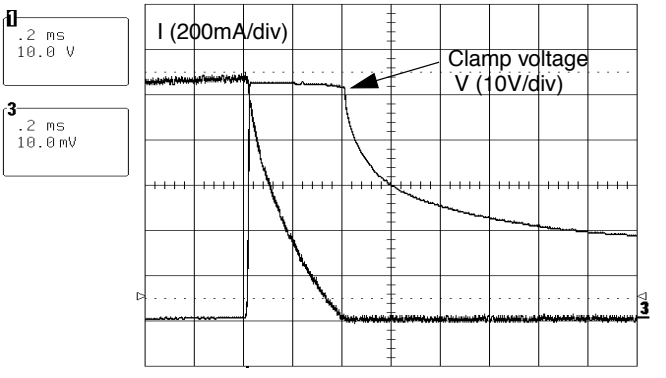


Figure 18 - Turn on Delay

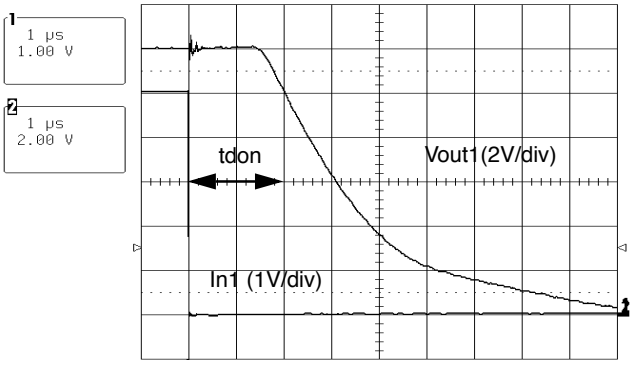
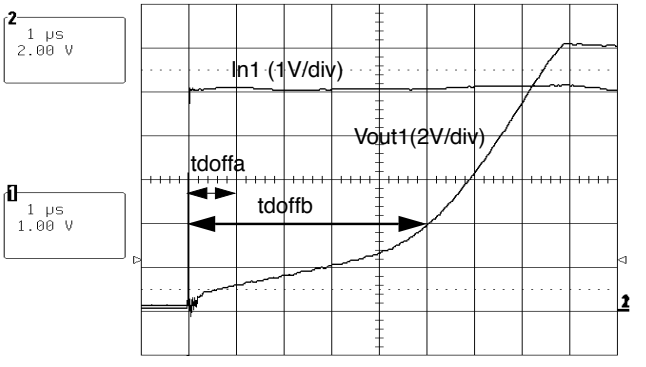
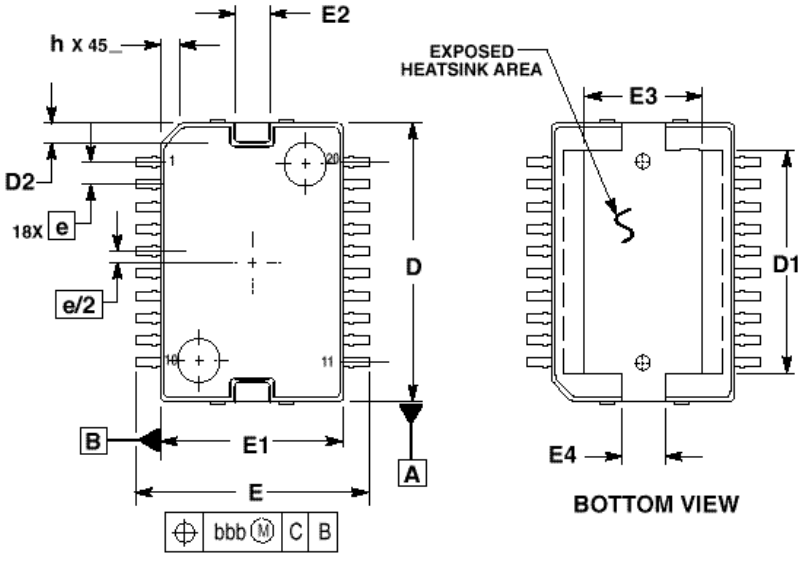
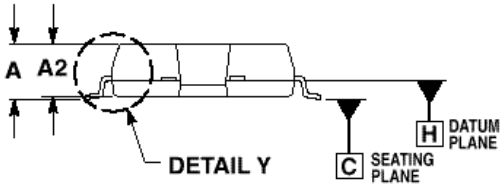


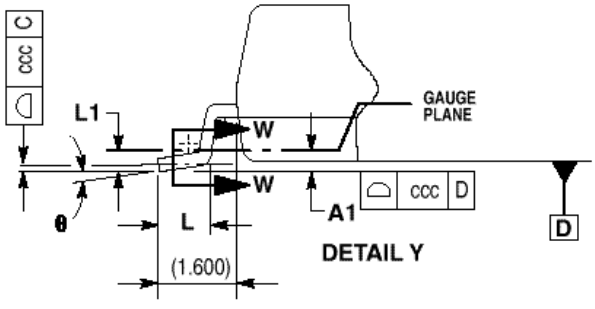
Figure 19 - Turn off Delay

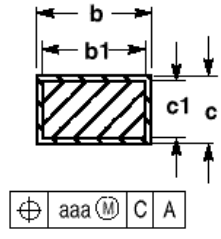


CASE OUTLINES









NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE ±H± IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.150 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE ±H±.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.178 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS ±A± AND ±B± TO BE DETERMINED AT DATUM PLANE ±H±.
7. DIMENSION D DOES NOT INCLUDE TIEBAR PROTRUSIONS. ALLOWABLE TIEBAR PROTRUSIONS ARE 0.150 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	3.100	3.350
A1	0.050 BSC	
A2	3.100	3.250
D	15.800	16.000
D1	12.270	12.470
D2	0.900	1.100
E	13.950	14.450
E1	10.900	11.100
E2	2.500	2.700
E3	7.000	7.200
E4	2.700	2.900
L	0.840	1.100
L1	0.350 BSC	
b	0.400	0.520
b1	0.400	0.482
c	0.230	0.310
c1	0.230	0.280
e	1.270 BSC	
h	±±±	1.100
θ	0_	8_
aaa	0.200	
bbb	0.200	
ccc	0.100	