IrDA – UART Integrated Interface

Description

The TSS4550 is a very low power consumption integrated circuit. It combines the functions of a PC–compatible UART and an IrDA interface circuit. It provides both serial and infrared communication interface ports to a processor. It connects to an external bus which may be either multiplexed address/data bus or separate address and data buses. It incorporates a FIFO–buffered high speed UART. The output of the UART may be connected, using a 3 way multiplexer, to either an external IrDA transceiver via an internal pulse shaping circuit or directly to one of two separate MODEM compatible output ports (logic levels). The pulse shaper is compliant to the IrDA standards revision 1.2.
The TSS4550 also provides additional peripheral support by way of control outputs and a parallel I/O port. In addition to normal operating modes, the device has a power–down mode for power saving and test modes to assist with board manufacturing.

Features

- General purpose processor interface with separate address and data buses
- Intel compatible ALE input for multiplexed address/data bus
- UART with 2x16 bytes receive and transmit FIFO
- Programmable rate from 50 to 115200 bauds
- Pulse shaping circuit for direct connection to IrDA transceivers
- 2 MODEM compatible ports (DTR, RTS, Sout, DSR, DCD, CTS, Sin)
- 6 MODEM inputs may be used as general–purpose interrupts
- 2 general–purpose control outputs
- 6 bits parallel I/O interface
- Global interrupt request output
- On–chip oscillator using a low–cost 32 kHz crystal
- Buffered clock output for real–time clock reference
- Low noise integrated PLL
- Wide operating voltage range: 2.7V to 5.5V
- Very low operating power consumption: 3 mW at 3V
- Power–down mode
- Industrial and Commercial temperature ranges
- TQFP64 (1.5 mm thickness) and PLCC68
- Test modes for automated test on board

Applications

- Telecommunication Products (mobile phones, MODEM, PABX...)
- Portable Equipments
- Medical & Industrial data collection
- Internet TV Boxes, Video Conferencing Systems
- Intelligent Remote Control
- Electronic Money Terminals

Block Diagram

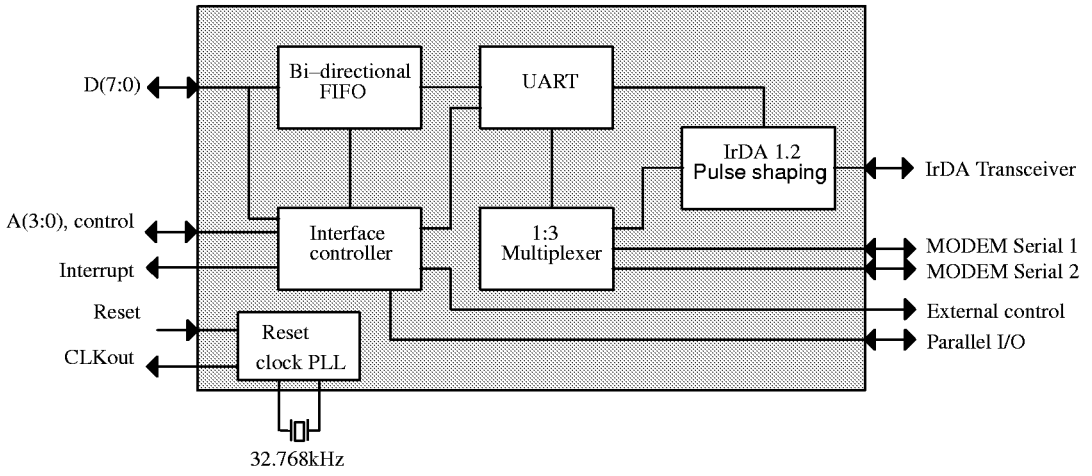


Figure 1. Block Diagram of TSS4550.

Pin Description

Function	Pins	Type	Rest State	Description
Data bus	D[7:0]	I/O strong	I / low	Data bus
Address bus	A[3:0]	I	I / low	Address bus
Bus interface control	ALE	I	I / low	Address Latch Enable, address latched on falling edge
	RD	I	I / low	Read strobe active high (must be tied low when not used)
	$\overline{RD}$	I	I / high	Read strobe active low (must be tied high when not used)
	WR	I	I / low	Write strobe active high (must be tied low when not used)
	$\overline{WR}$	I	I / high	Write strobe active low (must be tied high when not used)
	CS	I	I / low	Chip select active high (must be tied low when not used)
	$\overline{CS}$	I	I / high	Chip select active low (must be tied high when not used)
	$\overline{RESET}$	I	I / high	Hardware reset, active low
	INT	O medium	O / low	Interrupt to external bus, active high
Clocks	XTAL1	I	–	External crystal input
	XTAL2	O	–	External crystal output
	CLKOUT	O	O / low	Buffered clock
IrDA Interface	IRRX	I	I / high	From external IrDA transceiver – received data (inverted)
	TXIR	O medium	O / low	To external IrDA transceiver – transmitted data
	IRSD	O	O / low	External IrDA transceiver shutdown (when low) or general–purpose output, active high
MODEM Serial 1	$\overline{RTS1}$	O medium	O / high	MODEM 1 Request To Send or general–purpose output, active low

Function	Pins	Type	Rest State	Description
	$\overline{DTR1}$	O medium	O / high	MODEM 1 Data Terminal Ready or general–purpose output, active low
	SOUT1	O medium	O / high	MODEM 1 Serial data transmit
	$\overline{DSR1}$	I	I / high	MODEM 1 Data Set Ready or interrupt input, active low
	$\overline{DCD1}$	I	I / high	MODEM 1 Data Carrier Detect or interrupt input, active low
	$\overline{CTS1}$	I	I / high	MODEM 1 Clear To Send or interrupt input, active low
	SIN1	I	I / high	MODEM 1 Serial data receive
MODEM Serial 2	$\overline{RTS2}$	O medium	O / high	MODEM 2 Request To Send or general–purpose output, active low
	$\overline{DTR2}$	O medium	O / high	MODEM 2 Data Terminal Ready or general–purpose output, active low
	SOUT2	O medium	O / high	MODEM 2 Serial data transmit
	$\overline{DSR2}$	I	I / high	MODEM 2 Data Set Ready or interrupt input, active low
	$\overline{DCD2}$	I	I / high	MODEM 2 Data Carrier Detect or interrupt input, active low
	$\overline{CTS2}$	I	I / high	MODEM 2 Clear To Send or interrupt input, active low
	SIN2	I	I / high	MODEM 2 Serial data receive
External control	SEL1	O medium	O / low	Select or general–purpose output, active high
	SEL2	O		
Parallel I/O	P[2:0]	I/O strong	I / low	Parallel I/O port
Parallel I/O	P[5:3]	I/O strong	O / low	Parallel I/O port
Miscellaneous	$\overline{TEST}$	I	I / high	Test mode enable, internally pulled–up, active low
	XPLLF	PLL	–	PLL Filter pin
Oscillator Power	VCCO	PWR	–	VCC supply for on–chip oscillator
	VSSO	GND	–	GND pin for on–chip oscillator
PLL Power	XVCC	PWR	–	VCC supply for PLL
	XVEE	GND	–	GND pin for PLL
PLL HF Power	XVCCHF	PWR	–	VCC supply for PLL HF
	XVEEHF	GND	–	GND pin for PLL HF
Core Power	VCCA	PWR	–	VCC supply for core
	VSSA	GND	–	GND pin for core
Buffers Power	VCCB	PWR	–	VCC supply for I/O buffers ring
	VSSB	GND	–	GND pin for I/O buffers ring

Table 1. TSS4550 Pin Description by Groups

Functional Description

Figure 1. highlights the different functions included in TSS4550, which are further detailed in this section. Figure 2. provides a more detailed view highlighting how the registers are mapped to functions. The register names are given besides each block, along with their read/write capability (R/W). They are further detailed in the Programming Interface section.

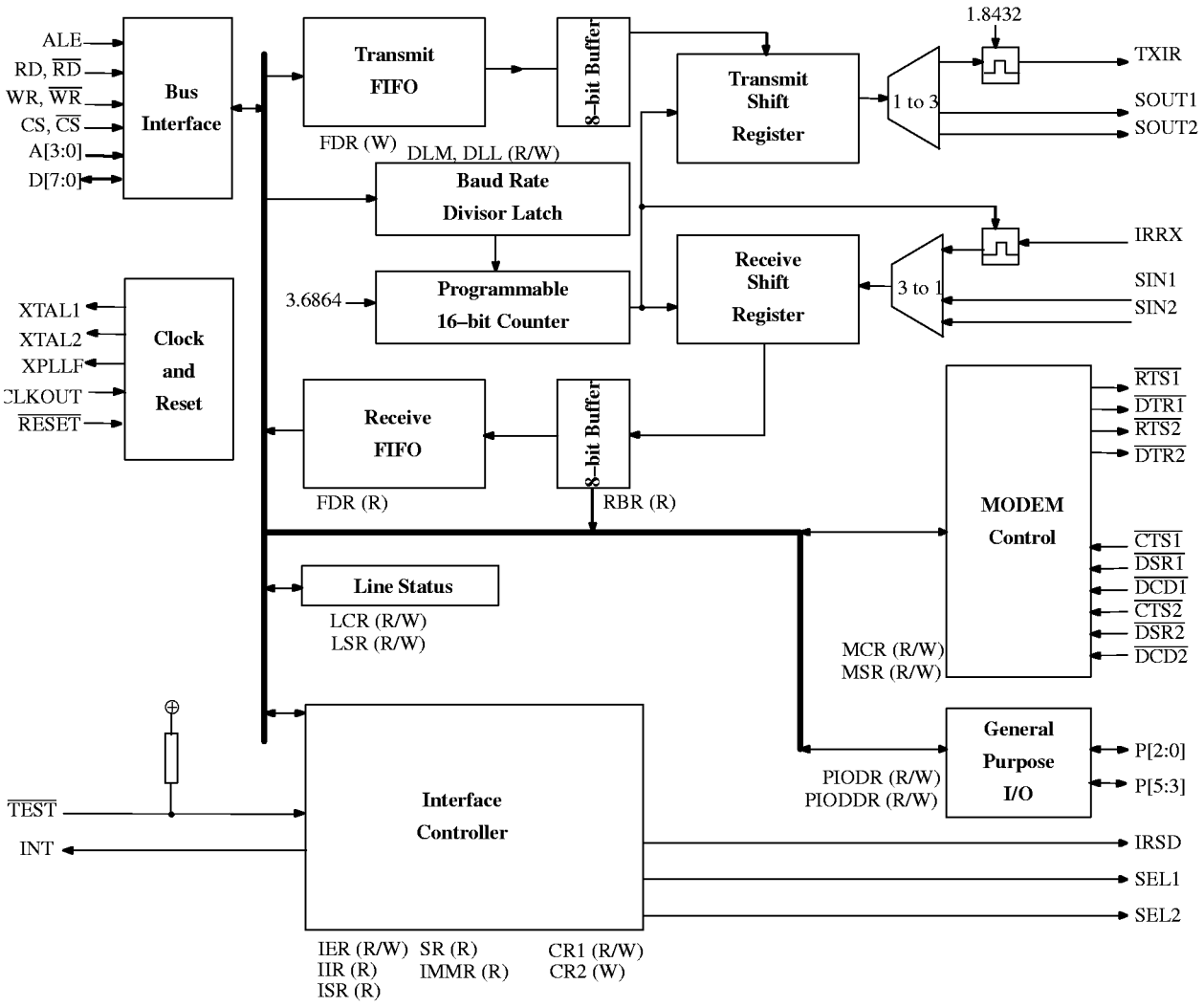


Figure 2. Detailed Block Diagram of TSS4550.

Transmit and Receive FIFO

The transmit and receive FIFO (see Figure 1.) are used to buffer the data between the UART and the external 8 bits data bus. These FIFO are 16 bytes deep in both directions, 8 bits wide in transmit (external bus to UART) and 10 bits wide in receive (UART to external bus). The wider receive path is used to convey the framing error and parity error information made available by the UART with each received byte. The received byte status bits are read from the FIFO using the status register (SR), see the Interface Controller section below.

UART / MODEM

The UART (see Figure 1.) is a high speed unit capable of operating at serial line speeds up to 115,200 bits/second from an internal clock input of 3.6864MHz. It supports the following signal lines: DTR, RTS, Serial output, DSR, DCD,

CTS and Serial input. Main UART operations are controlled and monitored by internal UART registers which are available at the external bus interface. Line status is made available with each received data byte and stored in the associated extra receive FIFO bits. Data transfers between the UART and FIFO are controlled by the Interface Controller block.

There is no automatic flow control, so DTR, RTS, DSR, DCD and CTS should be managed by software as required. If MODEM lines are not implemented, they can be used as general–purpose outputs or interrupt inputs.

There is no dedicated Ring Indicator input.

Multiplexer

The 1 to 3 multiplexer (see Figure 1.) is used to route the UART serial input/output and MODEM input signals to and from one of three ports: the IrDA 1.0 interface and two MODEM serial interfaces. The multiplexer is controlled by two bits in the Interrupt Mask and Misc. Register (IMMR).

Only the UART serial data and input signals are multiplexed. These are the Serial output, Serial input, DCD, CTS and DSR signals. The RTS and DTR signals for the two MODEM ports can be produced independently by software for each port using the MODEM Control Register (MCR).

IrDA 1.0 Pulse Shaping

TSS4550 may directly drive an external IrDA 1.0 transceiver through an internal pulse shaping circuit. The function is that of transmit pulse narrowing and receive pulse stretching. This unit generates transmit pulse widths of 1.6 µs nominal pulse width ($3/16^{ths}$ bit time of the maximum bit rate of 115,200 bits/second). At all times, the pulse shaper transmit output is kept in a state such that the transmit LED is normally off only being energized for the minimum on–times during data transmission. The pulse shaping circuit is reset by the PSRST bit in the Control Register 1 (CR1) or by the global hardware reset (RESET).

Interface Controller

The interface controller (see Figure 2.) provides control and monitoring of the data transfers between the external bus and FIFO and the UART and FIFO. It also allows the UART to be directly accessed by the external bus for UART control and monitoring. Additional miscellaneous control functions are provided for features such as enabling of external devices and parallel I/O.

It generates an external bus interrupt on the following conditions:

- Detection of an UART interrupt: changes in DSR, DCD or CTS, received characters with errors, break...
- Detection of receive FIFO becoming half–full.
- Detection of receive FIFO non–empty for longer than 3 character length times with no more characters being received.
- Detection of transmit FIFO becoming half–empty.
- Detection of toggling inputs on MODEM port 1 when not selected
- Detection of toggling inputs on MODEM port 2 when not selected

The received serial data from the UART is written into the receive FIFO and made available to the external bus via the FIFO Data Register (FDR – which is the output of the receive FIFO). The framing error and parity error bits (available from the UART along with each received byte) are also stored in the receive FIFO. These status bits are made available to the external bus in the Status Register (SR). When framing error or parity error information is needed, SR must be read before FDR is read. When FDR is read, the next data byte and associated status bits are popped off the FIFO so the SR locations are overwritten by the new status bits at the same time the data is available in FDR. If the status bits for a data byte are not read before reading another data byte, the status bits for the first byte will be overwritten with the status bits for the newly read data byte.

The receive FIFO will not be affected by external system reads whilst empty. An external read in these circumstances will not change FDR and SR contents. The receive FIFO will also not accept any more data from the UART when full.

Bytes received under these conditions will be lost and raise a FIFO overrun error on the first received byte and a UART overrun error on the second byte.

The transmit FIFO will not be affected by external system writes whilst full. An external write in these circumstances will not change FDR and SR contents and the written data will be lost.

Miscellaneous management functions are as follows:

- Provides reset and state control signals to internal TSS4550 functions – see also the section on Clocks, TSS4550 Disable and Reset below.
- Provides 2 general purpose control outputs (SEL1 and SEL2) for external devices (such as shutdown for RS232 transceivers).
- Provides a 6 bits wide parallel I/O port – P[5:0].

TSS4550 interrupt status is read in the Interrupt Status Register (ISR). This register shows the status of all interrupts within TSS4550, whether they are masked or not, except for the transmit FIFO half empty interrupt. This interrupt, when masked, will not generate a pending status in the ISR. An interrupt which is masked and becomes set is pending and will generate an external interrupt if unmasked. The interrupt mask status is readable in the Interrupt Mask and Misc. Register (IMMR).

Unused read/write strobe and chip select lines need only to be tied inactive. Multiplexed external buses are handled with the ALE signal, this can be tied high to provide a non–multiplexed bus interface or used to latch the address in either configuration.

Clocks, TSS4550 Disable and Reset

The main oscillator is controlled by an external 32.768kHz crystal. The oscillator output is internally fed to a Phase Locked Loop (PLL) to generate 3.6864MHz for the UART and IrDA interface. This 3.6864MHz clock is fed through a divide–by–two to provide 1.8432MHz for the IrDA pulse shaper. The on–chip oscillator output is buffered and fed to the external bus for real time clock reference. The oscillator may also be driven by an external signal source into the XTAL1 pin.

The on–chip oscillator is running continuously (as is the buffered clock output) but the rest of the clock chain (and TSS4550 PLL) may be disabled. This is achieved through the use of the CLKEN control bit in the Control Register 1 (CR1). When this bit is cleared, the PLL is disabled and the remainder of TSS4550 (except the on–chip oscillator) is held in a static mode with its outputs in a passive state. This state is explicitly defined as follows:

- The on–chip oscillator and buffered output (CLKOUT) are enabled but the clock to the PLL is stopped (or disabled).
- The CR1, CR2, IMMR and SR all operate normally but the other registers shall not be modified and may return undefined values.
- All outputs but the data bus are put into their rest state (the same as their reset state, See Table 1.).

TSS4550 is reset by a low logic level on the RESET pin. This forces several internal operations to take place:

- The FIFO pointers are cleared.
- The writeable TSS4550 registers are cleared resulting in a defined state for TSS4550 and its outputs (i.e. inactive).
- The UART is reset.
- The external peripherals connected to TSS4550 should be reset or shut down. This is accomplished by the setting of the rest state of TSS4550 control outputs: they are defined in Table 1.).

Programming Interface

Overview

TSS4550 provides the standard set of 16450 UART registers which are accessed in much the same way and at the same internal addresses as a discrete 16450.

TSS4550 also provides the following additional registers:

- FIFO Data Register: FDR.
- Control Register 1: CR1.
- Status Register: SR.
- Parallel I/O Data Register: PIODR.
- Parallel I/O Data Direction Register: PIODDR.
- Interrupt Status Register: ISR.
- Interrupt Mask & Misc. Register: IMMR.
- Control Register 2: CR2.

The following standard 16450 UART registers have a slightly modified utilization:

- MODEM Control Register: MCR.
- Receiver Buffer Register: RBR.
- Line Status Register: LSR.

The following standard 16450 UART registers are not available:

- Transmitter Holding Register: THR, use FDR instead.
- FIFO Control Register: FCR, use CR1, CR2 and IMMR instead.

All TSS4550 registers are detailed in the remainder of this section.

Note:

0x *is used to indicate a hexadecimal number*
X *is used to indicate undefined values*
R *is used to indicate Read–Only*
W *is used to indicate Write–Only*
R/W *is used to indicate Read/Write*

Register Summary

Table 2. gives the register list together with addresses and read/write capability.

A(3:0)[1]	DLAB[2]	Name	Read/ Write[5]	Reset Value	Description
0x0	0	RBR	R	XX	UART Receiver Buffer Register[6]
0x0	1	DLL	R/W	0x00	UART Divisor Latch (LSB)[8]
0x1	0	IER	R/W	00000000	UART Interrupt Enable Register
0x1	1	DLM	R/W	0x00	UART Divisor Latch (MSB)[8]
0x2	X[4]	IIR	R	00000001	UART Interrupt Identification Register
0x3	X[4]	LCR	R/W	0x00	UART Line Control Register
0x4	X[4]	MCR	R/W	0x00	UART Modem Control Register[3]
0x5	X[4]	LSR	R/W	01100000	UART Line Status Register[7]
0x6	X[4]	MSR	R/W	XXXX00X0	UART Modem Status Register
0x7	X[4]	SCR	R/W	XX	UART Scratch Register
0x8	X[4]	FDR	R/W	XX	FIFO Data Register
0x9	X[4]	CR1	R/W	00000X00	Control Register 1
0xA	X[4]	PIODR	R/W	00000XXX	Parallel I/O port Data Register
0xB	X[4]	PIODDR	R/W	00000000	Parallel I/O port Data Direction Register
0xC	X[4]	ISR	R	00XX0000	Interrupt Status Register
0xD	X[4]	IMMR	R/W	00000000	Interrupt Mask & Misc. Register
0xE	X[4]	SR	R	00000001	Status Register
0xF	X[4]	CR2	W	XXXXXXXX	Control Register 2

Table 2. TSS4550 Registers

Notes:

1) A(3:0) are the external address bus bits.
2) DLAB is the Divisor Latch Access Bit which is the MSB of the UART Line Control Register. Only relevant for UART register operations.
3) The use of bits in this standard 16450 register are modified for use in TSS4550.
4) Don't care state.
5) Read–only (R) registers have no effect when written to. Write–only (W) registers are undefined when read.
6) The UART Receiver Buffer Register is readable from the external bus but the data is always automatically read out by the receive FIFO as soon as it is received. The contents of this register are therefore not guaranteed.
7) The UART Line Status Register bits are handled in a different manner to the standard 16450.
8) The UART divisor latches require different values to those stated in the standard 16450 data sheet..
Reserved (–) registers have both characteristics.

Register Description

This section provides a detailed description of the bit fields of all TSS4550 registers.

The following notes apply to the description of the registers as highlighted by the Bit Mnemonics.

Notes:

** This bit must be handled with care or should not be used in normal operation.*
– Don't care bit: undefined when read and no effect when written to.
0 Reserved bit: 0 when read and must always be 0 when written to.

CR1 Control Register 1 (0x9, R/W)

7	6	5	4	3	2	1	0
PSRST	CLKEN	ESEL2	ESEL1	IRSD	–	RFCLR	TFCLR

Bit Number	Bit Mnemonic	Description
7	PSRST	**Pulse Shaper Reset** Set to logic 1 to bring the internal pulse shaper out of reset. Clear to initiate a reset of the internal pulse shaper.
6	CLKEN	**Internal Clock Enable** Set to logic 1 to asynchronously enable the internal clock PLL. Clear to asynchronously disable the internal clock PLL and hold the remaining TSS4550 functions (except the on–chip oscillator and buffered clock output) in a static state and output pins in the rest state (see Pin Description).
5	ESEL2	**External Device Select 2** The logic level of this bit is driven to SEL2 pin. The data read from this bit is not the actual logic value on the pin if there is an electrical conflict but the value previously written to SEL2.
4	ESEL1	**External Device Select 1** The logic level of this bit is driven to SEL1 pin. The data read from this bit is not the actual logic value on the pin if there is an electrical conflict but the value previously written to SEL1.
3	IRSD	**External IrDA Transceiver Shutdown** The logic level of this bit is driven to IRSD pin. The data read from this bit is not the actual logic value on the pin if there is an electrical conflict but the value previously written to IRSD.
2	–	–
1	RFCLR	**Receive FIFO Clear** Set to logic 1 to initiate a receive FIFO clear operation. The read and write pointers of the FIFO are cleared and the FIFO is emptied. This operation automatically clears all the UART line status flags (parity and framing errors) associated to the received data into the FIFO. However, the received data latched in the FIFO are not cleared. Clear to terminate the receive FIFO clear operation.
0	TFCLR	**Transmit FIFO Clear** Set to logic 1 to initiate a transmit FIFO clear operation. The read and write pointers of the FIFO are cleared and the FIFO is emptied. Clear to terminate the transmit FIFO clear operation.

CR2 Control Register 2 (0xF, W)

7	6	5	4	3	2	1	0
–	–	–	–	–	TIEN	RHFCLR	TIDIS

Bit Number	Bit Mnemonic	Description
7:3	–	–
2	TIEN	**Transmit FIFO Half Empty Interrupt Enable** To be used with TIDIS (see below) according to the following Table: TIEN TIDIS Function 0 0 Undefined 0 1 Disable THEINT (see ISR) 1 0 Enable THEINT (see ISR) 1 1 Undefined
1	RHFCLR	**Receive FIFO Half Full Flag Clear** Set to logic 1 to automatically clear RHFINT (see ISR). Clear not to clear RHFINT.
0	TIDIS	**Transmit FIFO Half Empty Interrupt Disable** To be used with TIEN (see above).

DLL Divisor Latch LSB (A=0x0, DLAB=1, R/W)

7	6	5	4	3	2	1	0
							(LS)

Bit Number	Bit Mnemonic	Description
7:0		This is the Least Significant Byte of the Divisor Latch. Recommended values for the Divisor Latch are given in Table 3.

DLM Divisor Latch MSB (A=0x1, DLAB=1, R/W)

15	14	13	12	11	10	9	8
(MS)							

Bit Number	Bit Mnemonic	Description
7:0		This is the Most Significant Byte of the Divisor Latch. Recommended values for the Divisor Latch are given in Table 3.

FDR FIFO Data Register (0x8, R/W)

7	6	5	4	3	2	1	0
(MS)							(LS)

Bit Number	Bit Mnemonic	Description
7:0		FDR has different usages when it is read or written to. It is used to read received characters out of the receive FIFO. One byte is used to store a received character and the Most Significant (MS) bits are set to 0 according to WLS (see LCR). Special care is needed not to loose status bit when reading FDR (See SR). It is used to buffer characters to send into the transmit FIFO. One byte is used to store a character and the Most Significant (MS) bits are discarded according to WLS (see LCR). Note: the least significant bits are transmitted first.

IER Interrupt Enable Register (A=0x1, DLAB=0, R/W)

7	6	5	4	3	2	1	0
0	0	0	0	EDSSI	ELSI*	ETBEI*	ERBFI*

Bit Number	Bit Mnemonic	Description
7:4	0	**0**
3	EDSSI	**Enable MODEM Status Interrupt** This bit enables the MODEM Status Interrupts (see MSR) of the selected MODEM (see IMMR) when set to logic 1. It must be set to logic 0 to disable the MODEM Status Interrupts or when the IrDA interface is selected.
2	ELSI*	**Enable Receiver Line Status Interrupt** This bit enables the Receiver Line Status Interrupts (see LSR) when set to logic 1. It disables the Receiver Line Status Interrupts when set to logic 0. As LSR may provide spurious information, it is recommended not to set this flag to prevent spurious interrupts. The status of the line should be checked as required when received data are ready (see ISR) or when closing the connection.
1	ETBEI*	**Enable Transmitter Buffer Empty Interrupt** This bit enables the Transmitter Holding Register Empty Interrupts when set to logic 1 (see THRE flag in LSR). As THR is automatically filled from the internal FIFO of the TSS4550, it is recommended not to enable this interrupt. Hence, in normal operation, this bit should always be set to a logic 0. ETHEINT (see IMMR), TIEN and TIDIS (see CR2) should be used instead.
0	ERBFI*	**Enable Received Data Available Interrupt** This bit enables the Received Data Available Interrupts when set to logic 1 (see DR flag in LSR). As the received data are automatically read out to the internal FIFO of the TSS4550, it is recommended not to enable this interrupt which may cause spurious events. Hence, in normal operation, this bit should always be set to a logic 0. ERTOINT and ERHFINT (see IMMR) should be used instead.

IIR Interrupt Identification Register (A=0x2, R)

7	6	5	4	3	2	1	0
0	0	0	0	0	ID1	ID0	IPF

Bit Number	Bit Mnemonic	Description
7:3	0	**0**
2:1	ID[1:0]	**Interrupt ID** In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in IIR. The four levels of priority are the following (from 1 the highest to 4 the lowest priority): ID[1:0] Level Type 11 1 Receiver Line Status 10 2 Received Data Ready 01 3 Transmitter Buffer empty 00 4 MODEM status When the CPU accesses IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is completed. This field is only significant when an enabled UART interrupt is pending (see IPF flag below).
0	IPF	**Interrupt Pending Flag** This bit is a logic 0 when an enabled UART interrupt is pending (see IER). It is a logic one otherwise. Interrupts which are disabled are not reported in IIR.

IMMR Interrupt Mask & Misc. Register (0xD, R/W)

7	6	5	4	3	2	1	0
MUX2	MUX1	EMPINT	PLLBP	ETHEINT	ERTOINT	ERHFINT	EUINT

Bit Number	Bit Mnemonic	Description
7:6	MUX[1:0]	**Line Multiplex** Value Selection 00 IrDA interface 01 MODEM serial interface 1 10 MODEM serial interface 2 11 IrDA interface
5	EMPINT	**Enable MODEM Port Interrupt** Set to logic 1 to allow MP1INT and MP2INT (see ISR) generating interrupts. Clear to mask MP1INT and MP2INT interrupts (besides MP1INT and MP2INT operation is unchanged).
4	PLLBP	**PLL By–Pass** Set to logic 1 to bypass the internal PLL. This connects the output of the on–chip oscillator directly to TSS4550 internal functions. This may be used when an external clock reference must be used. Clear for default operation with internal PLL and on–chip oscillator.
3	ETHEINT	**Enable Transmit FIFO Half Empty Interrupt** Set to logic 1 to allow THEINT (see ISR) generating interrupts. Clear to mask THEINT interrupts (besides THEINT operation is unchanged).
2	ERTOINT	**Enable Receiver Time–Out Interrupt** Set to logic 1 to allow RTOINT (see ISR) generating interrupts. Clear to mask RTOINT interrupts (besides RTOINT operation is unchanged).
1	ERHFINT	**Enable Receive FIFO Half Full Interrupt** Set to logic 1 to allow RHFINT (see ISR) generating interrupts. Clear to mask RHFINT interrupts (besides RHFINT operation is unchanged).
0	EUINT	**Enable UART Interrupt** Set to logic 1 to allow UINT (see ISR) generating interrupts. Clear to mask UINT interrupts (besides UINT operation is unchanged).

ISR Interrupt Status Register (0xC, R)

7	6	5	4	3	2	1	0
UOE	UBI	MP2INT	MP1INT	THEINT	RTOINT	RHFINT	UINT

Bit Number	Bit Mnemonic	Description
7	UOE	**UART Overrun Error Status** Set to logic 1 when UART has been overrun (see OE flag in LSR). Cleared when ISR is read. This is only a status bit not causing any interrupt (no mask is required). It should be checked as required when data are ready as indicated by RTOINT and RHFINT interrupt flags (see below).
6	UBI	**UART Break Interrupt Status** Set to logic 1 when UART has received a Break Interrupt (see BI flag in LSR). Cleared when ISR is read. This is only a status bit not causing any interrupt (no mask is required). It should be checked as required when data are ready as indicated by RTOINT and RHFINT interrupt flags (see below).
5	MP2INT	**MODEM Port 2 Interrupt** Set to logic 1 when MODEM port 2 is not selected (see MUX field in IMMR) and any one of the input signals (SIN2, DSR2, DCD2 or CTS2) has changed state. Cleared when MODEM port 2 is selected.
4	MP1INT	**MODEM Port 1 Interrupt** Set to logic 1 when MODEM port 1 is not selected (see MUX field in IMMR) and any one of the input signals (SIN1, DSR1, DCD1 or CTS1) has changed state. Cleared when MODEM port 1 is selected.
3	THEINT	**Transmit FIFO Half Empty Interrupt** Set to logic 1 when transmit FIFO has become half empty (8 or fewer bytes) and transmit FIFO automatic reads are in progress. Cleared when transmit FIFO becomes more than half full (more than 8 bytes). The value of this bit is not defined when the FIFO has been emptied. This interrupt should be masked (see ETHEINT in IMMR) when there is no data anymore to transmit.
2	RTOINT	**Receiver Time–Out Interrupt** Receive FIFO is not empty and has not received characters during 32 bit times (approximately 3 character times). The value of the bit time is set by the baud rate value. Cleared when the receive FIFO has been emptied.
1	RHFINT	**Receive FIFO Half Full Interrupt** Set to logic 1 when receive FIFO has become more than half full (more than 8 bytes) and receive FIFO automatic writes are in progress. Cleared when receive FIFO becomes half empty (8 or fewer bytes) and RHFCLR (see CR2) has been set.
0	UINT	**UART Interrupt** Set to a logic 1 when an enabled UART interrupt is pending (see IIR). It is a logic 0 otherwise.

LCR Line Control Register (0x3, R/W)

7	6	5	4	3	2	1	0
DLAB	BRK	STICK	EPS	PEN	STB	WLS1	WLS0

Bit Number	Bit Mnemonic	Description
7	DLAB	**Divisor Latch Access Bit** This bit, when set, gives access to the Divisor Latches of the baud generator through DLL and DLM registers. When it is cleared, RBR (Receiver Buffer Register) and IER (Interrupt Enable Register) are available instead.
6	BRK	**Break Transmission** It causes a break condition to be transmitted on the line. When it is set to a logic 1, the serial output (SOUT) is forced to a Spacing (logic 0) state. The break is terminated by setting this bit to a logic 0. The Break Transmission bit acts only on SOUT and has no effect on the transmission logic. Note: during the break, the transmitter can be used as a character timer to accurately establish the break duration.
5	STICK	**Stick Parity** When the parity is enabled (see PEN bit below), STICK forces the parity according to EPS. If EPS is a logic 0, the parity bit is generated or checked as a logic 1. If EPS is a logic 1, the parity bit is generated or check as a logic 0. When the parity is disabled, this bit is discarded.
4	EPS	**Even Parity Set** When the parity is enabled (see PEN bit below), EPS selects the parity bit. If Parity Stick is enabled (see STICK above) the parity bit does not depend of the character, otherwise it depends on the character as defined hereafter. When EPS is a logic 0, an odd number of logic 1 is generated or checked in the data word of the character and the parity bit. When EPS is a logic 1, an even number of logic 1 is generated or checked in the data word of the character and the parity bit. When the parity is disabled, this bit is discarded.
3	PEN	**Parity Enable** When this bit is set to a logic 1, a parity bit is generated (transmit data) or checked (receive data). When this bit is set to a logic 0, no parity bit is generated or checked. The parity bit is appended after the most significant bit of the character.
2	STB	**Stop Bits** 1 1,5 stop is added to 5 bits transmitted characters, 2 stop bits are added to 6, 7 and 8 bits transmitted character. 0 1 stop bit is added to the transmitted character.
1:0	WLS[1:0]	**Data Length** 11 8 bits character 10 7 bits character 01 6 bits character 00 5 bits character

LSR Line Status Register (0x5, R/W)

7	6	5	4	3	2	1	0
0	TEMT	THRE*	BI*	FE*	PE*	OE*	DR*

Bit Number	Bit Mnemonic	Description
7	0	**0**
6	TEMT	**Transmitter Empty** This bit is set whenever THR and the Transmitter shift register are both empty. It is reset whenever either THR or the Transmitter shift register are fed with data. As THR is automatically reloaded through the transmit FIFO when emptied, this bit can reliably be used to indicate there is no data anymore to transmit.
5	THRE*	**Transmitter Holding Register Empty** This bit is set whenever THR is empty. It is cleared when THR is automatically reloaded through the transmit FIFO. Due to this automatic filling, this bit may provide spurious information before LSR can be read by software. THEINT flag (see ISR) should be used instead to control the transmit data buffering.
4	BI*	**Break Interrupt** This bit is set whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (i.e. the total time of Start bit + data bits + Parity + Stop bits). It is cleared when RBR is read. Due to to the automatic read out of RBR by the receive FIFO, this bit may provide spurious information before LSR can be read by software. To provide a reliable error detection, this bit is latched in UBI flag (see ISR).
3	FE*	**Framing Error** This bit indicates that the received data character in RBR does not have a valid stop bit. It is set whenever the Stop bit following the last data (or parity when enabled) bit is detected as a logic 0 (Spacing level). It is cleared when RBR is read. Due to to the automatic read out of RBR by the receive FIFO, this bit may provide spurious information before LSR can be read by software. To provide a reliable error detection, this bit is stored in the FIFO with the received character (see RFE flag in SR).
2	PE*	**Parity Error** This bit indicates that the received data character in RBR does not have the correct parity (see parity configuration in LCR). It is set upon detection of a parity error. It is cleared when RBR is read. Due to to the automatic read out of RBR by the receive FIFO, this bit may provide spurious information before LSR can be read by software. To provide a reliable error detection, this bit is stored in the FIFO with the received character (see RPE flag in SR).
1	OE*	**Overrun Error** This bit indicates that data in RBR was not read before the next character was transferred into RBR. This will occur when the receive FIFO is full. As soon as data has been read out of the receive FIFO, it will automatically read out RBR, hence the overrun information will be cleared and this bit may provide spurious information before LSR can be read by software. To provide a reliable error detection, this bit is latched in UOE flag (see ISR).
0	DR*	**Data Ready** This bit is set to to a logic 1 whenever a complete incoming character has been received and transferred into RBR. It is cleared when the data is automatically read and feed into the receive FIFO. Hence, in normal operation, this bit will have spurious states and should not be used. RTOINT and RHFINT (see ISR) should be used instead to provide the data ready (in FIFO) information.

MCR MODEM Control Register (0x4, R/W)

7	6	5	4	3	2	1	0
0	0	0	LOOP	RTS2	DTR2	RTS1	DTR1

Bit Number	Bit Mnemonic	Description
7:5	0	**0**
4	LOOP	**Loop Back** The MODEM loop–back mode allows to test software. To use this mode, MODEM 1 must be selected (see MUX field of IMMR). Otherwise this bit must be set to logic 0. When this bit is set, the MODEM line are configured in loop–back: SOUT pin is set to the Marking (logic 1) state; SIN pin is disconnected and the output of the transmitter shift register is looped back internally to the input of the receiver shift register; the three MODEM Control input pins ($\overline{DSR1}$, $\overline{CTS1}$ and $\overline{DCD1}$) are disconnected; and the logic values of three programmable bits of MCR (DTR1, RTS1 and RTS2 respectively) are internally set to the MODEM control inputs (DSR, CTS and DCD respectively). Then DTR2 is discarded.
3	RTS2	**Request To Send 2** The value of this bit is used to control the state of $\overline{RTS2}$ pin. The data read from this bit is not the actual logic value on the pin if there is an electrical conflict but the value previously written to. When RTS2 is set, $\overline{RTS2}$ is driven to logic 0 . When RTS2 is cleared $\overline{RTS2}$ is driven to logic 1. When LOOP is set to logic 1, the value of this bit is used to program the state of DCD (see LOOP above).
2	DTR2	**Data Terminal Ready 2** The value of this bit is used to control the state of $\overline{DTR2}$ pin. The data read from this bit is not the actual logic value on the pin if there is an electrical conflict but the value previously written to. When DTR2 is set, $\overline{DTR2}$ is driven to logic 0 . When DTR2 is cleared $\overline{DTR2}$ is driven to logic 1.
1	RTS1	**Request To Send 1** The value of this bit is used to control the state of $\overline{RTS1}$ pin. The data read from this bit is not the actual logic value on the pin if there is an electrical conflict but the value previously written to. When RTS1 is set, $\overline{RTS1}$ is driven to logic 0 . When RTS1 is cleared $\overline{RTS1}$ is driven to logic 1. When LOOP is set to logic 1, the value of this bit is used to program the state of CTS (see LOOP above).
0	DTR1	**Data Terminal Ready 1** The value of this bit is used to control the state of $\overline{DTR1}$ pin. The data read from this bit is not the actual logic value on the pin if there is an electrical conflict but the value previously written to. When DTR1 is set, $\overline{DTR1}$ is driven to logic 0 . When DTR1 is cleared $\overline{DTR1}$ is driven to logic 1. When LOOP is set to logic 1, the value of this bit is used to program the state of DSR (see LOOP above).

MSR MODEM Status Register (0x6, R/W)

7	6	5	4	3	2	1	0
DCD	–	DSR	CTS	DDCD	–	DDSR	DCTS

Bit Number	Bit Mnemonic	Description
7	DCD	**Data Carrier Detect** This bit is the image of the DCD input of the selected MODEM (see MUX in IMMR). It is the logic complement of the corresponding $\overline{DCD1}$ or $\overline{DCD2}$ pin. When LOOP is set in MCR, this bit is equivalent to RTS2 in MCR. It is not significant if the IrDA interface is selected.
6	–	–
5	DSR	**Data Set Ready** This bit is the image of the DSR input of the selected MODEM (see MUX in IMMR). It is the logic complement of the corresponding $\overline{DSR1}$ or $\overline{DSR2}$ pin. When LOOP is set in MCR, this bit is equivalent to DTR1 in MCR. It is not significant if the IrDA interface is selected.
4	CTS	**Clear To Send** This bit is the image of the CTS input of the selected MODEM (see MUX in IMMR). It is the logic complement of the corresponding $\overline{CTS1}$ or $\overline{CTS2}$ pin. When LOOP is set in MCR, this bit is equivalent to RTS1 in MCR. It is not significant if the IrDA interface is selected.
3	DDCD	**Delta Data Carrier Detect** This bit is set when DCD has changed state since the last time MSR has been read (See DCD above). Then a MODEM Status interrupt is requested if enabled (See IER). It is automatically cleared as soon as MSR has been read.
2	–	–
1	DDSR	**Delta Data Set Ready** This bit is set when DSR has changed state since the last time MSR has been read (See DSR above). Then a MODEM Status interrupt is requested if enabled (See IER). It is automatically cleared as soon as MSR has been read.
0	DCTS	**Delta Clear To Send** This bit is set when CTS has changed state since the last time MSR has been read (See CTS above). Then a MODEM Status interrupt is requested if enabled (See IER). It is automatically cleared as soon as MSR has been read.

PIODR Parallel I/O Port Data Register (0xA, R/W)

7	6	5	4	3	2	1	0
–	–	P5	P4	P3	P2	P1	P0

Bit Number	Bit Mnemonic	Description
7:6	–	–
5:0	P[5:0]	**Parallel I/O Port Data** The logic levels of these bits are driven to the corresponding pins of the parallel I/O port if the corresponding data direction bits (see PIODDR) are set for output. The data read from this register reflect the actual logic state of the parallel I/O port pins, not necessarily the value written to it.

PIODDR Parallel I/O Port Data Direction Register (0xB, R/W)

7	6	5	4	3	2	1	0
0	0	PD5	PD4	PD3	PD2	PD1	PD0

Bit Number	Bit Mnemonic	Description
7:6	–	–
5:3	PD[5:3]	**Parallel I/O Port (resting as output) Direction** Set to logic 1 the port direction bit to configure the corresponding I/O pin as an input. Clear the port direction bit to configure the corresponding I/O pin as an output.
2:0	PD[2:0]	**Parallel I/O Port (resting as input) Direction** Set to logic 1 the port direction bit to configure the corresponding I/O pin as an output. Clear the port direction bit to configure the corresponding I/O pin as an input.

RBR Receiver Buffer Register (A=0x0, DLAB=0, R)

7	6	5	4	3	2	1	0
(MS)							(LS)

Bit Number	Bit Mnemonic	Description
7:0		This register is automatically read by the receive FIFO and FDR should be used instead.

SCR Scratch–pad Register (0x7, R/W)

7	6	5	4	3	2	1	0

Bit Number	Bit Mnemonic	Description
7:0		This register can be used to store and recall temporary 8–bit data.

SR Status Register (0xE, R)

7	6	5	4	3	2	1	0
–	PLOCK	FOVR	RPE	RFE	RFERR	TXFF	RXFE

Bit Number	Bit Mnemonic	Description
7	–	–
6	PLOCK	**PLL Locked** Set to logic 1 to indicate the PLL is locked. Software should test this bit once the PLL clock has been enabled (see CLKEN in CR1) before allowing transmission. Clear while PLL is tracking. This continuously occurs during normal operation to compensate frequency shifts and is not an indication of unstable operation if PLOCK has previously been detected to a logic 1. The tracking parameters are adjusted by an external RC filter (see PLL Filter).
5	FOVR	**FIFO Overrun** Set to logic 1 when the receive FIFO is full and at least one byte is waiting in the UART receiver (RBR and receive shift register). Cleared when SR is read or the receive FIFO is cleared (see RFCLR in CR1).
4	RPE	**Next FDR Read Parity Error** Set to logic 1 to indicate a parity error associated to the received data in FDR. Cleared when there is no parity error associated to the received data in FDR. This bit is overwritten each time FDR is read. It must be read before the associated data in order not to be lost.
3	RFE	**Next FDR Read Framing Error** Set to logic 1 to indicate a framing error associated to the received data in FDR. Cleared when there is no framing error associated to the received data in FDR. This bit is overwritten each time FDR is read. It must be read before the associated data in order not to be lost.
2	RFERR	**Received FIFO Contains ERROR** This bit is set whenever any of the parity or framing error bits of the received data characters has been activated. When the corrupted data character is read out of the receive FIFO, the associated error bits within the FIFO are not cleared. This flag is automatically cleared when the FIFO has been emptied by reading FDR. If the FIFO is continuously filling in at the same time it is emptied without being fully emptied, the flag will only disappear when all the corrupted entries have been used again to store good characters. This flag is also cleared when the receive FIFO is cleared (see RFCLR in CR1).
1	TXFF	**Transmit FIFO Full** Set to logic 1 when the transmit FIFO is full. Cleared whilst the transmit FIFO is not full.
0	RXFE	**Receive FIFO Empty** Set to logic 1 when the receive FIFO is empty. Cleared whilst the receive FIFO contains data.

Application

TSS4550 Application Block Diagram

TSS4550 may be connected to any microcontroller or microprocessor with an external 8–bit memory interface. Figure 3. shows a typical application where TSS4550 is connected to a standard C51/C251 microcontroller. The microcontroller generates an active high power–on which is buffered and inverted to reset TSS4550. Only one 8–bit port is enough to interface the multiplexed address/data bus which leaves 20 I/Os for the microcontroller internal peripherals or general–purpose usage. Two outputs of the microcontroller are used to generate read and write signals (P3.7/$\overline{RD}$, P3.6/$\overline{WR}$). Two inputs of the microcontroller are used for TSS4550 interrupts (P3.2/$\overline{INT0}$) and a real–time clock timer (P3.4/T0). The Decoding Logic (typically a zero–power PLD such as Atmel ATF16LV8CZ) allows to select TSS4550 among the external peripherals which depend of the target application and are not represented here. If TSS4550 is connected to a microcontroller with a non–multiplexed address/data bus then ALE must be tied to a logic high level. Unused control signals (CS, RD and WR) are connected to a logic low level (inactive).

TSS4550 is directly connected to an IrDA–SIR transceiver (typically a Vishay–Telefunken TFDS4500, please refer to TFDU4100 data sheet for the recommended circuit diagram of this device). It is also directly connected to RS232 transceivers (the select control output may be connected to an active low shut down input or inverted to control an active low enable input).

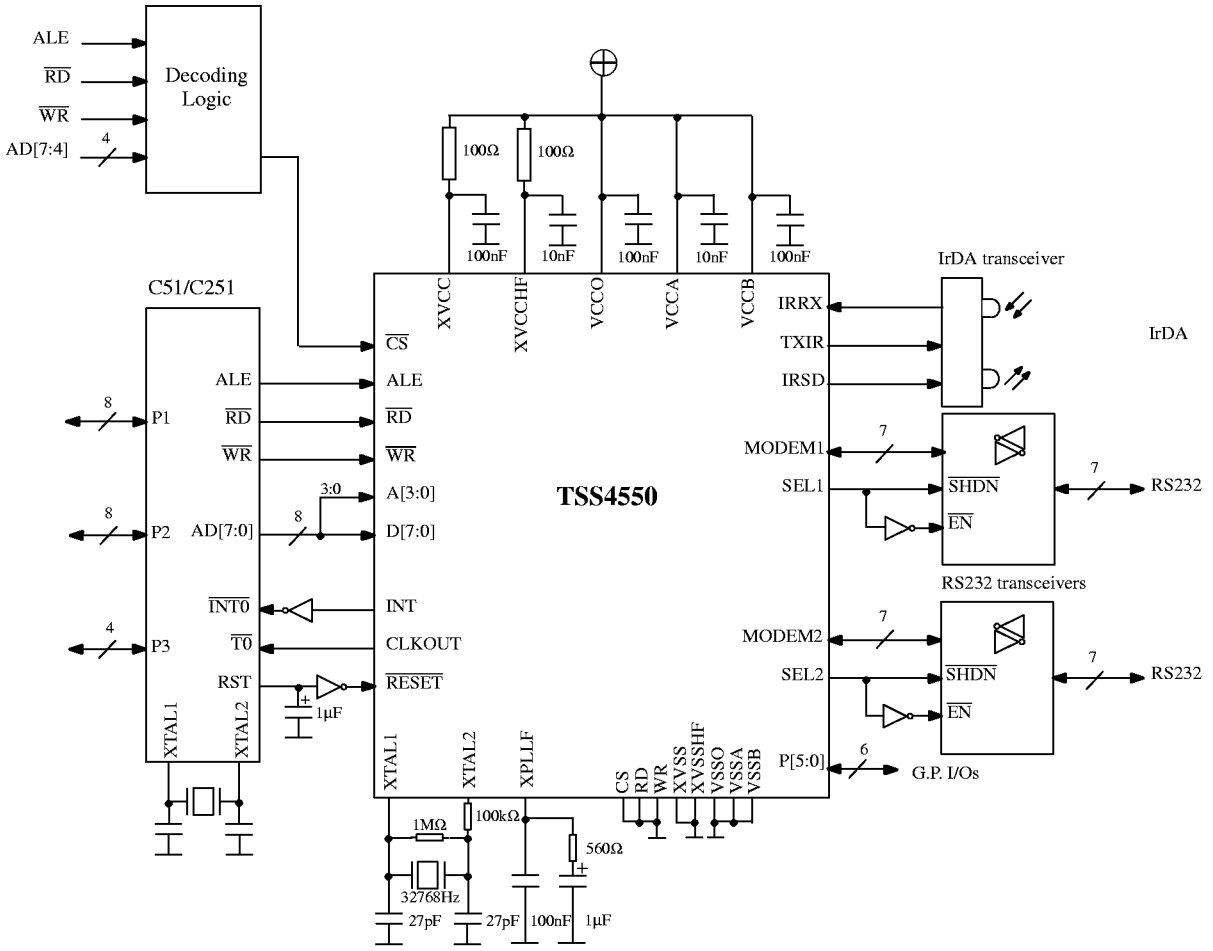


Figure 3. TSS4550 Application Block Diagram

Oscillator

The RC network used with the external 32768Hz crystal insures the oscillator stability and start–up while minimizing the power consumption.

Power supply filtering and PLL filtering are addressed below.

Power Supply

The separated power supply lines and the very low power consumption simplifies EMC friendly designs. A RC filter can be added on the power supply line of the HF part of the PLL to prevent high frequency noise emission through the power supply line. A RC filter can also be added on the other PLL power supply to prevent any modulation of the PLL output. Typical values are shown in Figure 3.

To further reduce the power consumption, a low–cost MOSFET can be used to switch off the oscillator power supply when the clock is not needed.

PLL Filter

The Phase Locked Loop (PLL) within TSS4550 operates from the on–chip oscillator and generates the 1.8432MHz and 3.6864MHz signals required by IrDA pulse shaper and UART respectively. This PLL requires an external loop filter which is provided by external capacitors connected to XPLLF.

The topology of this filter is as shown in Figure 4. :

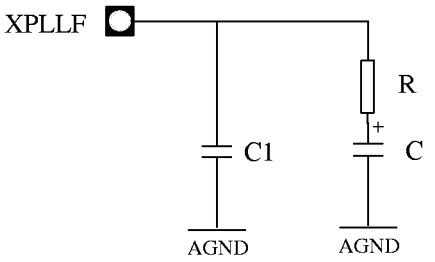


Figure 4. TSS4550 PLL Filter Network.

Note:
XPLLF is a "hot point" considering the high BWA value (see below). This wire should be as short as possible and can be protected by a guard ring to prevent any modulation of the PLL output.

Values for the external RC filter network can be calculated based on an initial value for the Band Width Attenuation factor (BWA). This is the total filter band width compared to the input frequency. BWA should be greater than 100 though the loop lock time increases as BWA increases.

The design equations for component value calculation are as follows:

$$C = BWA^2 \times 8.52 \times 10^{-11}(F)$$

$$R2 = \frac{BWA}{C} \times 4.973 \times 10^{6}(\Omega)$$

$$C1 = \frac{BWA}{R2} \times 4.973 \times 10^{7}(\Omega)$$

Typical recommended values are as follows: C = 1 µF, then BWA = 108, R2 = 540Ω (use 560Ω) and C1 = 100 nF.

UART Baud Rate

The UART within TSS4550 normally runs at a clock speed of 3.6864MHz. Then the baud rate divisors are as shown in Table 3. :

Desired baud rate	Divisor required
50	0x1200
75	0x0C00
110	0x082E
134.5	0x06B2
150	0x0600
300	0x0300
600	0x0180
1200	0x00C0
1800	0x0080
2000	0x0074
2400	0x0060
3600	0x0040
4800	0x0030
7200	0x0020
9600	0x0018
19200	0x000C
38400	0x0006
57600	0x0004
115200	0x0002

Table 3. UART Baud Rate Divisor Values at 3.6864 MHz

Note:
A TSS4550 reset will clear the baud rate Divisor Latch registers. This means that the UART baud rate has to be reset up following a reset.

Test Modes

TSS4550 has multiple test modes which are controlled by the test mode pin in conjunction with other pins, as defined in Table 4. :

Test	P0	P1	P2	IRRX	Test Mode
0	0	0	0	1	Hi–Z
0	1	0	0	1	Pin Test
0	0	1	0	1	PLL Function Test
0	X	X	1	1	Reserved
0	X	X	X	0	Reserved for factory test

Table 4. TSS4550 Test Modes

Hi–Z Test Mode

In this test mode, all TSS4550 output buffers are asynchronously disabled. The internal state of TSS4550 is not directly altered by this test mode.

Pin Test Mode

In this test mode, all TSS4550 signal pins (except the on–chip oscillator pins) are connected internally to one big notional XOR gate, the output of which is routed to the SEL2 output pin. The input pad of each signal is fed into this XOR gate. This means that driving any signal to the opposite state of its rest state whilst in this test mode will cause a transition on the SEL2 pin. Table 1. defines the rest state of all TSS4550 pins.

PLL Function Test Mode

In this test mode, the internal PLL output is disconnected from the remainder of TSS4550 but its input is still driven by the on–chip oscillator. The internal state of TSS4550 is not directly altered by this test mode except that the internal 3.6864MHz clock is stopped. Internal PLL signals are routed out to external TSS4550 pins to enable the PLL operation to be inspected (See Table 5.):

TSS4550 Pin	PLL Test Mode Signal	Description
P3	VCO / 8	3.6864 MHz output
P4	LOCK	PLL lock state output
SEL1	VCO / 100	295 kHz output
SEL2	VCO	29.5 MHz output

Table 5. TSS4550 PLL Test Mode Outputs

Electrical Specification

Absolute Maximum Ratings

DC supply voltage (Vdd)	–0.5V min. to +7V max.
DC input/output voltage	0V to Vdd +0.5V.
Operating temperature	–40°C min. to +85°C max.
Storage temperature	–65°C min. to +145°C max.

Stresses at or above those listed may cause permanent damage to the device. Exposure to absolute Maximum ratings conditions for extended period may affect devices.

Table 6. TSS4550 Absolute Maximum Ratings

DC Characteristics

The following characteristics are specified at Vdd = 2.7V to 5.5V over an operating temperature of 0°C to +70°C for Commercial and –40°C to +85°C for Industrial.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Comment
V_{IH}	CMOS input high level	0.7xVdd			V	
V_{IL}	CMOS input low level			0.3xVdd	V	
V_{OH}	CMOS output high level	0.9xVdd			V	IOH (normal, medium, strong) = +3 mA, +6 mA, +12 mA @4.5V = +1 mA, +2 mA, +4 mA @2.7V
V_{OL}	CMOS output low level			0.1xVdd	V	IOL (normal, medium, strong) = –3 mA, –6 mA, –12 mA @4.5V = –1.5 mA, –3 mA, –6 mA @2.7V
I_{IN}	Input leakage current no internal pull–up internal pull–up	 –1 –100	 –50	 +1 	 µA µA	 VIN = VDD or GND VIN = GND
I_{OZ}	Output tri–state leakage current	–1		+1	µA	VOUT = VDD or GND
C_{IN}	Input capacitance			5	pF	
C_{OUT}	Output capacitance			5	pF	
C_{IO}	Transceiver capacitance			5	pF	
IDD_S	Standby current @3.6V Standby current @5.5V		20 35	 70	µA	Only on–chip oscillator running, all other functions & I/O static
IDD_R	Operating current @3V Operating current @5V		1 2		mA	Main clock PLL running, UART, FIFO & IrDA in operation
VDD_S	Standby supply voltage	2.3			V	Minimum standby voltage for state retention and on–chip oscillator operation

Table 7. TSS4550DC Operating Conditions

AC Characteristics

IrDA AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Comment
T_{TXW}	Infrared transmit output pulse width		1.63		µs	IrDA 1.2 compliant
T_{TLTH}	Infrared transmit output rise time			10	ns	Negligible
T_{TLTH}	Infrared trasnmit output falling time			10	ns	Negligible
T_{RXW}	Infrared receive input pulse width	1.4	1.63	88.5	µs	IrDA 1.2 compliant

Table 8. IrDA AC Characteristics

External Bus Write Cycles

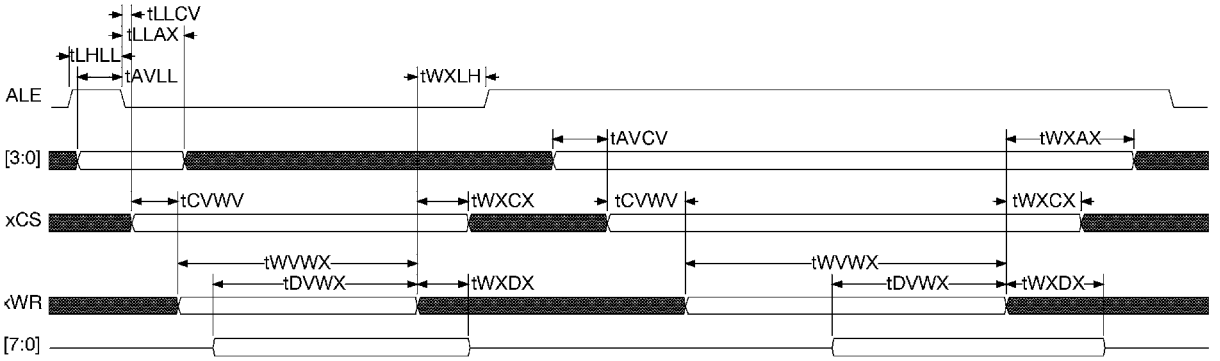


Figure 5. External Bus Write Cycles

Name	Min	Max	Comment
tLHLL	20		ALE pulse width
tAVLL	8		Address setup time to ALE falling edge
tLLAX	20		Address hold time from ALE falling edge
tLLCV	0		ALE setup time to Chip Select active
tCVWV	20		Chip Select setup time to Write Strobe active
tWXCX	20		Chip Select hold time from Write Strobe inactive
tWXLH	20		ALE hold time from Write Strobe inactive
tAVCV	0		Address setup time to Chip Select active
tWXAX	20		Address hold time from Write Strobe inactive
tWVWX	100		Write Strobe pulse width
tDVWX	20		Data setup time to Write Strobe active
tWXDX	20		Data hold time from Write Strobe inactive

Table 9. External Bus Write Cycles

External Bus Read Cycles

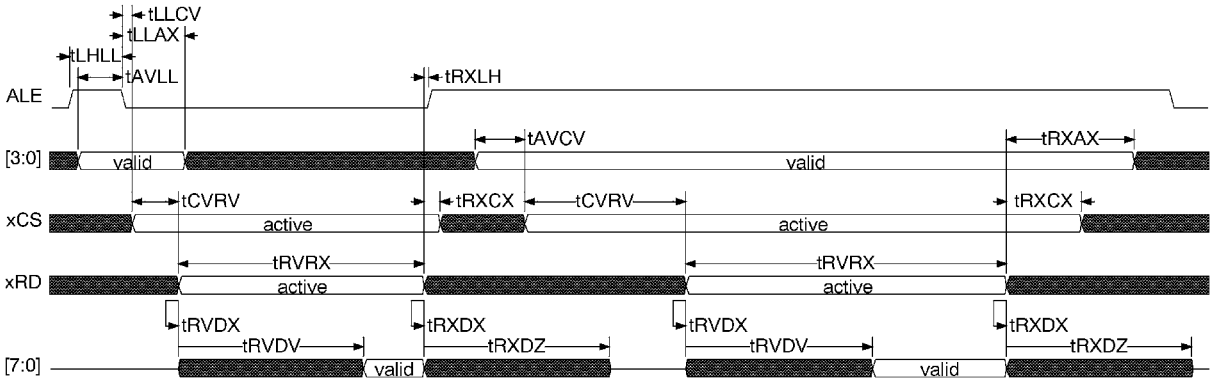


Figure 6. External Bus Read Cycles

Symbol	Min	Max	Comment
tLHLL	20		ALE pulse width
tAVLL	8		Address setup time to ALE falling edge
tLLAX	20		Address hold time from ALE falling edge
tLLCV	0		ALE setup time to Chip Select active
tCVRV	20		Chip Select setup time to Read Strobe active
tRXCX	0		Chip Select hold time from Read Strobe inactive
tRXLH	0		ALE hold time from Read Strobe inactive
tAVCV	0		Address setup time to Chip Select active
tRXAX	0		Address hold time from Read Strobe inactive
tRVRX	100		Read Strobe pulse width
tRVDV		80	Data valid delay from Read Strobe active
tRVDX	0		Data driven delay from Read Strobe active
tRXDX	0		Data hold time from Read Strobe inactive
tRXDZ		80	Data Hi–Z delay from Read Strobe inactive

Table 10. External Bus Read Cycles

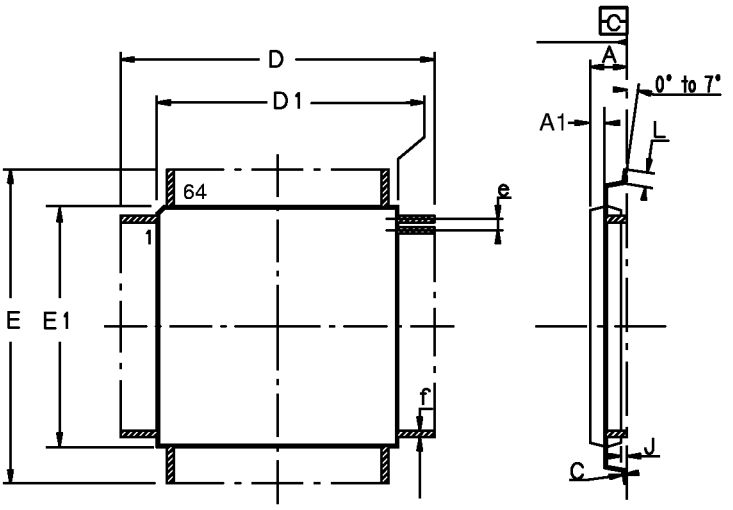
Oscillator AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Comment
F_{OSC}	Oscillator input frequency		32768		Hz	With external oscillator and PLL by-pass for maximum value
T_{SUP}	Oscillator start–up time			10	ms	
D_{OSC}	Oscillator duty cycle	40		60	%	
J_{PLL}	PLL Clock output Jitter				%	In typical application conditions

Table 11. Oscillator AC Characteristics

TQFP64

Mechanical Outline



Package Size

	MM		INCH	
	Min	**Max**	**Min**	**Max**
A	–	1.60	–	.063
A1	0.64 REF		.025 REF	
C	0.17 BSC		0.007 BSC	
D	11.75	12.25	.463	.483
D1	9.90	10.10	.390	.398
E	11.75	12.25	.463	.483
E1	9.90	10.10	.390	.398
e	0.50 BSC		.0197 BSC	
f	0.25 BSC		.010 BSC	
J	0.05	–	.002	–
L	0.45	0.75	.018	.030

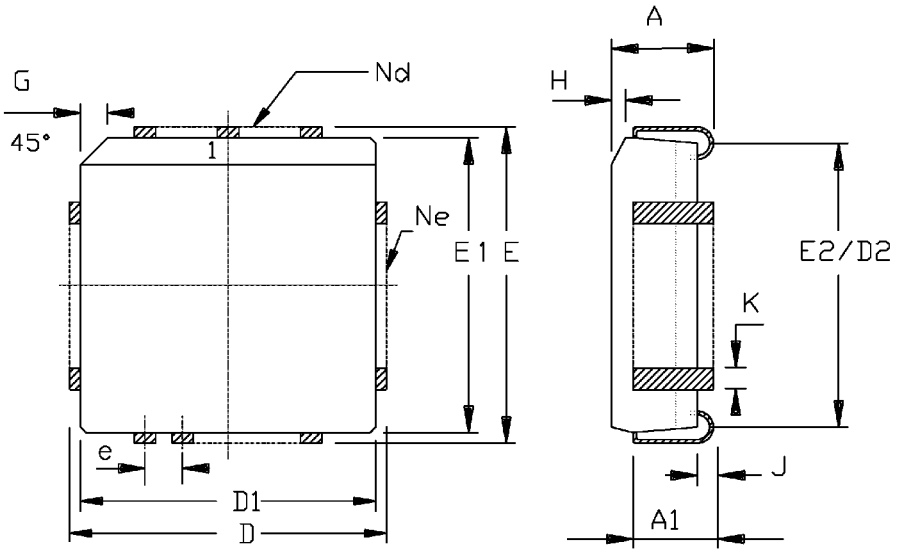
Pin Assignement

Pin Number	Pin Name	Pin Number	Pin Name
1	XVEE1	33	$\overline{WR}$
2	XVCCHF	34	CS
3	XVEEHF	35	$\overline{CS}$
4	VCCA	36	$\overline{RESET}$
5	P0	37	IRRX
6	P1	38	TXIR
7	P2	39	IRSD
8	P3	40	RTS1
9	P4	41	DTR1
10	CLKOUT	42	SOUT1
11	VSSO	43	DSR1
12	XTAL2	44	VSSB1
13	XTAL1	45	DCD1
14	VCCO	46	CTS1
15	A0	47	P5
16	A1	48	INT
17	A2	49	SIN1
18	A3	50	RTS2
19	D0	51	DTR2
20	D1	52	SOUT2
21	D2	53	VSSA1
22	VSSB2	54	DSR2
23	D3	55	DCD2
24	D4	56	CTS2
25	D5	57	$\overline{TEST}$
26	D6	58	SIN2
27	D7	59	SEL1
28	VCCB2	60	SEL2
29	ALE	61	VCCB1
30	RD	62	XVEE2
31	$\overline{RD}$	63	XVCC1
32	WR	64	XPLLF

Table 12. TSS4550 TQFP64 Numeric Signal List

PLCC68

Mechanical Outline



Package Size

	MM		INCH	
A	4.20	5.08	.165	.200
A1	2.29	3.30	.090	.130
D	25.02	25.27	.985	.995
D1	24.13	24.33	.950	.958
D2	22.61	23.62	.890	.930
E	25.02	25.27	.985	.995
E1	24.13	24.33	.950	.958
E2	22.61	23.62	.890	.930
e	1.27	BSC	.050	BSC
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	–	.020	–
K	0.33	0.53	.013	.021
Nd	17		17	
Ne	17		17	

Pin Assignement

Pin Number	Pin Name	Pin Number	Pin Name
1	$\overline{\text{TEST}}$	35	D5
2	SIN2	36	D6
3	SEL1	37	D7
4	SEL2	38	VCCB
5	VCCB	39	VCCB
6	XVEE	40	ALE
7	XVCC	41	RD
8	XPLLF	42	$\overline{\text{RD}}$
9	XVEE	43	WR
10	XVCCHF	44	$\overline{\text{WR}}$
11	XVEEHF	45	CS
12	VCCA	46	$\overline{\text{CS}}$
13	VCCA	47	$\overline{\text{RESET}}$
14	P0	48	IRRX
15	P1	49	TXIR
16	P2	50	IRSD
17	P3	51	RTS1
18	P4	52	DTR1
19	CLKOUT	53	SOUT1
20	VSSO	54	DSR1
21	XTAL2	55	VSSB
22	XTAL1	56	VSSB
23	VCCO	57	DCD1
24	A0	58	CTS1
25	A1	59	P5
26	A2	60	INT
27	A3	61	SIN1
28	D0	62	RTS2
29	D1	63	DTR2
30	D2	64	SOUT2
31	VSSB	65	VSSA
32	VSSB	66	DSR2
33	D3	67	DCD2
34	D4	68	CTS2

Table 13. TSS4550 PLCC68 Numeric Signal List

Ordering Information

TSS4550–CAB	Commercial, TQFP64, Tape & Reel with Dry Pack	Reel* of 1500
TSS4550–CAD	Commercial, TQFP64, Dry Pack	Tray of 160, box of 800
TSS4550–DK	**Design Kit**	
TSS4550–IAB	**Industrial, TQFP64, Tape & Reel with Dry Pack**	Reel* of 1500
TSS4550–IAD	**Industrial, TQFP64, Dry Pack**	Tray of 160, box of 800
TSS4550–IB	**Industrial, PLCC68**	Box of 304
TSS4550–XY	**Wafer on ring**	

** Tape information: tape width 24 mm, part to part pitch 16 mm, reel diamater 330 mm (13")*

Product Marking

TEMIC

TSS4550–IB

YYWW Lot Number