

100mA Dual H-Bridge Air-Core Gauge Driver

Description

The CS3750 is a dual H-bridge four quadrant air-core gauge driver. The IC provides all the functions necessary to drive a tachometer or speedometer as part of a microprocessor based multiplexed system. Digital input control eliminates the need for any analog calibration of the gauge.

The controlling microprocessor sends out a PWM signal to each H bridge driver input (IN1, IN2). The PWM signal duty cycle is proportional to the H-bridge output. Output current

(100mA max) direction is controlled by the DIRECTION input. PWM switching noise is minimized at each half bridge by an internal RC filter and external programmable capacitor.

The CS3750 is protected against 50V load dump, over voltage and thermal runaway fault conditions. Any of these faults causes the IC to shut down. Each high side of the output driver is current limited. A short circuit condition in one driver does not affect the others.

Features

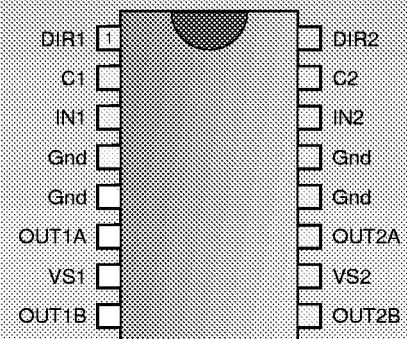
- 2 Independent NPN H-Bridge Drivers
- No Analog Trim Required
- Used in Multiplexed Systems
- Quiet Gauge Operation
- Programmable Slew Rate Minimizes Switching Noise
- Fault Protection
 - Over Voltage
 - Thermal Shutdown
 - Short Circuit

Absolute Maximum Ratings

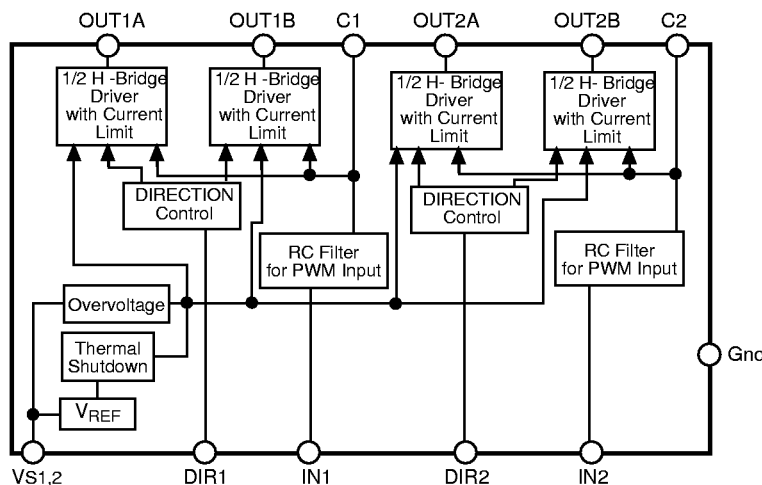
Supply Voltage.....	16V
Internal Power Dissipation.....	Internally limited
Logic Input Voltages.....	-0.3V to 6.5V
Junction Temperature Range.....	-40°C to +150°C
Storage Temperature Range.....	-55°C to +165°C
Lead Temperature Soldering	
Wave Solder (through hole styles only).....	10 sec. max, 260°C peak
Electrostatic Discharge (Human Body Model).....	4kV

Package Options

16 Lead PDIP
(internally fused leads)



Block Diagram



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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Output Stage					
V_{OUT} Saturation Voltage (Low Side)	$I_{OUT} = 100mA$; $V_{IN} = 0V$ $I_{OUT} = 1mA$; $V_{IN} = 0V$		0.25 0.01	0.50 0.10	V V
V_{OUT} Offset Voltage	$V_C = 5V$; $I_{OUT} = -30mA$		15	50	mV
V_{OUT} Saturation High Side Low Side	$V_{IN} = 5V$; $I_{OUT} = -100mA$ $V_{IN} = 0V$; $I_{OUT} = -1mA$	VS-2	VS-1.5	VS	V V
V_{OUT} Differential Matching Voltage	$V_C = 5V$, $I_{OUT} = -100mA$			100	mV
Supply Current	$V_{IN} = V_{DIR} = 0$;		23	45	mA
■ Input Stage					
V_{IN} LOW HIGH Hysteresis	V_{IN} decreasing; $V_{DIR} = 0V$ V_{IN} increasing; $V_{DIR} = 0V$ $V_{DIR} = 0V$	0.8	1.9 2.0 100		V V mV
I_{IN} LOW HIGH	$V_{IN} = 0.8V$; $V_{DIR} = 0V$ $V_{IN} = 3.5V$		20 0.4	100 100.0	μA μA
Output Slew Rate with respect to input	$V_{IN} = 250Hz$; $R_{LOAD} = 150\Omega$		0.2	0.8	V/ μs
Output Turn on Delay with respect to input	$V_{IN} = 250Hz$; $R_{LOAD} = 150\Omega$, note 1		1.5	6	μs
Output Turn off Delay with respect to input	$V_{IN} = 250Hz$; $R_{LOAD} = 150\Omega$, note 2		2.4	9	μs
■ Direction					
V_{DIR} LOW HIGH Hysteresis	$V_{IN} = 5V$; V_{DIR} decreasing $V_{IN} = 5V$; V_{DIR} increasing $V_{IN} = 5V$	0.8	1.9 2.0 100		V V mV
I_{DIR} LOW HIGH	$V_{IN} = 0V$; $V_{DIR} = 0.8V$ $V_{IN} = 0V$; $V_{DIR} = 3.5V$		40 0.4	100 100	μA μA
Output Slew Rate with respect to DIR	$V_{IN} = 5V$; $f_{DIR} = 250Hz$; $C = 0\mu F$	0.2	1.5		V/ μs
Output Fall Time with respect to DIR	$V_{IN} = 0V$; $V_{DIR} = 0V$; $C = 0\mu F$		0.2	2.0	μs
Output Turn on Delay with respect to DIR	$V_{IN} = 5V$; $R_{LOAD} = 150\Omega$ $V_{DIR} = 250Hz$; $C = 0\mu F$, note 1		1	6	μs
Output Turn off Delay with respect to DIR	$V_{IN} = 5V$; $R_{LOAD} = 150\Omega$ $V_{DIR} = 250Hz$; $C = 0\mu F$, note 2		2.5	9	μs
■ Protection Functions					
I_{OUT} Current Limit (High Side Only)	$V_{IN} = 5V$	100	225		mA
Over Voltage Threshold Hysteresis	$V_{IN} = 5V$	17.0	21.5 0.5	26.0	V V
Thermal Shutdown Hysteresis			160 20		$^{\circ}C$ $^{\circ}C$

Note 1: Time required for output signal to rise to 90% of its amplitude after input signal switches.

Note 2: Time required for output signal to decrease to 10% of its amplitude after input signal switches.

Package Pin Description

PACKAGE PIN #	PIN SYMBOL	FUNCTION
16L PDIP (internally fused leads)		
1	DIR1	CMOS compatible input pin controls direction of current through OUT1
2	C1	RC filter capacitor for OUT1 connected to Ground
3	IN1	CMOS compatible input pin controls output OUT1A and 1B
4,5,12,13	Gnd	Ground connection
6	OUT1A	One half of H-bridge output stage 1
7	VS1	Supply voltage
8	OUT1B	One half of H-bridge output stage 1
9	OUT2B	One half of H-bridge output stage 2
10	VS2	Supply voltage
11	OUT2A	One half of H-bridge output stage 2
14	IN2	CMOS compatible input pin controls output OUT2A and 2B
15	C2	RC filter capacitor for OUT2 connected to Ground
16	DIR2	CMOS compatible input pin controls direction of current through OUT2

Circuit Description

Output Stage

Each output stage contains 4 power NPN transistors arranged in a traditional H bridge configuration. Current flow through the two outputs (OUTxA, OUTxB) in each H-bridge is controlled by the logic signal DIRx.

PWM input signals from the microprocessor, are filtered on chip and sent to the output stage. The duty cycle of the PWM signal is proportional to output voltage. The RC filter reduces the noise of the PWM input signal by slowing its slew rate: i.e., the output signal is converted from a square wave to an exponential sawtooth waveform. An external capacitor (Cx) controls the slew rate for each H bridge.

Motor Direction Control

When the voltage on the control pin (INx) is low, both halves of the H bridge are off (Table 1). When INx is high, DIR controls the flow of current through the H-bridge. If DIRx=0, current flows from OUTxA out to the coil and back in through OUTxB. If DIRx=1, current flows from OUTxB out to the coil and back in through OUTxA.

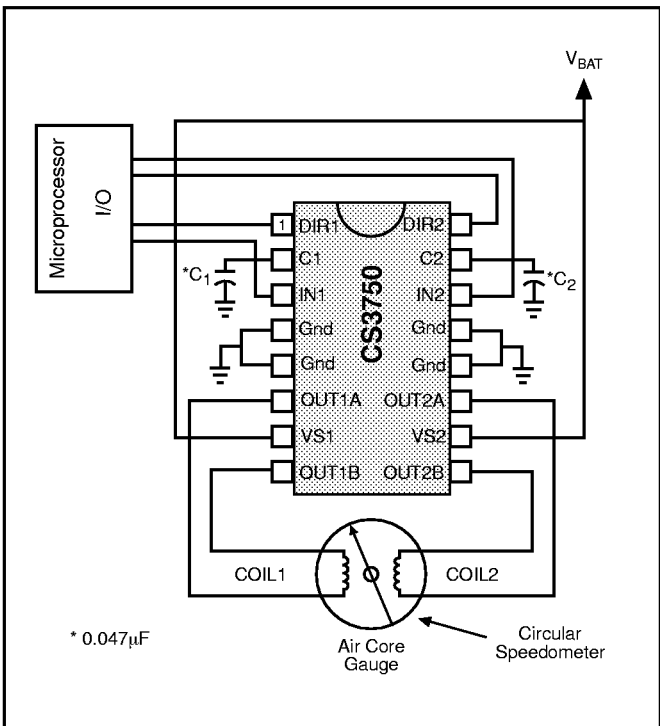
Table 1. Logic Control of H-Bridge

Input	Direction	Outputs	
INX	DIRX	OUTxA	OUTxB
0	X	0	0
1	0	1	0
1	1	0	1

Protection

The high side driver transistor in each H-bridge is current limited as a protection against a short circuit fault condition. If an over voltage or a thermal runaway fault conditions occurs, all outputs shut down.

Application Diagram



Package Specification

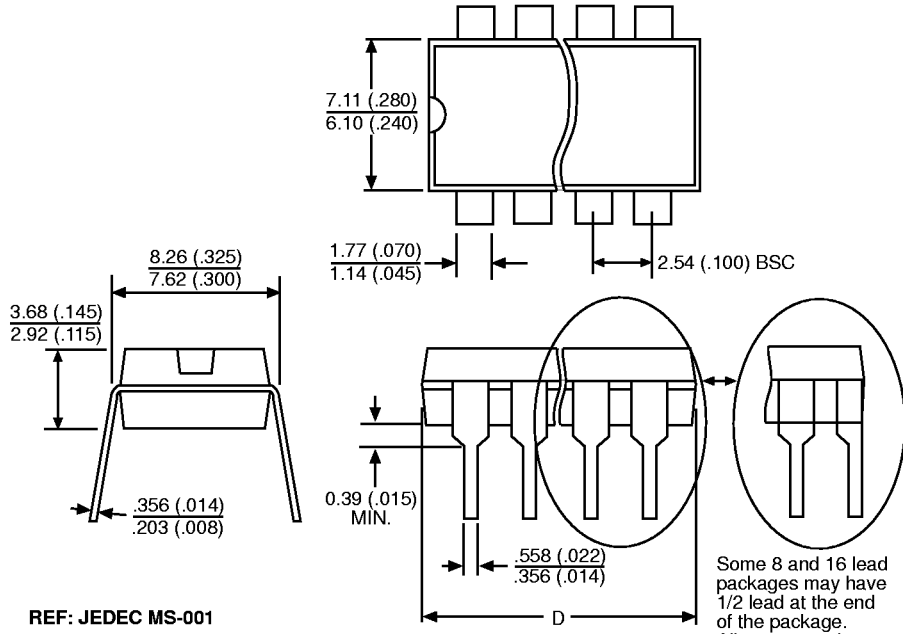
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16L PDIP (internally fused leads)	19.69	18.67	.775	.735

PACKAGE THERMAL DATA

Thermal Data		16L PDIP (internally fused leads)	
R _{θJC}	typ	15	°C/W
R _{θJA}	typ	50	°C/W

Plastic DIP (N), 300 mil wide



REF: JEDEC MS-001

Ordering Information

Part Number	Description
CS3750ENF16	16L PDIP (internally fused leads)

Cherry Semiconductor Corporation reserves the right to make changes to the specifications without notice. Please contact Cherry Semiconductor Corporation for the latest available information.