Area Detector Based Embedded Servo Demodulator

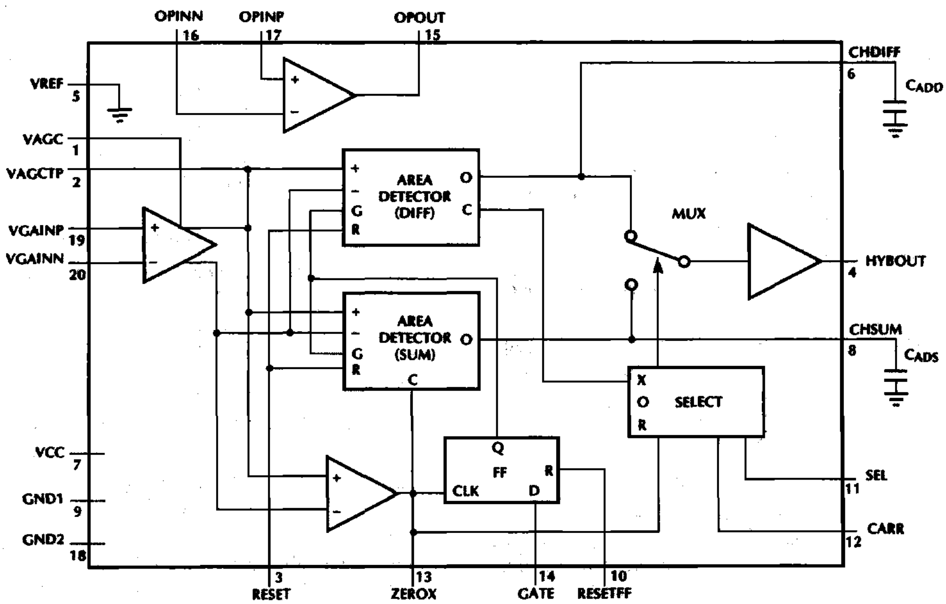
GENERAL DESCRIPTION

The ML4534 Embedded Servo Demodulator IC is designed for use in the hybrid data surface channel of an high-performance disk drive. Hybrid data are interleaved on the data surface with data records and encoded in A/B differential burst format, with a AGC field preceding the burst information. The AGC field is used by the read channel to set AGC gain levels in the burst area, which once established are held fixed for the duration of the servo burst. The demodulator measures burst amplitude using an area detection scheme, for improved noise immunity and provides both (A-B) and (A+B), to permit position error normalization with on-chip synchronization and reset functions. Using the SEL and CARR inputs the on-chip multiplexer allows selection of either (A-B) or (A+B) as the output. The multiplexer and area detection capacitors operate in concert to provide a hold capability for both the (A-B) and (A+B) outputs. Also included is an uncommitted operational amplifier which could be used for voice-coil motor current sensing.

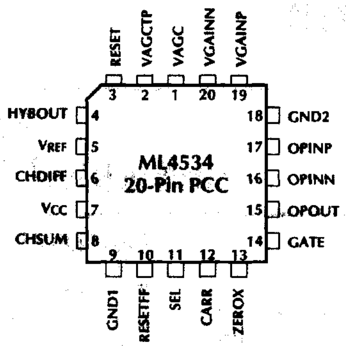
FEATURES

- Allows for Area Detection of back-to-back bursts
- 2% nonlinearity over input signal range
- Reset forces voltage on the Area Detecting capacitors C_{ADD} to V_{REF} & C_{ADS} to $V_{REF}/2$
- Separate Reset provided for Resync Flip-Flop
- Muxed/Selectable (A–B) & (A+B) demodulator output
- General purpose operational amplifier, applicable for use in voice coil motor current sensing
- 5V supply, 20-pin, J-leaded, PLCC package

BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	VAGC	Gain Control input on the VGA
2	VAGCTP	Test point connected through an isolation resistor to the output of the VGA
3	RESET	Asserting this input pin resets the area detector (DIFF) to V_{REF} (+2.5V) and the area detector (SUM) to $V_{REF}/2$
4	HYBOUT	Output of the multiplexing amplifier, with V_{REF}, (A–B) or (A+B) area detector output, depending on the state of the SEL & CARR pins.
5	V_{REF}	+2.5V reference voltage input.
8	CHSUM	The (A+B) area detector integrating capacitor is connected between this pin and the ground.
7	V_{CC}	+5 Volt supply
6	CHDIFF	The (A–B) area detector integrating capacitor is connected between this pin and the ground.
9	GND	Ground
10	RESETFF	Active high signal resets the resynch flip-flop
11	SEL	This pin in conjunction with the CARR pin, governs the multiplexer channel selection as follows : SEL CARR Mux Channel 0 X V_{REF} 1 0 (A–B) 1 1 (A+B)
12	CARR	Asserting this pin high inverts the carrier input of the (A–B) area detector. CARR should be asserted throughout the B burst of the A/B burst pair. While the CARR pin is asserted, the (A–B)

PIN NO.	NAME	FUNCTION
12	(Cont.)	area detector integrates the B burst in a direction opposite to that in which the A burst is integrated, thus realizing the (A–B) differencing operation. Carrier polarity in the (A+B) Area Detector is not affected by the state of the CARR pin. CARR pin in conjunction with the SEL pin, selects the multiplexer output.
13	ZEROX	This is the output of the Carrier Comparator. +ZEROX is a nominally square wave having transitions coinciding with zero crossings of the output VGA.
14	GATE	Asserting this line enables the (A+B) and (A–B) area detectors to measure area of the output signal of the VGA. This signal is re-synchronized to the area detector carrier internally before application to the area detectors.
15	OPOUT	Optional operational amplifier (short circuit protected) output.
16	OPINN	Optional operational amplifier inverting input.
17	OPINP	Optional operational amplifier non-inverting input.
18	GND	Ground
19	VGAINP	VGA non-inverting input. Inputs should be AC coupled
20	VGAINN	VGA inverting input. Inputs should be AC coupled

NOTE: The value of the CHSUM capacitor should be roughly twice that of the CHDIFF capacitor. It is also advisable to include a small resistor in series with the capacitor on the CHSUM pin and also the CHDIFF pin, to improve settling time.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (V_{CC}) .... –0.3 to + 7 VDC
Storage Temperature (T_{STG}) .... –65 to +150°C
Package Dissipation
T_A = 25°C (Board Mount) 875mW
Package Lead Temperature:
Soldering (10 sec) .... 260°C
Vapor Phase (60 sec) .... 215°C
Infrared (15 sec) .... 220°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage Range (V_{CC}) .... 5 ± 5% VDC
Temperature Range .... 0 to +70°C
Operating Junction Temperature (T_J) .... +25 to +125°C

ELECTRICAL CHARCTERISTICS

The following specifications apply over the recommended operating conditions of T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, and external component values as recommended, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	VAGC = 4.0V, V_{REF} = 2.5V	20	40	60	mA
I_{VREF}	V_{REF} = 2.5 V	–50	25	200	µA
GATE, CARR, SEL, RESET, RESETFF	For all signals in test program V_{IH}			2.0	V
	V_{IL}	0.8			V
GATE, CARR, SEL, RESET, RESETFF	For V_{IH} = 2.4V I_{IH}	–250		–10	µA
	and V_{IL} = 0.8V I_{IL}	–400		40	µA
VGAINPDC (VINP)	VGAINP, VGAINN open	2.3	2.5	2.7	V
VGAINNDC (VINN)	VGAINP, VGAINN open	2.3	2.5	2.7	V
V_{OH} ZEROX	VGAINP = 3.5, I_{OH} = –0.4mA VGAINN = 1.5V	2.7		5.0	V
V_{OL} ZEROX	VGAINN = 3.5, I_{OL} = 2.0mA VGAINP = 1.5V	0		0.5	V
OPERATIONAL AMPLIFIER USED FOR MOTOR CURRENT SENSING					
I_{BIAS} Offset	OPINN = OPINP = 1.0V	–200		200	nA
V_{OS} - MCS	A_V = 2.0, V_{IN} = 0	–15		+15	mV
V_{OH} - MCS	A_V = 2.0, V_{IN} =-1.0, I_{SRC} = –1.5mA	3.8		5.0	V
V_{OL} - MCS	A_V = 2.0, V_{IN} =1.0, I_{SINK}= 1.5mA	0		1.0	V
I_{SINK} - MCS	Openloop, OPINP = 0.0V OPINN = 1.0, OPOUT = V_{CC}	1.5		10	mV
I_{BIAS} - MCS	OPINN = 1.0, OPINP = 1.0 (IOPINN + IOPINP)/2	–2.0		0.0	µA
Amplifier Settling Time (t_{SMCS})	R_{OUT} = 604Ω, C_{OUT} = 36pF		0.4	1.0	µs
Amplifier Bandwidth		4	8		MHz
Amplifier Gain (A_V)	Open Loop	58	63		dB
AGC					
A_V - VGAMIN	Minimum Gain of AGC with 400mV input	0		1.1	V/V
A_V - VGAMAX	Maximum Gain of AGC with 100mV input	6.6		20	V/V
VAGCBIAS	VAGC = 1.0	0		200	µA

ELECTRICAL CHARCTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
RESET CIRCUITRY					
IRESET SUM, DIFF	RESET = V_{IH}	80		400	µA
IOFF SUM, DIFF	RESET = V_{IL}	–10		10	nA
VCH SUM RESET = V_{IH}	1.245	1.260	1.275	V	
VCH DIFF RESET = V_{IH}	2.490	2.5	2.510	V	
I SUM, DIFF UNBAL	GATE = V_{IH}, CLOCK, 1V swing VAGC 1X, Measure Current with VGAINP = VINP + 0.2 and VGAINN = VINN – 0.2, then do VGAINP = VINP – 0.2 and VGAINN = VINN + 0.2, Subtract	–40		40	µA
I DIFF UNBALXOR	CARR = V_{IH}	–40		+40	µA
I PEAK SUM	VGAINP = VINP + 1.0 VAGC = 1.0	–540	–400	–265	µA
I PEAK DIFF P	VGAINP = VINP + 1.0 VGAINN = VINN – 1.0 VAGC = 1.0, CARR = V_{IL}	–540	–400	–265	µA
I PEAK DIFF ON	VGAINP = VINP + 1.0 VGAINN = VINN – 1.0 VAGC = 1.0, CARR = V_{IH}	265	400	540	µA
VOH SUM	VGAINP = VINP + 1.0 VGAINN = VINN – 1.0	3.9		5.0	V
VOH DIFF	VGAINP = VINP + 1.0 VGAINN = VINN – 1.0 CARR = V_{IL}	3.9		5.0	V
VOL DIFF	VGAINP = VINP + 1.0 VGAINN = VINN - 1.0 CARR = V_{IH}	0.0		1.0	V
IGATE	GATE = V_{IH}, CLOCK, VAGC 1X, V_{SWING} = 1.0	–10		10	nA
IRESETFF	RESETFF = V_{IH}	–10		10	nA

ELECTRICAL CHARCTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
MUX AMPLIFIER					
VHYBOUT	CARR = V_{IL}, SEL = V_{IL}	2.4		2.6	V
VOS MUX SUM	CARR = SEL = V_{IH}, CHSUM = 2.5	–8		8	mV
VOS MUX DIFF	CARR = V_{IL}, SEL = V_{IH}, CHDIFF = 2.5	–8		8	mV
IBIASSUM	CARR = SEL = V_{IH}, CHSUM = 2.5	0		300	nA
IBIASDIFF	CARR = VIL, SEL = V_{IH}, CHSUM = 2.5	0		300	nA
VOHMUX	CARR = SEL = V_{IH} CHSUM = 3.95, I_{SRC} = 1.5mA	3.8		5.0	V
VOLMUX	CARR = V_{IL}, SEL = V_{IH} CHDIFF = 0.95, I_{SINK} = 1.5mA	0		1.0	V
ISINKMUX	CARR = V_{IL}, CHDIFF = 0.95 SEL = V_{IH}, VHYBOUT = V_{CC}	1.5		10	mA
Amplifier settling time (t_{SMUX})	R_{OUT} = 604Ω, C_{OUT} = 36pF		0.4	1	µs
$I_{LEAKAGE}$			10	nA	
Linearity	0 to 1 V_{INPUT}, with VAGC such that A_V VAGC = 1.0	–5		5	%F.S

FUNCTIONAL DESCRIPTION

The ML4534, +5V Embedded Servo Demodulator IC is designed for use in the hybrid data surface channel of an high-performance disk drive. Hybrid data are interleaved on the data surface with data records and encoded in A/B differential burst format, with an AGC field preceding the burst information. The AGC field is used by the read channel to set AGC gain levels in the burst area, which once established are held fixed for the duration of the servo burst. The demodulator measures burst amplitude using an area detection scheme, for improved noise immunity and provides both (A–B) and (A+B), to permit position error normalization. Using the SEL and CARR inputs, the on-chip multiplexer allows selection of either (A–B) or (A+B) on the output. The multiplexer and area detection capacitors operate in concert to provide a hold capability for both the (A–B) and (A+B) outputs. The area detectors are designed to minimize the pipeline transport delay while accurately quantizing the area of servo bursts in high speed hybrid servo systems. The major functional blocks of the ML4534 are briefly discussed below.

VARIABLE GAIN AMPLIFIER

Hybrid servo burst data from the disk read channel are capacitively coupled into the VGA through the differential input pins (VGAINP, VGAINN). VGA gain is controlled by the voltage on the VAGC pin, and the gain is varied in order to secure constant area of the output signal and counteract the amplitude regulating operation of the read channel AGC loop.

VGABUF COMPARATOR

The VGABUF comparator detects zero crossings of the composite signal delivered by the VGA. The output of this comparator controls the synchronous rectification of the composite VGA output, in the area detectors.

The comparator output is provided at a TTL level on the ZEROX pin. Control logic in the servo channel employs the ZEROX signal to produce an area detector enabling gate, which spans a fixed number of cycles of the composite signal.

AREA DETECTORS (SUM AND DIFF)

The area detectors detect A and B burst levels by area detection. Two area detectors are provided — one to measure the sum of A and B bursts (A+B), and a second one to measure the difference (A–B). Each area detector is implemented as a gated current — output synchronous rectifier driving an external charge accumulating integrating capacitor. Area detection occurs only while the area detector is enabled under control of the GATE pin. When the detector is disabled, the integrating capacitor is effectively floated. An on-chip binary (FF) re-synchronizes the gating signal to remove any phase shifts due to logic delays in the external gate control logic. Initial conditions on the integrating capacitors are established prior to an area detecting operation by a reset circuit controlled by the RESET pin. A reset operation forces the voltage on the area detecting capacitors to equal the 2.5 volts applied on the V_{REF} pin. Determination of the burst difference (A–B) is accomplished under control of the CARR pin, by inverting the phase of the carrier input to the second area detector, while the burst B is being detected. The inversion is performed by an XOR gate. Accordingly (A–B) is bipolar relative to V_{REF}, while (A+B) is unipolar.

MULTIPLEXER AMPLIFIER

The multiplexer amplifier drives the HYBOUT pin and allows sequential interrogation of the (A–B) and (A+B) measurements, the results of which are stored on the external integrating capacitors. The amplifier is implemented as two independently selectable input stages, driving a common output structure, to form a voltage follower. To minimize the droop of the (A–B) and the (A+B) measurements, both input stages are biased off during periods when neither measurement is required to be routed to the HYBOUT pin. The SEL and CARR pins govern multiplexer channel selection through a decoding network.

Figure 1 shows a typical hybrid servo system application diagram for the ML4534 and also illustrates waveforms characteristic of a hybrid demodulator in a typical application.

OPERATIONAL AMPLIFIER USED FOR MOTOR CURRENT SENSE

This general purpose operational amplifier is intended for use as a differential to single-ended convertor and level shift stage. It performs voice coil motor current sensing by monitoring the voltage developed differentially across current sense resistors, on the ground side of the voice coil power driver bridge.

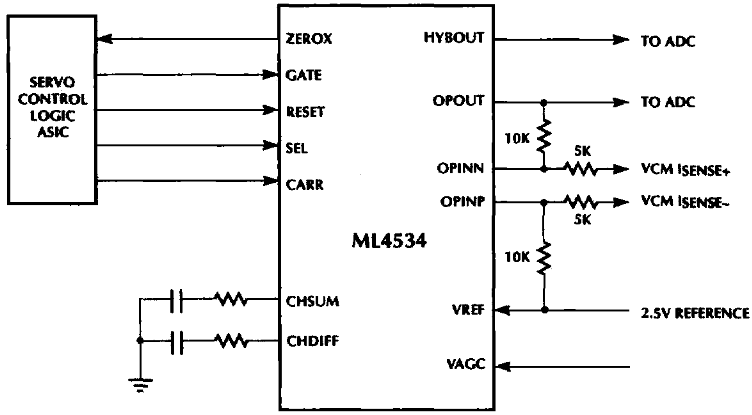


Figure 1. A Typical Servo System Application with the ML4534.

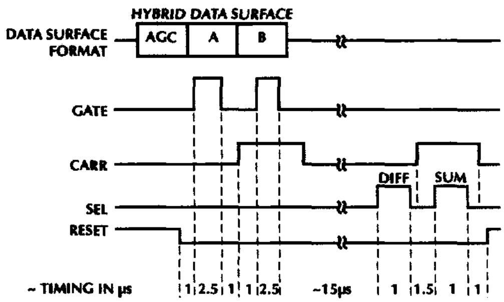


Figure 2. Illustrative Waveforms

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4534CQ	0°C to +70°C	20-Pin Molded PLCC (Q20)