Signetics

74S350
Shifter

4-Bit Shifter With 3-State Outputs
Product Specification

Logic Products

FEATURES

- **Shifts 4 bits of data to 0, 1, 2, 3 places under control of two select lines**
- **3-State outputs for bus organized systems**
- **Alternate source AM25S10**

DESCRIPTION

The '350 is a combination logic circuit that shifts a 4-bit word from 0 to 3 places. No clocking is required as with shift registers.

The '350 can be used to shift any number of bits any number of places up or down by suitable interconnection. Shifting can be:

1. Logical – with logic zeros filled in at either end of the shifting field.
2. Arithmetic – where the sign bit is extended during a shift down.
3. End around – where the data word forms a continuous loop.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74S350	7ns	71mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74S350N

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

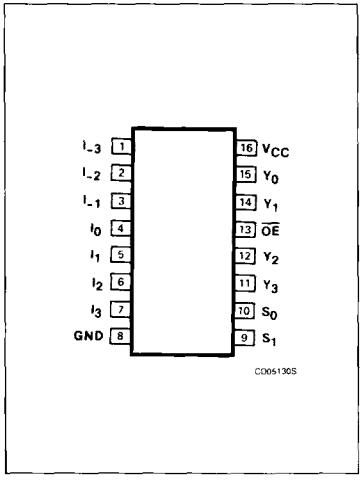
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S
All	Inputs	1Sul
All	Outputs	10Sul

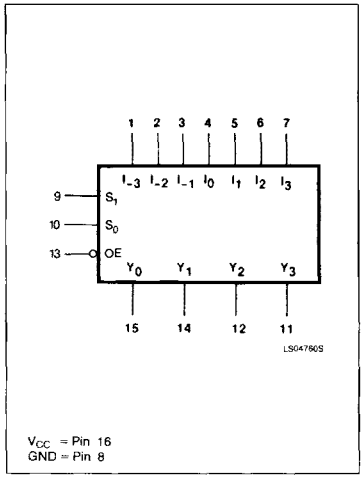
NOTE:
A 74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

The 3-State outputs are useful for bus interface applications or expansion to a larger number of shift positions in end around shifting. The active LOW Output Enable ($\overline{OE}$) input controls the state of the outputs. The outputs are in the HIGH impedance "off" state when $\overline{OE}$ is HIGH, and they are active when $\overline{OE}$ is LOW.

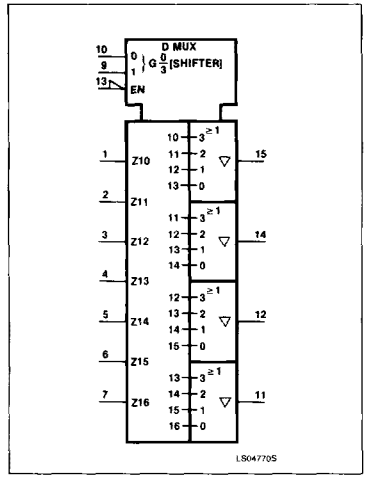
PIN CONFIGURATION



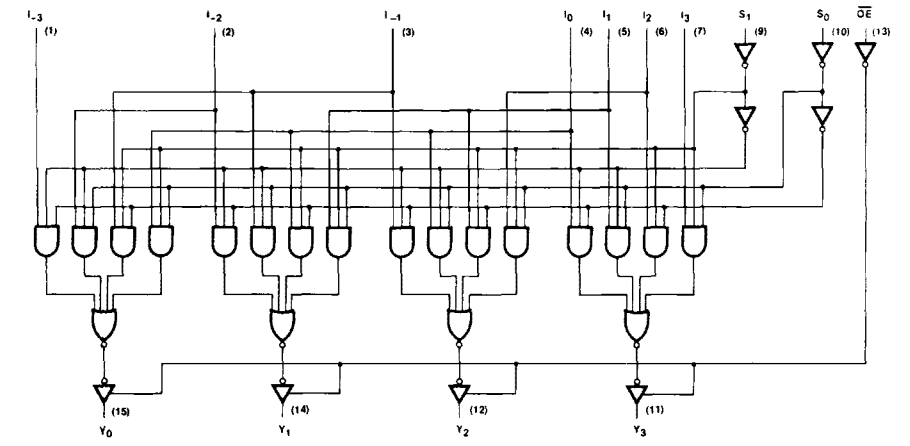
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin Numbers

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FUNCTION TABLE

OE	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	S_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state
D_n = HIGH or LOW state of referenced I_n input

LOGIC EQUATIONS

$$Y_0 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_0 + S_0 \cdot \overline{S}_1 \cdot I_{-1} + \overline{S}_0 \cdot S_1 \cdot I_{-2} + S_0 \cdot S_1 \cdot I_{-3}$$

$$Y_1 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_1 + S_0 \cdot \overline{S}_1 \cdot I_0 + \overline{S}_0 \cdot S_1 \cdot I_{-1} + S_0 \cdot S_1 \cdot I_{-2}$$

$$Y_2 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_2 + S_0 \cdot \overline{S}_1 \cdot I_1 + \overline{S}_0 \cdot S_1 \cdot I_0 + S_0 \cdot S_1 \cdot I_{-1}$$

$$Y_3 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_3 + S_0 \cdot \overline{S}_1 \cdot I_2 + \overline{S}_0 \cdot S_1 \cdot I_1 + S_0 \cdot S_1 \cdot I_0$$

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	74S	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74S			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IH}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−6.5	mA
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

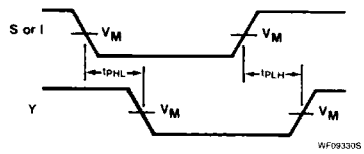
PARAMETER		TEST CONDITIONS[1]	74S350			UNIT
			Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	2.4			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.4V			50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_O = 0.5V			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V			1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V			−2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	−40		−100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, V_{IN} = 0V		71	85	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

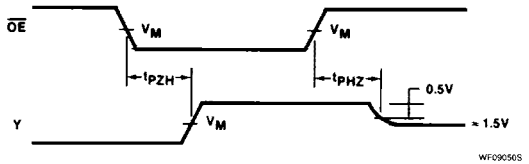
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74S		UNIT
			C_L = 15pF, R_L = 280Ω		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		17 20	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		19.5	ns
t_{PZL}	Enable time to LOW level	Waveform 3		21	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, C_L = 5pF		8.0	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, C_L = 5pF		15	ns

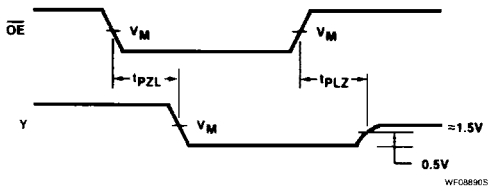
AC WAVEFORMS



Waveform 1. Propagation Delay Data (I) Or Select (S) To Output



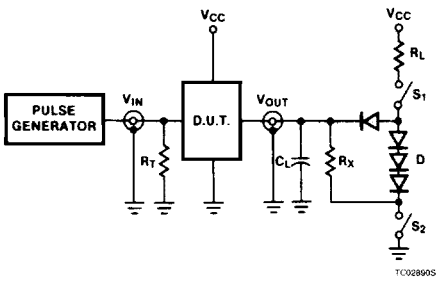
Waveform 2. 3-State Enable Time To High Level And Disable Time From High Level



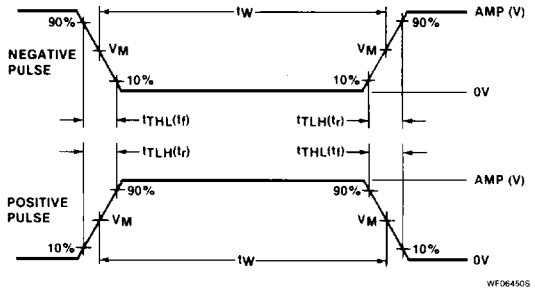
For all waveforms, V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS/74LS

Waveform 3. 3-State Enable Time To Low Level And Disable Time From Low Level

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

R_X = 1kΩ for 74, 74S, R_X = 5kΩ for 74LS.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

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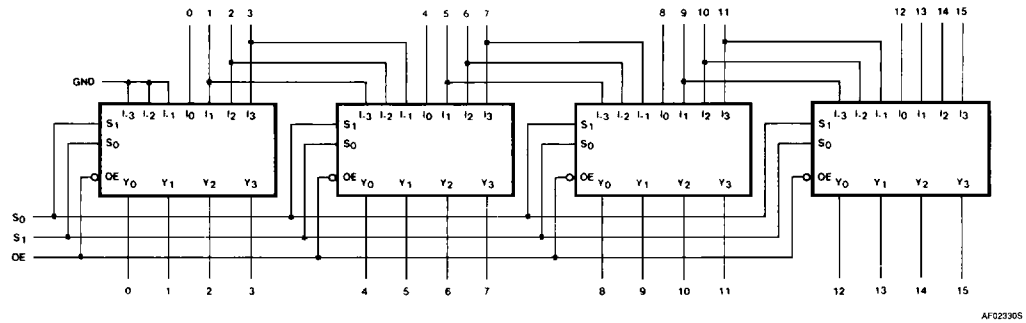
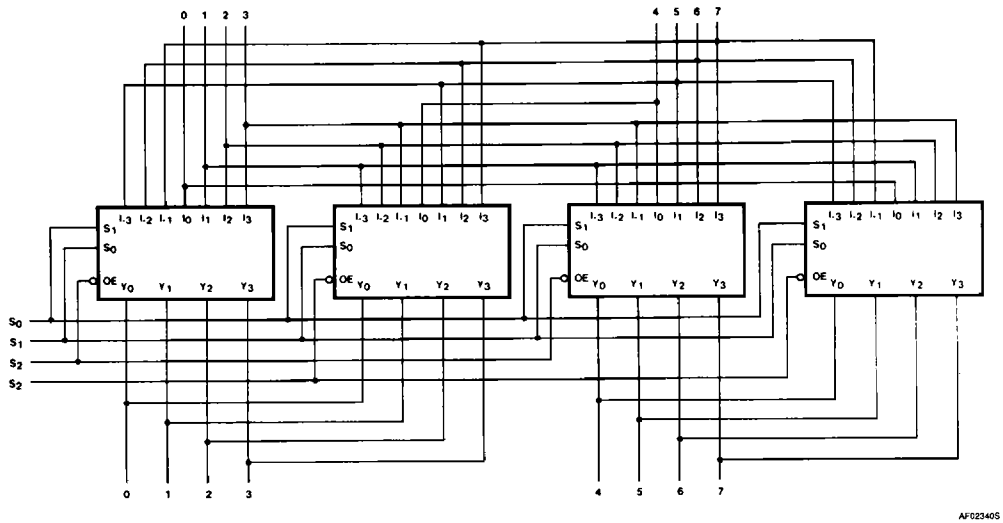
APPLICATIONS DIAGRAMS



S_1	S_0	
L	L	NO SHIFT
L	H	SHIFT 1 PLACE
H	L	SHIFT 2 PLACES
H	H	SHIFT 3 PLACES

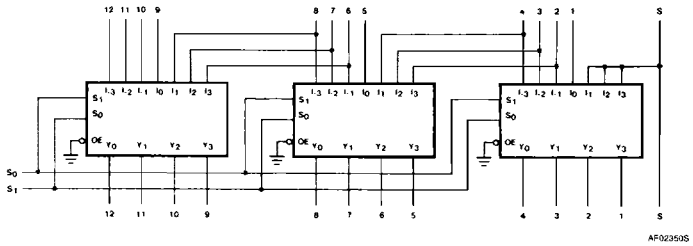
16-Bit Shift-Up 0, 1, 2, Or 3 Places



S_2	S_1	S_0	
L	L	L	NO SHIFT
L	L	H	SHIFT END AROUND 1
L	H	L	SHIFT END AROUND 2
L	H	H	SHIFT END AROUND 3
H	L	L	SHIFT END AROUND 4
H	L	H	SHIFT END AROUND 5
H	H	L	SHIFT END AROUND 6
H	H	H	SHIFT END AROUND 7

8-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6, 7 Places

APPLICATIONS DIAGRAMS (Continued)



S_1	S_0		SCALE
L	L	+8	1/8
L	H	+4	1/4
H	L	+2	1/2
H	H	NO CHANGE	1

13-Bit 2's Complement Scaler

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