

HIGH PERFORMANCE V53C405	60/60L	70/70L	80/80L	10/10L
Max. RAS Access Time, (t_{RAC})	60 ns	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	30 ns	35 ns	40 ns	50 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	55 ns	65 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	130 ns	150 ns	180 ns

LOW POWER V53C405L	60L	70L	80L	10L
Max. CMOS Standby Current, (I_{DD6})	0.4 mA	0.4 mA	0.4 mA	0.4 mA

Features

- 1M x 4-bit 4 CAS organization
- RAS access time: 60,70,80,100 ns
- Low power dissipation
 - V53C405-10
 - Operating Current – 65 mA max.
 - TTL Standby Current – 2.0 mA max.
- Low CMOS Standby Current
 - V53C405 – 1.0 mA max.
- Read-Modify-Write, RAS-Only Refresh, CAS-Before-RAS Refresh capability
- Refresh Interval
 - V53C405 – 1024 cycles/16ms
 - V53C405L – 1024 cycles/64ms
- Fast Page Mode for a sustained data rate greater than 20 MHz
- Available in 26/24 pin SOJ package (300 mil)

Description

The V53C405 is a high speed 1,048,576x4 bit CMOS dynamic random access memory. The V53C405 offers 4 CAS inputs, in addition to: Fast Page Mode for high data bandwidth, low CMOS standby current and, on request, extended refresh for very low data retention power (V53C405L).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 1024 (x4) bits within a row with cycle times as short as 45 ns. These features make the V53C405 ideally suited for parity bits for the SIMM module and parity memory for the main memories, graphics, digital signal processing and high performance computing systems.

The V53C405L offers a maximum data retention power of 5.5 mW when operating in CMOS standby mode and performing RAS-only or CAS-before-RAS refresh cycles.

Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)				Power		Temperature Mark
	K	60	70	80	100	Low	Std.	
0°C to 70 °C	•	•	•	•	•	•	•	Blank

V53C405 Rev. 00 March 1993