PSoC™ 4200L Automotive

Based on Arm® Cortex®-M0

General description

PSoC™ 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an Arm® Cortex®-M0 CPU. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC™ 4200L product family, based on this platform, is a combination of a microcontroller with digital programmable logic, programmable analog, programmable interconnect, secure expansion of memory off-chip, high-performance analog-to-digital conversion, opamps with Comparator mode, and standard communication and timing peripherals. The PSoC™ 4200L products will be fully compatible with members of the PSoC™ 4 platform for new applications and design needs. The programmable analog and digital subsystems allow flexibility and in-field tuning of the design.

Features

- 32-bit MCU subsystem
  - 48 MHz Arm® Cortex®-M0 CPU with single-cycle multiply
  - Up to 256 kB of flash with read accelerator
  - Up to 32 kB of SRAM
  - DMA engine with 32 channels
- Programmable analog
  - Four opamps that operate in Deep Sleep mode at very low current levels
  - All opamps have reconfigurable high current pin-drive, high-bandwidth internal drive, ADC input buffering, and Comparator modes with flexible connectivity allowing input connections to any pin
  - Four current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
  - Two low-power comparators that operate in Deep Sleep mode
- Programmable digital
  - Eight programmable logic blocks, each with eight Macrocells and an 8-bit data path (called universal digital blocks or UDBs)
  - Infineon-provided peripheral component library, user-defined state machines, and Verilog input
- Low-power 1.71 V to 5.5 V operation
  - 20-nA Stop mode with GPIO pin wakeup
  - Hibernate and Deep Sleep modes allow wakeup-time versus power trade-offs
- Capacitive sensing
  - Two capacitive sigma-delta blocks provide best-in-class SNR (> 5:1) and water tolerance
  - Infineon-supplied software component makes capacitive sensing design easy
  - Automatic hardware tuning (SmartSense)
- Segment LCD drive
  - LCD drive supported on any pin with up to a maximum of 64 outputs (common or segment)
  - Operates in Deep Sleep mode with 4 bits per pin memory
- Serial communication
  - Four independent run-time reconfigurable Serial Communication Blocks (SCBs) with reconfigurable I^2C, SPI, or UART functionality
  - USB Full-Speed device interface 12 Mbits/sec with Battery Charger Detect capability
  - Two independent CAN blocks for industrial and automotive networking
- Timing and pulse-width modulation
  - Eight 16-bit timer/counter pulse-width modulator (TCPWM) blocks
  - Center-aligned, Edge, and Pseudo-random modes
  - Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications

Features

- Up to 98 programmable GPIOs
  - 124-ball VFBGA package
  - Any of up to 94 GPIO pins can be CAPSENSE™, analog, or digital
  - Drive modes, strengths, and slew rates are programmable
- PSoC™ Creator design environment
  - Integrated development environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
  - Applications programming interface (API) component for all fixed-function and programmable peripherals
- Industry-standard tool compatibility
  - After schematic entry, development can be done with Arm®-based industry-standard development tools

Table of contents

1 Development ecosystem

1.1 PSoC™ 4 MCU resources

Infineon provides a wealth of data at **www.infineon.com** to help you to select the right PSoC™ device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article **KBA86521, How to Design with PSoC™ 3, PSoC™ 4, and PSoC™ 5LP**. Following is an abbreviated list for PSoC™ 4:

- Overview: **PSoC™ Portfolio, PSoC™ Roadmap**
- Product Selectors: **PSoC™ 1, PSoC™ 3, PSoC™ 4, PSoC™ 5LP**
  In addition, PSoC™ Creator includes a device selection tool.
- Application notes: Infineon offers a large number of PSoC™ application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC™ 4 are:
  - **AN79953**: Getting started with PSoC™ 4
  - **AN88619:** PSoC™ 4 hardware design considerations
  - **AN86439:** Using PSoC™ 4 GPIO pins
  - **AN57821:** Mixed signal circuit board layout
  - **AN81623:** Digital design best practices
  - **AN73854:** Introduction to bootloaders
  - **AN89610:** Arm® Cortex® code optimization
  - **AN85951:** PSoC™ 4 and PSoC™ 6 MCU CAPSENSE™ design guide
- **Code examples** demonstrate product features and usage, and are also available on **Infineon GitHub repositories**.Technical reference manual (TRM) is in two documents:
  - **Architecture TRM** details each PSoC™ 4 functional block.
  - **Registers TRM** describes each of the PSoC™ 4 registers.
- Development tools:
  - **PSoC™ Creator** is a free Windows-based IDE. It enables concurrent hardware and firmware design of PSoC™ 3, PSoC™ 4, PSoC™ 5LP, and PSoC™ 6 MCU based systems. Applications are created using schematic capture and over 150 pre-verified, production-ready peripheral components.
  - **CY8CKIT-042**, PSoC™ 4 pioneer kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
  - **CY8CKIT-046**, PSoC™ 4 L-Series pioneer kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields.
  - **CY8CKIT-049** is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC™ 4 devices.
  - **CY8CKIT-001** is a common development platform for any one of the PSoC™ 1, PSoC™ 3, PSoC™ 4, or PSoC™ 5LP families of devices.
  - **MiniProg4** and **MiniProg3** all-in-one development programmers and debuggers.
  - **PSoC™ 4 MCU CAD libraries** provide footprint and schematic support for common tools. **IBIS models** are also available.

Infineon developer community enables connection with fellow PSoC™ developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated **PSoC™ 4 MCU community**.

1.2 PSoC™ Creator

PSoC™ Creator is a free Windows-based IDE. It enables you to design hardware and firmware systems concurrently, based on PSoC™ 4 MCU. As **Figure 1** shows, with PSoC™ Creator you can:

1. Explore the library of 200+ Components
2. Drag and drop Component icons to complete your hardware system design in the main design workspace
3. Configure Components using the Component configuration tools and the Component datasheets
4. Co-design your application firmware and hardware in the PSoC™ Creator IDE or build a project for a third-party IDE
5. Prototype your solution with the PSoC™ 4 pioneer kits. If a design change is needed, PSoC™ Creator and Components enable you to make changes on-the-fly without the need for hardware revisions.

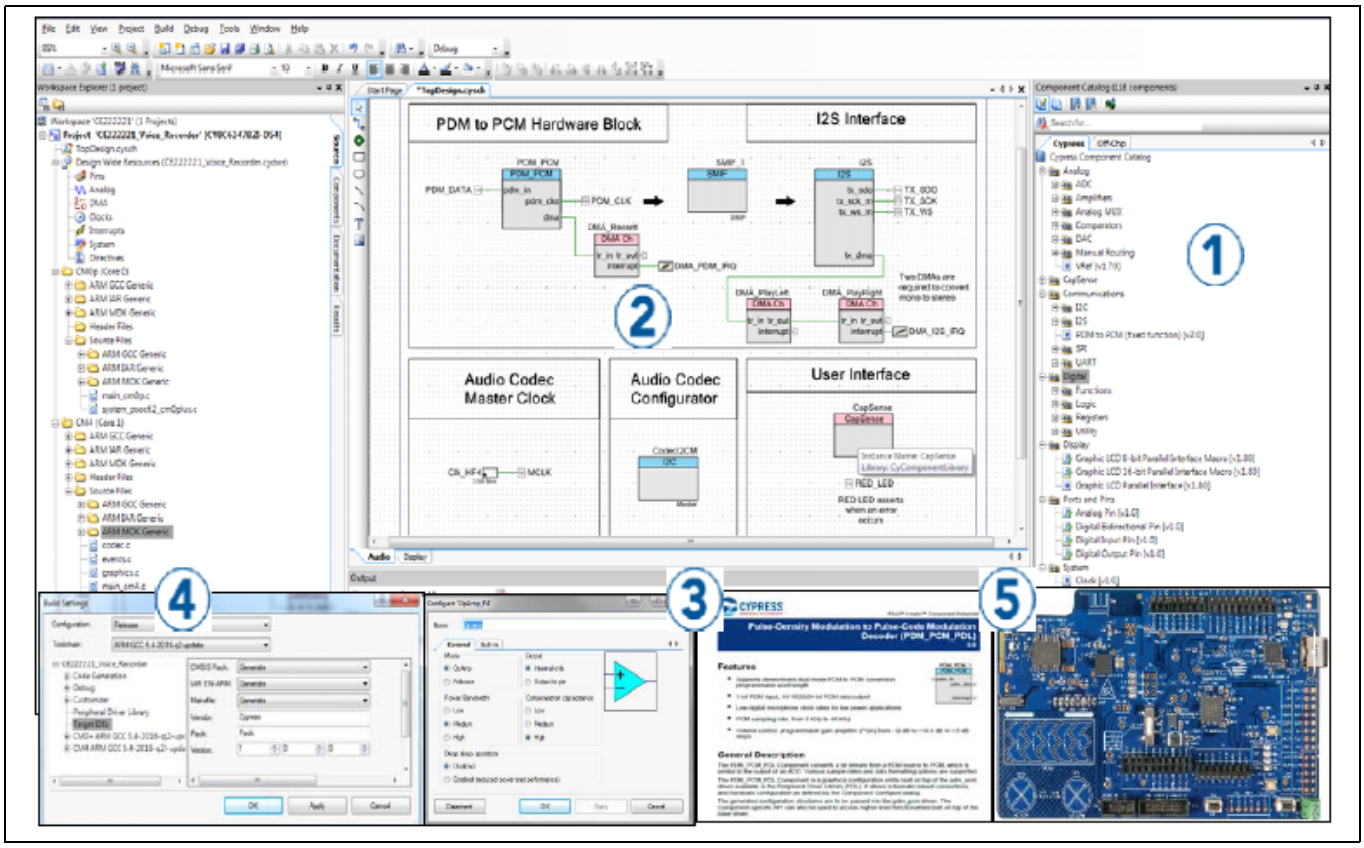


Figure 1 PSoC™ Creator schematic entry and components

2 PSoC™ 4200L block diagram

The PSoC™ 4200L devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm® serial wire debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC™ Creator IDE provides fully integrated programming and debug support for PSoC™ 4200L devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC™ 4200L family provides a level of security not possible with multi-chip application solutions or with microcontrollers. This is due to its ability to disable debug features, robust flash protection, and because it allows customer-proprietary functionality to be implemented in on-chip programmable blocks.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC™ 4200L with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC™ 4200L allows the customer to make.

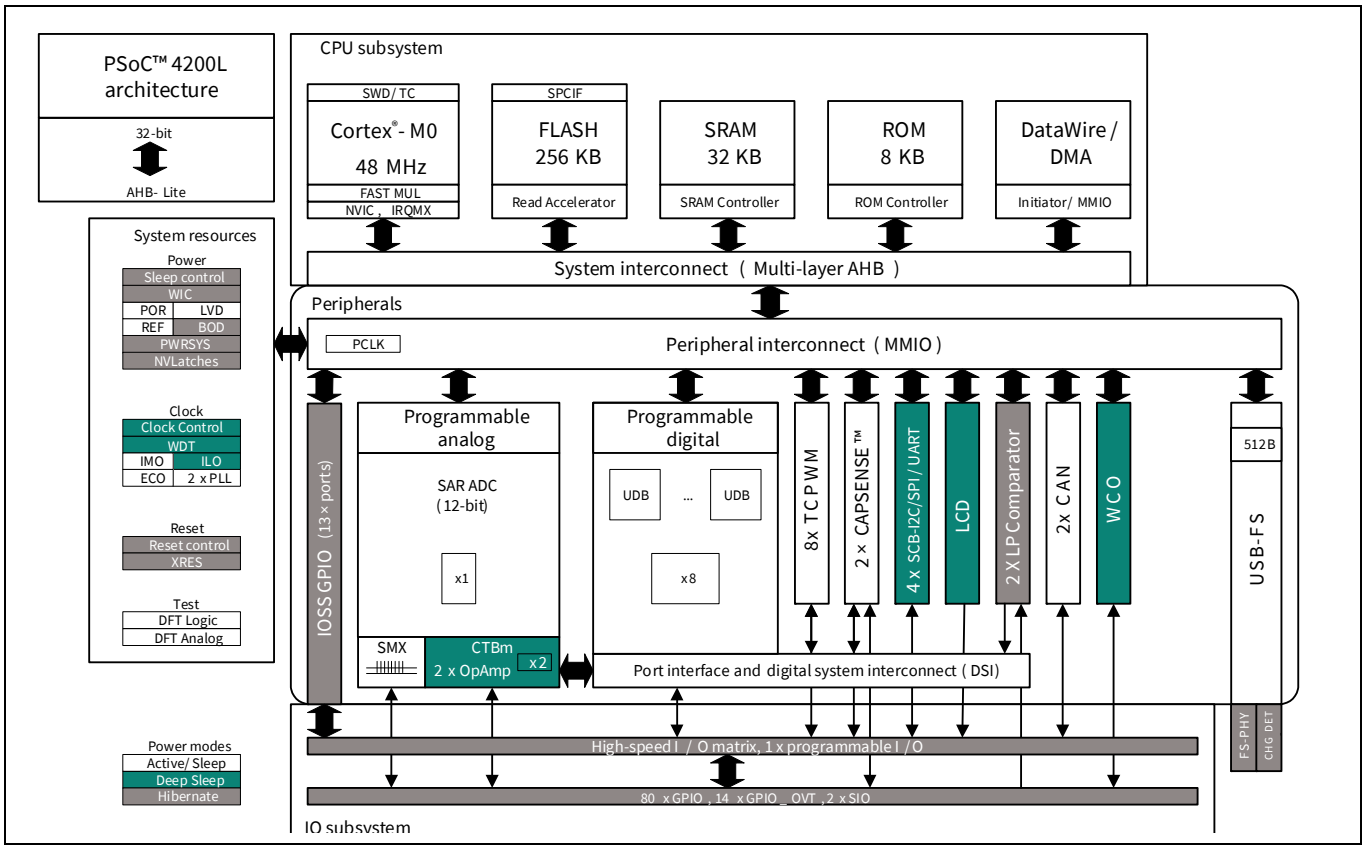


Figure 2 Block diagram

3 Functional definition

3.1 CPU and memory subsystem

3.1.1 CPU

The Cortex®-M0 CPU in the PSoC™ 4200L is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and execute a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex®-M3 and M4, thus enabling upward compatibility. The Infineon implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from the Deep Sleep mode allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex®-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC™ 4200L has four break-point (address) comparators and two watchpoint (data) comparators.

3.1.2 Flash

The PSoC™ 4200L has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 2 wait-state (WS) access time at 48 MHz and with 1-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

3.1.3 SRAM

SRAM memory is retained during Hibernate.

3.1.4 SROM

A supervisory ROM that contains boot and configuration routines is provided.

3.1.5 DMA

A DMA engine is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

3.2 System resources

3.2.1 Power system

The power system is described in detail in the section **“Power”** on page 22. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detection (BOD)) or interrupts (low voltage detect (LVD)). The PSoC™ 4200L operates with a single external supply over the range of 1.71V to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC™ 4200L provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

3.2.2 Clock system

The PSoC™ 4200L clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no meta-stable conditions occur.

The clock system for the PSoC™ 4200L consists of a crystal oscillator (4 to 33 MHz), a watch crystal oscillator (32 kHz), a phase-locked loop (PLL), the IMO and the ILO internal oscillators, and provision for an external clock.

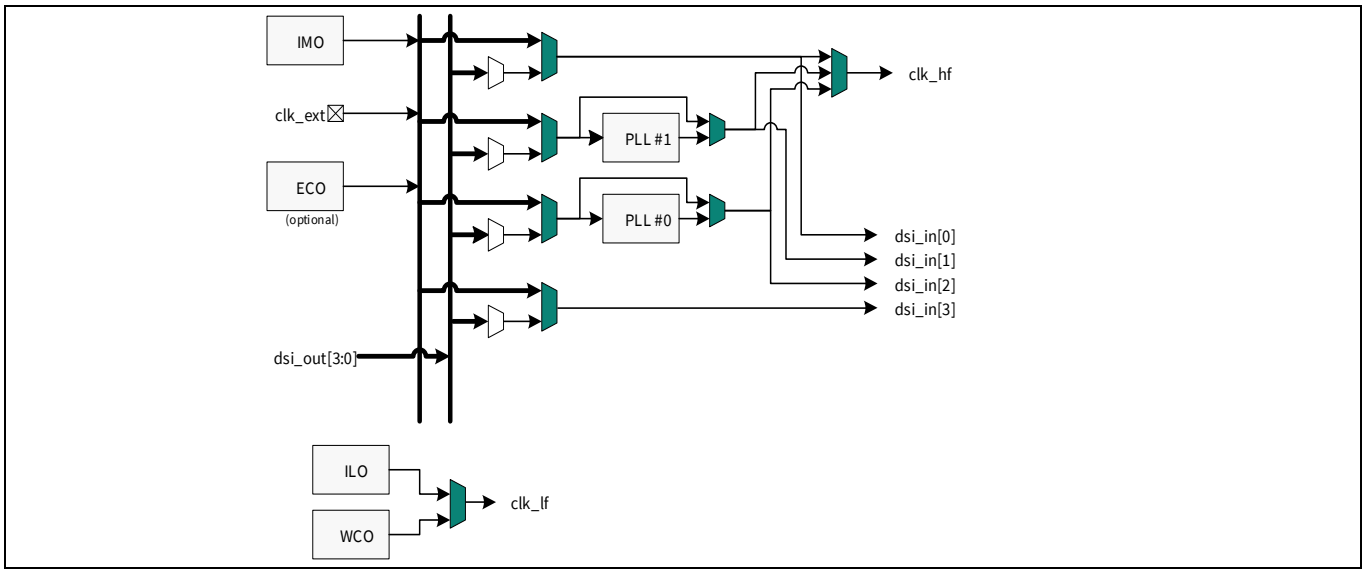


Figure 3 PSoC™ 4200L MCU clocking architecture

The clk_hf signal can be divided down to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 16 clock dividers for the PSoC™ 4200L, each with 16-bit divide capability; this allows 12 to be used for the fixed-function blocks and four for the UDBs. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC™ Creator.

3.2.3 IMO clock source

The IMO is the primary source of internal clocking in the PSoC™ 4200L. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. IMO tolerance with Infineon-provided calibration settings is ±2%.

3.2.4 ILO clock source

The ILO is a very low-power oscillator, nominally 32 kHz, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Infineon provides a software component, which does the calibration.

3.2.5 Crystal oscillators and PLL

The PSoC™ 4200L clock subsystem also implements two oscillators: high-frequency (4 to 33 MHz) and low-frequency (32-kHz watch crystal) that can be used for precision timing applications. The PLL can generate a 48-MHz output from the high-frequency oscillator.

3.2.6 Watchdog timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

3.2.7 Reset

The PSoC™ 4200L can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

3.2.8 Voltage reference

The PSoC™ 4200L reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to add an external bypass capacitor to the internal reference using a GPIO pin or to use an external reference for the SAR.

3.3 Analog blocks

3.3.1 12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice (for the PSoC™ 4200L case) of three internal voltage references: V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.024 V) as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. The system performance will be 65 dB for true 12-bit precision if appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an eight input sequencer (expandable to sixteen inputs). The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps, whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. In addition, the signal range specification through a pair of range registers (LOW and HIGH range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

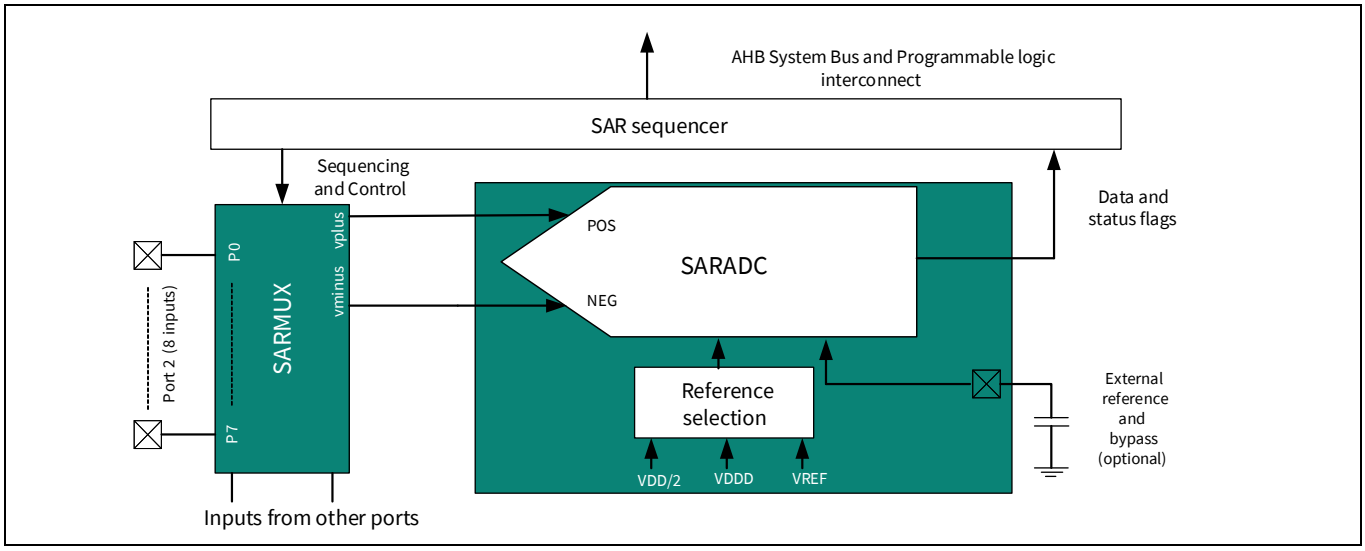


Figure 4 SAR ADC system diagram

3.3.2 Analog multiplex bus

The PSoC™ 4200L has two concentric analog buses (Analog MUX bus A and Analog MUX bus B) that circumnavigate the periphery of the chip. These buses can transport analog signals from any pin to various analog blocks (including the opamps) and to the CAPSENSE™ blocks allowing, for instance, the ADC to monitor any pin on the chip. These buses are independent and can also be split into three independent sections. This allows one section to be used for CAPSENSE™ purposes, one for general analog signal processing, and the third for general-purpose digital peripherals and GPIO.

3.3.3 Four opamps (CTBm Blocks)

The PSoC™ 4200L has four opamps with Comparator modes, which allow most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering. The opamps can operate in the Deep Sleep mode at very low-power levels. The following diagram shows one of two identical opamp pairs of the opamp subsystem.

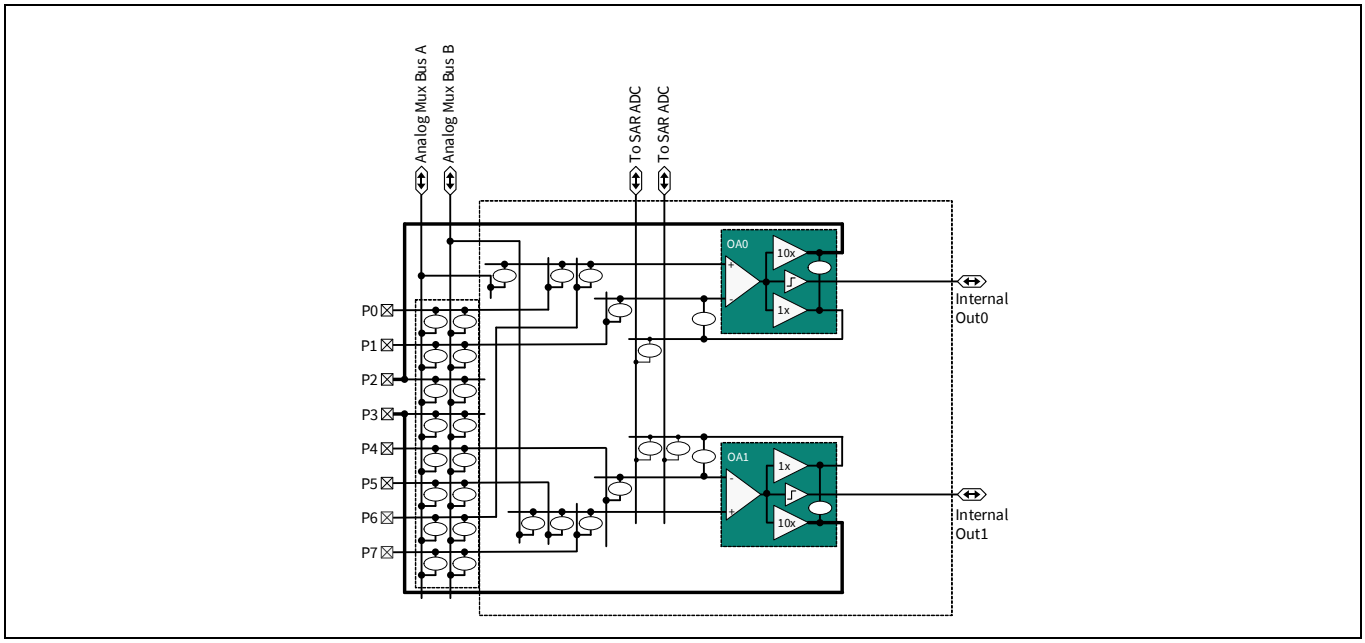


Figure 5 Identical opamp pairs in opamp subsystem

The ovals in **Figure 5** represent analog switches, which may be controlled via user firmware, the SAR sequencer, or user-defined programmable logic. The opamps (OA0 and OA1) are configurable via these switches to perform all standard opamp functions with appropriate feedback components.

The opamps (OA0 and OA1) are programmable and reconfigurable to provide standard opamp functionality via switchable feedback components, unity gain functionality for driving pins directly, or for internal use (such as buffering SAR ADC inputs as indicated in the diagram), or as true comparators.

The opamp inputs provide highly flexible connectivity and can connect directly to dedicated pins or, via the analog mux buses, to any pin on the chip. Analog switch connectivity is controllable by user firmware as well as user-defined programmable digital state machines (implemented via UDBs).

The opamps operate in Deep Sleep mode at very low currents allowing analog circuits to remain operational during Deep Sleep.

3.3.4 Temperature sensor

The PSoC™ 4200L has one on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Infineon-supplied software that includes calibration and linearization.

3.3.5 Low-power comparators

The PSoC™ 4200L has a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid meta-stability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

3.4 Programmable digital

3.4.1 Universal digital blocks (UDBs) and port interfaces

The PSoC™ 4200L has eight UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control. **Figure 6**shows the UDB array.

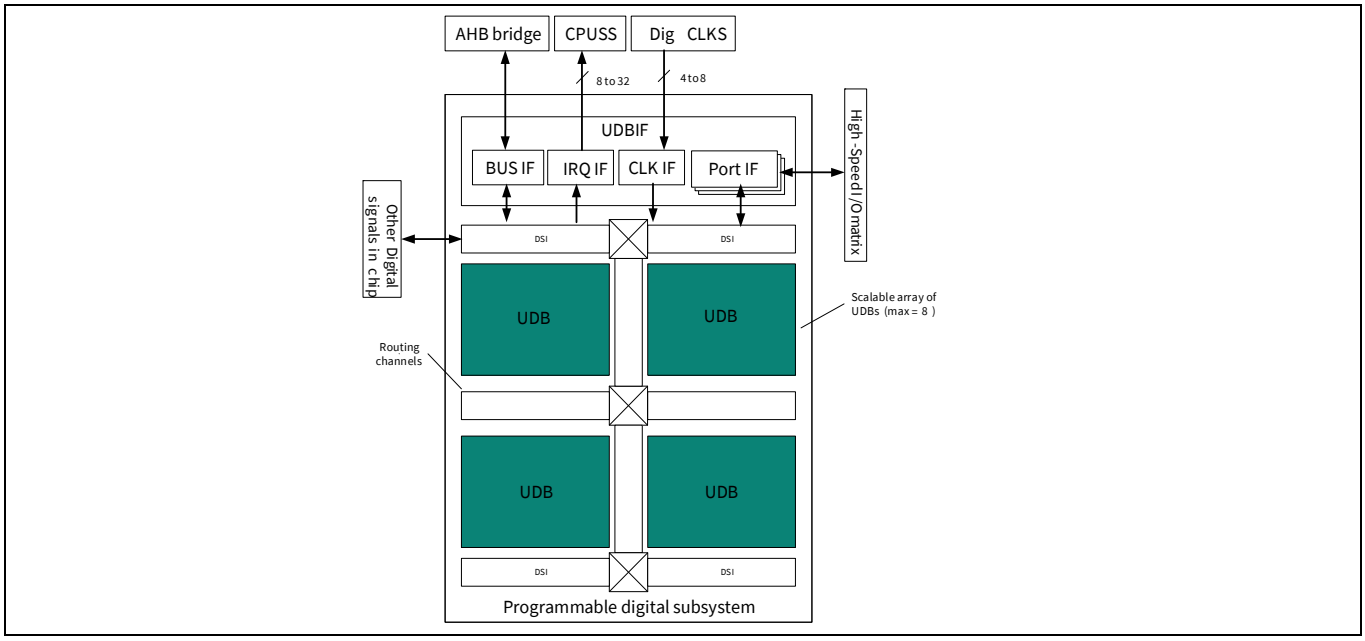


Figure 6 UDB array

UDBs can be clocked from a clock divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs. The port interface is shown in **Figure 7**.

The UDBs can generate interrupts (one UDB at a time) to the interrupt controller. The UDBs retain the ability to connect to most of the pins on the chip through the DSI, with the exception of the pins from Port 7, 8, and 9.

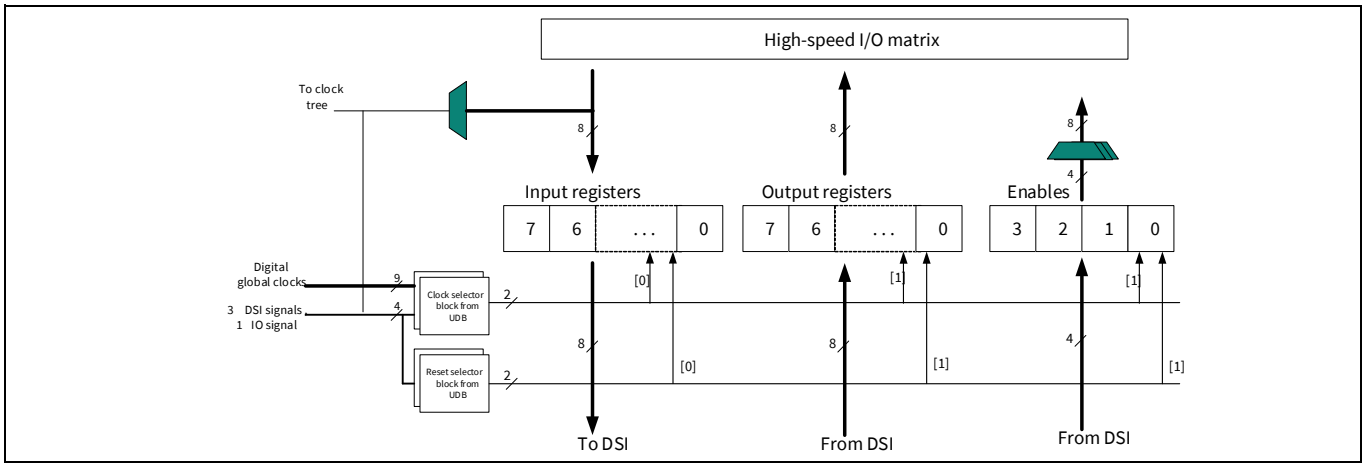


Figure 7 Port interface

3.5 Fixed function digital

3.5.1 Timer/Counter/PWM (TCPWM) block

The TCPWM block consists of one 16-bit counter with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a Period register which is used to either Stop or Auto-reload the counter when its count is equal to the Period register, and compare registers to generate compare value signals, which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut-off immediately with no time for software intervention. The PSoC™ 4200L has eight TCPWM blocks.

3.5.2 Serial Communication Blocks (SCB)

The PSoC™ 4200L has four SCBs, which can each implement an I^2C, UART, or SPI interface.

- **I^2C mode**: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EzI2C that creates a mailbox address range in the memory of the PSoC™ 4200L and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.
  The I^2C peripheral is compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.
- **UART mode**: This is a full-feature UART operating at up to 1 Mbps. It supports Automotive single-wire interface (LIN), Infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.
- **SPI mode:** The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

3.5.3 USB device

A Full-speed USB 2.0 device interface is provided. It has a Control endpoint and eight other endpoints. The interface has a USB transceiver and can be operated from the IMO obviating the need for a crystal oscillator.

3.5.4 CAN blocks

There are two independent CAN 2.0B blocks, which are certified CAN conformant.

3.6 GPIO

The PSoC™ 4200L has 96 GPIOs. The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes)
- Selectable slew rates for DV/DT related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin may be routed to any UDB through the DSI network, with the exception of pins from Port 7, 8, and 9.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (13 for PSoC™ 4200L).

There are fourteen GPIO pins that are overvoltage tolerant (V_{IN} can exceed V_{DD}). The overvoltage cells will not sink more than 10 µA when their inputs exceed V_{DDIO} in compliance with I^2C specifications. Meeting the I^2C minimum fall time requirement for FM and FM+ may require the slower slew rate setting depending on bus loading (also applies to all GPIO and SIO pins).

3.7 SIO

The special I/O (SIO) pins have the following features in addition to the GPIO features:

- Overvoltage protection and hot swap capability
- Programmable switching thresholds
- Programmable output pull-up voltage capability

They allow interfacing to buses, such as I^2C with full I^2C compatibility and interfacing to devices operating at different voltage levels. There are two SIO pins on the PSoC™ 4200L.

3.8 Special function peripherals

3.8.1 LCD segment Drive

The PSoC™ 4200L has an LCD controller, which can drive up to eight commons and up to 56 segments. Any pin can be either a common or a segment pin. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays.

3.8.2 CAPSENSE™

CAPSENSE™ is supported on all pins in the PSoC™ 4200L through two capacitive Sigma-Delta (CSD) blocks that can be connected to any pin through an Analog MUX bus that any GPIO pin can be connected to via an analog switch. CAPSENSE™ function can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CAPSENSE™ block to make it easy for the user.

The shield voltage can be driven on another MUX bus to provide water tolerance capability. The water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

Each CAPSENSE™ block has two IDACs which can be used for general purposes if CAPSENSE™ is not being used.(both IDACs are available in that case) or if CAPSENSE™ is used without water tolerance (one IDAC is available). The two CAPSENSE™ blocks can be used independently.

4 Pinouts

The following is the pin list for the PSoC™ 4200L.

Table 1 Pinout

124-BGA		124-BGA	
Pin	**Name**	**Pin**	**Name**
H13	P0.0	C3	VSSA
H12	P0.1	C5	P1.0
G13	P0.2	B5	P1.1
G12	P0.3	A5	P1.2
K10	VSSD	A4	P1.3
G11	P0.4	B4	P1.4
F13	P0.5	C4	P1.5
F12	P0.6	A3	P1.6
F11	P0.7	B3	P1.7
E13	P8.0	B1	VREF
E12	P8.1	–	–
E11	P8.2	D4	VSSA
D13	P8.3	B2	VDDA
D12	P8.4	C1	P2.0
C13	P8.5	C2	P2.1
C12	P8.6	D1	P2.2
B12	P8.7	D2	P2.3
C11	XRES	D3	P2.4
A12	VCCD	E1	P2.5
D10	VSSD	E2	P2.6
B13	VDDD	E3	P2.7
A13	VDDD	K4	VSSD
A11	P9.0	A1	VDDA
B11	P9.1	F1	P10.0
A10	P9.2	F2	P10.1
B10	P9.3	F3	P10.2
C10	P9.4	G1	P10.3
A9	P9.5	G2	P10.4
B9	P9.6	G3	P10.5
C9	P9.7	H1	P10.6
–	–	H2	P10.7
C8	P5.0	–	–
B8	P5.1	J1	P6.0
A8	P5.2	J2	P6.1
A7	P5.3	J3	P6.2
B7	P5.4	K1	P6.3

Table 1 Pinout *(continued)*

124-BGA		124-BGA	
Pin	**Name**	**Pin**	**Name**
C7	P5.5	K2	P6.4
A6	P5.6	L1	P12.0
B6	P5.7	L2	P12.1
A2	VDDA	K3	P6.5
–	–	L3	VSSD
N2	P3.0	L8	P4.0
M2	P3.1	N9	P4.1
N3	P3.2	M9	P4.2
M3	P3.3	N10	P4.3
N4	P3.4	M10	P4.4
M4	P3.5	N11	P4.5
N5	P3.6	M11	P4.6
M5	P3.7	M12	P4.7
M1	VDDIO	L11	VSSD
N1	VDDIO	L12	D+/P13.0
N6	P11.0	L13	D-/P13.1
M6	P11.1	M13	VBUS/P13.2
L6	P11.2	L9	P7.0
N7	P11.3	L10	P7.1
M7	P11.4	K13	P7.2
L7	P11.5	K12	P7.3
N8	P11.6	K11	P7.4
M8	P11.7	J13	P7.5
N12	VDDIO	J12	P7.6
N13	VDDIO	J11	P7.7

Port 12 (Port pins 12.0 and 12.1) are SIO pins.

Port 13 (Port pins 13.0 and 13.1) require VBUS (P13.2) to be powered.

Ports 6 (Port pins P6.0..6.5) and 9 (Port pins 9.0..9.7) are overvoltage tolerant (GPIO_OVT)

Balls C6, D11, H11, H3, L4, and L5 are No Connects (NC) on the 124-BGA package.

Each of the pins shown in the previous table can have multiple programmable functions as shown in the following table.

Port/pin	Analog	USB	Alt. function 1	Alt. function 2	Alt. function 3	Alt. function 4	Alt. function 5	CSD_SENSE	CSD_SHIELD
P0.0	lpcomp.in_p[0]	–	–	–	can[1].can_rx:0	usb.vbus_valid	scb[0].spi_select1:3	csd[0].sense	csd[0].shield
P0.1	lpcomp.in_n[0]	–	–	–	can[1].can_tx:0	–	scb[0].spi_select2:3	csd[0].sense	csd[0].shield
P0.2	lpcomp.in_p[1]	–	–	–	–	–	scb[0].spi_select3:3	csd[0].sense	csd[0].shield
P0.3	lpcomp.in_n[1]	–	–	–	–	–	–	csd[0].sense	csd[0].shield
P0.4	wco_in	–	–	scb[1].uart_rx:0	–	scb[1].i2c_scl:0	scb[1].spi_mosi:0	csd[0].sense	csd[0].shield
P0.5	wco_out	–	–	scb[1].uart_tx:0	–	scb[1].i2c_sda:0	scb[1].spi_miso:0	csd[0].sense	csd[0].shield
P0.6	–	–	srss.ext_clk:0	scb[1].uart_cts:0	–	–	scb[1].spi_clk:0	csd[0].sense	csd[0].shield
P0.7	–	–	–	scb[1].uart_rts:0	can[1].can_tx_enb_n:0	srss.wakeup	scb[1].spi_select0:0	csd[0].sense	csd[0].shield
P8.0	–	–	–	scb[3].uart_rx:0	–	scb[3].i2c_scl:0	scb[3].spi_mosi:0	csd[1].sense	csd[1].shield
P8.1	–	–	–	scb[3].uart_tx:0	–	scb[3].i2c_sda:0	scb[3].spi_miso:0	csd[1].sense	csd[1].shield
P8.2	–	–	–	scb[3].uart_cts:0	–	lpcomp.comp[0]:0	scb[3].spi_clk:0	csd[1].sense	csd[1].shield
P8.3	–	–	–	scb[3].uart_rts:0	–	lpcomp.comp[1]:0	scb[3].spi_select0:0	csd[1].sense	csd[1].shield
P8.4	–	–	–		–		scb[3].spi_select1:0	csd[1].sense	csd[1].shield
P8.5	–	–	–		–		scb[3].spi_select2:0	csd[1].sense	csd[1].shield
P8.6	–	–	–		–		scb[3].spi_select3:0	csd[1].sense	csd[1].shield
P8.7	–	–	–		–			csd[1].sense	csd[1].shield
P9.0	–	–	tcpwm.line[0]:2	scb[0].uart_rx:0	–	scb[0].i2c_scl:0	scb[0].spi_mosi:0	csd[1].sense	csd[1].shield
P9.1	–	–	tcpwm.line_compl[0]:2	scb[0].uart_tx:0	–	scb[0].i2c_sda:0	scb[0].spi_miso:0	csd[1].sense	csd[1].shield
P9.2	–	–	tcpwm.line[1]:2	scb[0].uart_cts:0	–	–	scb[0].spi_clk:0	csd[1].sense	csd[1].shield
P9.3	–	–	tcpwm.line_compl[1]:2	scb[0].uart_rts:0	–	–	scb[0].spi_select0:0	csd[1].sense	csd[1].shield
P9.4	–	–	tcpwm.line[2]:2	–	–	–	scb[0].spi_select1:0	csd[1].sense	csd[1].shield
P9.5	–	–	tcpwm.line_compl[2]:2	–	–	–	scb[0].spi_select2:0	csd[1].sense	csd[1].shield
P9.6	–	–	tcpwm.line[3]:2	–	–	scb[3].i2c_scl:3	scb[0].spi_select3:0	csd[1].sense	csd[1].shield
P9.7	–	–	tcpwm.line_compl[3]:2	–	–	scb[3].i2c_sda:3	–	csd[1].sense	csd[1].shield
P5.0	ctb1_pads[0] csd[1].c_mod Csd[1].CintA	–	tcpwm.line[4]:2	scb[2].uart_rx:0	–	scb[2].i2c_scl:0	scb[2].spi_mosi:0	csd[1].sense	csd[1].shield
P5.1	ctb1_pads[1] csd[1].c_sh_tank Csd[1].CintB	–	tcpwm.line_compl[4]:2	scb[2].uart_tx:0	–	scb[2].i2c_sda:0	scb[2].spi_miso:0	csd[1].sense	csd[1].shield
P5.2	ctb1_pads[2] ctb1_oa0_out_10x	–	tcpwm.line[5]:2	scb[2].uart_cts:0	–	lpcomp.comp[0]:1	scb[2].spi_clk:0	csd[1].sense	csd[1].shield
P5.3	ctb1_pads[3] ctb1_oa1_out_10x	–	tcpwm.line_compl[5]:2	scb[2].uart_rts:0	–	lpcomp.comp[1]:1	scb[2].spi_select0:0	csd[1].sense	csd[1].shield
P5.4	ctb1_pads[4]	–	tcpwm.line[6]:2	–	–	–	scb[2].spi_select1:0	csd[1].sense	csd[1].shield
P5.5	ctb1_pads[5]	–	tcpwm.line_compl[6]:2	–	–	–	scb[2].spi_select2:0	csd[1].sense	csd[1].shield
P5.6	ctb1_pads[6]	–	tcpwm.line[7]:2	–	–	–	scb[2].spi_select3:0	csd[1].sense	csd[1].shield
P5.7	ctb1_pads[7]	–	tcpwm.line_compl[7]:2	–	–	–		csd[1].sense	csd[1].shield

Port/pin	Analog	USB	Alt. function 1	Alt. function 2	Alt. function 3	Alt. function 4	Alt. function 5	CSD_SENSE	CSD_SHIELD
P1.0	ctb0_pads[0]	–	tcpwm.line[2]:1	scb[0].uart_rx:1	–	scb[0].i2c_scl:1	scb[0].spi_mosi:1	csd[0].sense	csd[0].shield
P1.1	ctb0_pads[1]	–	tcpwm.line_compl[2]:1	scb[0].uart_tx:1	–	scb[0].i2c_sda:1	scb[0].spi_miso:1	csd[0].sense	csd[0].shield
P1.2	ctb0_pads[2] ctb0_oa0_out_10x	–	tcpwm.line[3]:1	scb[0].uart_cts:1	–	–	scb[0].spi_clk:1	csd[0].sense	csd[0].shield
P1.3	ctb0_pads[3] ctb0_oa1_out_10x	–	tcpwm.line_compl[3]:1	scb[0].uart_rts:1	–	–	scb[0].spi_select0:1	csd[0].sense	csd[0].shield
P1.4	ctb0_pads[4]	–	tcpwm.line[6]:1	–	–	–	scb[0].spi_select1:1	csd[0].sense	csd[0].shield
P1.5	ctb0_pads[5]	–	tcpwm.line_compl[6]:1	–	–	–	scb[0].spi_select2:1	csd[0].sense	csd[0].shield
P1.6	ctb0_pads[6]	–	tcpwm.line[7]:1	–	–	–	scb[0].spi_select3:1	csd[0].sense	csd[0].shield
P1.7	ctb0_pads[7], sar_ext_vref	–	tcpwm.line_compl[7]:1	–	–	–		csd[0].sense	csd[0].shield
P2.0	sarmux_pads[0]	–	tcpwm.line[4]:1	scb[1].uart_rx:1	–	scb[1].i2c_scl:1	scb[1].spi_mosi:1	csd[0].sense	csd[0].shield
P2.1	sarmux_pads[1]	–	tcpwm.line_compl[4]:1	scb[1].uart_tx:1	–	scb[1].i2c_sda:1	scb[1].spi_miso:1	csd[0].sense	csd[0].shield
P2.2	sarmux_pads[2]	–	tcpwm.line[5]:1	scb[1].uart_cts:1	–	–	scb[1].spi_clk:1	csd[0].sense	csd[0].shield
P2.3	sarmux_pads[3]	–	tcpwm.line_compl[5]:1	scb[1].uart_rts:1	–	–	scb[1].spi_select0:1	csd[0].sense	csd[0].shield
P2.4	sarmux_pads[4]	–	tcpwm.line[0]:1	–	–	–	scb[1].spi_select1:0	csd[0].sense	csd[0].shield
P2.5	sarmux_pads[5]	–	tcpwm.line_compl[0]:1	–	–	–	scb[1].spi_select2:0	csd[0].sense	csd[0].shield
P2.6	sarmux_pads[6]	–	tcpwm.line[1]:1	–	–	–	scb[1].spi_select3:0	csd[0].sense	csd[0].shield
P2.7	sarmux_pads[7]	–	tcpwm.line_compl[1]:1	–	–	–	–	csd[0].sense	csd[0].shield
P10.0	–	–	–	scb[2].uart_rx:1	–	scb[2].i2c_scl:1	scb[2].spi_mosi:1	csd[0].sense	csd[0].shield
P10.1	–	–	–	scb[2].uart_tx:1	–	scb[2].i2c_sda:1	scb[2].spi_miso:1	csd[0].sense	csd[0].shield
P10.2	–	–	–	scb[2].uart_cts:1	–	–	scb[2].spi_clk:1	csd[0].sense	csd[0].shield
P10.3	–	–	–	scb[2].uart_rts:1	–	–	scb[2].spi_select0:1	csd[0].sense	csd[0].shield
P10.4	–	–	–	–	–	–	scb[2].spi_select1:1	csd[0].sense	csd[0].shield
P10.5	–	–	–	–	–	–	scb[2].spi_select2:1	csd[0].sense	csd[0].shield
P10.6	–	–	–	–	–	–	scb[2].spi_select3:1	csd[0].sense	csd[0].shield
P10.7	–	–	–	–	–	–	–	csd[0].sense	csd[0].shield
P6.0	–	–	tcpwm.line[4]:0	scb[3].uart_rx:1	can[0].can_tx_enb_n:0	scb[3].i2c_scl:1	scb[3].spi_mosi:1	csd[0].sense	csd[0].shield
P6.1	–	–	tcpwm.line_compl[4]:0	scb[3].uart_tx:1	can[0].can_rx:0	scb[3].i2c_sda:1	scb[3].spi_miso:1	csd[0].sense	csd[0].shield
P6.2	–	–	tcpwm.line[5]:0	scb[3].uart_cts:1	can[0].can_tx:0	scb[2].i2c_scl:3	scb[3].spi_clk:1	csd[0].sense	csd[0].shield
P6.3	–	–	tcpwm.line_compl[5]:0	scb[3].uart_rts:1	–	scb[2].i2c_sda:3	scb[3].spi_select0:1	csd[0].sense	csd[0].shield
P6.4	–	–	tcpwm.line[6]:0	–	–	scb[0].i2c_scl:3	scb[3].spi_select1:1	csd[0].sense	csd[0].shield
P12.0	–	–	tcpwm.line[7]:0	–	–	scb[1].i2c_scl:3	scb[3].spi_select3:1	–	–
P12.1	–	–	tcpwm.line_compl[7]:0	–	–	scb[1].i2c_sda:3	–	–	–
P6.5	–	–	tcpwm.line_compl[6]:0	–	–	scb[0].i2c_sda:3	scb[3].spi_select2:1	csd[0].sense	csd[0].shield

Port/pin	Analog	USB	Alt. function 1	Alt. function 2	Alt. function 3	Alt. function 4	Alt. function 5	CSD_SENSE	CSD_SHIELD
P3.0	–	–	tcpwm.line[0]:0	scb[1].uart_rx:2	–	scb[1].i2c_scl:2	scb[1].spi_mosi:2	csd[0].sense	csd[0].shield
P3.1	–	–	tcpwm.line_compl[0]:0	scb[1].uart_tx:2	–	scb[1].i2c_sda:2	scb[1].spi_miso:2	csd[0].sense	csd[0].shield
P3.2	–	–	tcpwm.line[1]:0	scb[1].uart_cts:2	–	cpuss.swd_data:0	scb[1].spi_clk:2	csd[0].sense	csd[0].shield
P3.3	–	–	tcpwm.line_compl[1]:0	scb[1].uart_rts:2	–	cpuss.swd_clk:0	scb[1].spi_select0:2	csd[0].sense	csd[0].shield
P3.4	–	–	tcpwm.line[2]:0	–	–	–	scb[1].spi_select1:1	csd[0].sense	csd[0].shield
P3.5	–	–	tcpwm.line_compl[2]:0	–	–	–	scb[1].spi_select2:1	csd[0].sense	csd[0].shield
P3.6	–	–	tcpwm.line[3]:0	–	–	–	scb[1].spi_select3:1	csd[0].sense	csd[0].shield
P3.7	–	–	tcpwm.line_compl[3]:0	–	–	–	–	csd[0].sense	csd[0].shield
P11.0	–	–	tcpwm.line[4]:3	scb[2].uart_rx:2	–	scb[2].i2c_scl:2	scb[2].spi_mosi:2	csd[0].sense	csd[0].shield
P11.1	–	–	tcpwm.line_compl[4]:3	scb[2].uart_tx:2	–	scb[2].i2c_sda:2	scb[2].spi_miso:2	csd[0].sense	csd[0].shield
P11.2	–	–	tcpwm.line[5]:3	scb[2].uart_cts:2	–	cpuss.swd_data:1	scb[2].spi_clk:2	csd[0].sense	csd[0].shield
P11.3	–	–	tcpwm.line_compl[5]:3	scb[2].uart_rts:2	–	cpuss.swd_clk:1	scb[2].spi_select0:2	csd[0].sense	csd[0].shield
P11.4	–	–	tcpwm.line[6]:3		–	–	scb[2].spi_select1:2	csd[0].sense	csd[0].shield
P11.5	–	–	tcpwm.line_compl[6]:3		–	–	scb[2].spi_select2:2	csd[0].sense	csd[0].shield
P11.6	–	–	tcpwm.line[7]:3		–	–	scb[2].spi_select3:2	csd[0].sense	csd[0].shield
P11.7	–	–	tcpwm.line_compl[7]:3		–	–	–	csd[0].sense	csd[0].shield
P4.0	–	–	–	scb[0].uart_rx:2	can[0].can_rx:1	scb[0].i2c_scl:2	scb[0].spi_mosi:2	csd[0].sense	csd[0].shield
P4.1	–	–	–	scb[0].uart_tx:2	can[0].can_tx:1	scb[0].i2c_sda:2	scb[0].spi_miso:2	csd[0].sense	csd[0].shield
P4.2	csd[0].c_mod Csd[0].CintA	–	–	scb[0].uart_cts:2	can[0].can_tx_enb_n:1	lpcomp.comp[0]:2	scb[0].spi_clk:2	csd[0].sense	csd[0].shield
P4.3	csd[0].c_sh_tank Csd[0].CintB	–	–	scb[0].uart_rts:2		lpcomp.comp[1]:2	scb[0].spi_select0:2	csd[0].sense	csd[0].shield
P4.4	–	–	–	–	can[1].can_tx_enb_n:1	–	scb[0].spi_select1:2	csd[0].sense	csd[0].shield
P4.5	–	–	–	–	can[1].can_rx:1	–	scb[0].spi_select2:2	csd[0].sense	csd[0].shield
P4.6	–	–	–	–	can[1].can_tx:1	–	scb[0].spi_select3:2	csd[0].sense	csd[0].shield
P4.7	–	–	–	–	–	–	–	csd[0].sense	csd[0].shield
P13.0	–	USBDP	–	–	–	–	–	–	–
P13.1	–	USBDM	–	–	–	–	–	–	–
P13.2	–	VBUS	–	–	–	–	–	–	–
P7.0	srss.eco_in	–	tcpwm.line[0]:3	scb[3].uart_rx:2	–	scb[3].i2c_scl:2	scb[3].spi_mosi:2	csd[0].sense	csd[0].shield
P7.1	srss.eco_out	–	tcpwm.line_compl[0]:3	scb[3].uart_tx:2	–	scb[3].i2c_sda:2	scb[3].spi_miso:2	csd[0].sense	csd[0].shield
P7.2	–	–	tcpwm.line[1]:3	scb[3].uart_cts:2	–	–	scb[3].spi_clk:2	csd[0].sense	csd[0].shield
P7.3	–	–	tcpwm.line_compl[1]:3	scb[3].uart_rts:2	–	–	scb[3].spi_select0:2	csd[0].sense	csd[0].shield
P7.4	–	–	tcpwm.line[2]:3	–	–	–	scb[3].spi_select1:2	csd[0].sense	csd[0].shield
P7.5	–	–	tcpwm.line_compl[2]:3	–	–	–	scb[3].spi_select2:2	csd[0].sense	csd[0].shield
P7.6	–	–	tcpwm.line[3]:3	–	–	–	scb[3].spi_select3:2	csd[0].sense	csd[0].shield
P7.7	–	–	tcpwm.line_compl[3]:3	–	–	–	–	csd[0].sense	csd[0].shield

Descriptions of the power pin functions are as follows:

VDDD: Power supply for both analog and digital sections (where there is no V_{DDA} pin)

VDDA: Analog V_{DD} pin where package pins allow; should be present before or concurrently with VDDD and the value of VDDA should be equal to or higher than VDDD and VDDIO

VDDIO: I/O pin power domain. It should not be present without VDDD.

VSSA: Analog ground pin where package pins allow; shorted to VSS otherwise

VSS: Ground pin

VCCD: Regulated digital supply (1.8 V ±5%)

VBUS: USB voltage. There is no constraint on VBUS with respect to VDDD. However, since it comes from USB, it is typically assumed to and ideally be 5 V (4.35 to 5.5 V is the range).

GPIO and GPIO_OVT pins can be used as CSD sense and shield pins (a total of 96). Up to 64 of the pins can be used for LCD drive.

The following package is supported: 124-ball BGA.

5 Power

The supply voltage range is 1.71 V to 5.5 V with all functions and circuits operating over that range.

The PSoC™ 4200L family allows two distinct modes of power supply operation: Unregulated external supply and regulated external supply modes.

5.1 Unregulated external supply

In this mode, the PSoC™ 4200L is powered by an external power supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC™ 4200L supplies the internal logic and the VCCD output of the PSoC™ 4200L must be bypassed to ground via an external Capacitor (in the range of 1-to 1.6-µF; X5R ceramic or better).

VDDA and VDDD must be shorted together on the PC board; the grounds, VSSA and VSS must also be shorted together. Bypass capacitors must be used from VDDD and VDDA to ground, typical practice for systems in this frequency range is to use a capacitor in the 1 µF range in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Power supply	Bypass capacitors
VDDD–VSS and VDDIO-VSS	0.1 µF ceramic at each pin plus bulk capacitor 1 to 10 µF
VDDA–VSSA	0.1 µF ceramic at pin. Additional 1 to 10 µF bulk capacitor
VCCD–VSS	1 µF ceramic capacitor at the VCCD pin
VREF–VSSA (optional)	The internal bandgap may be bypassed with a 1 µF to 10 µF capacitor for better ADC performance.

5.2 Regulated external supply

In this mode, the PSoC™ 4200L is powered by an external power supply that must be within the range of 1.71 V to 1.89 V (1.8 ±5%); note that this range needs to include power supply ripple. In this mode, the VCCD and VDDD pins are shorted together and bypassed. The internal regulator is disabled in firmware.

6 Electrical specifications

6.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID1	V_{DD_ABS}	Analog or digital supply relative to V_{SS} ($V_{SSD} = V_{SSA}$)	–0.5	–	6	V	Absolute maximum
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.5	–	1.95	V	Absolute maximum
SID3	V_{GPIO_ABS}	GPIO voltage; V_{DDD} or V_{DDA}	–0.5	–	V_{DD} + 0.5	V	Absolute maximum
SID4	I_{GPIO_ABS}	Current per GPIO	–25	–	25	mA	Absolute maximum
SID5	IG-PIO_injection	GPIO injection current per pin	–0.5	–	0.5	mA	Absolute maximum
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
BID46	LU	Pin current for latch-up	–140	–	140	mA	–

Note
1. Usage above the absolute maximum conditions listed in **Table 2** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

6.2 Device level specifications

All specifications are valid for –40°C ≤ T_A ≤ 105°C and T_J ≤ 125°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 3 DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID53	V_{DDD}	Power supply input voltage ($V_{DDA} = V_{DDD} = V_{DD}$)	1.8	–	5.5	V	With regulator enabled
SID255	V_{DDD}	Power supply input voltage unregulated	1.71	1.8	1.89	V	Internally unregulated supply
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	–
SID55	C_{EFC}	External regulator voltage (V_{CCD}) bypass	1	1.3	1.6	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply decoupling capacitor	–	1	–	µF	X5R ceramic or better
Active mode							
SID6	I_{DD1}	Execute from flash; CPU at 6 MHz	–	2.2	3.1	mA	–
SID7	I_{DD2}	Execute from flash; CPU at 12 MHz	–	3.7	4.8	mA	–
SID8	I_{DD3}	Execute from flash; CPU at 24 MHz	–	6.7	8.0	mA	–
SID9	I_{DD4}	Execute from flash; CPU at 48 MHz	–	12.8	14.5	mA	–

Table 3 DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Sleep mode							
SID21	I_{DD16}	I^2C wakeup, WDT, and Comparators ON. Regulator OFF.	–	–	2.9	mA	V_{DD} = 1.71 to 1.89, 6 MHz
SID22	I_{DD17}	I^2C wakeup, WDT, and Comparators oON.	–	1.7	2.1	mA	V_{DD} = 1.8 to 5.5, 6 MHz
SID23	I_{DD18}	I^2C wakeup, WDT, and Comparators ON. Regulator OFF.	–	2.4	2.9	mA	V_{DD} = 1.71 to 1.89, 12 MHz
SID24	I_{DD19}	I^2C wakeup, WDT, and Comparators ON.	–	2.3	2.8	mA	V_{DD} = 1.8 to 5.5, 12 MHz
Deep Sleep mode, –40°C to +60°C							
SID30	I_{DD25}	I^2C wakeup and WDT ON, Regulator OFF.	–	–	13.5	µA	V_{DD} = 1.71 to 1.89
SID31	I_{DD26}	I^2C wakeup and WDT ON	–	1.3	20.0	µA	V_{DD} = 1.8 to 3.6
SID32	I_{DD27}	I^2C wakeup and WDT ON	–	–	20.0	µA	V_{DD} = 3.6 to 5.5
Deep Sleep mode, +85°C							
SID33	I_{DD28}	I^2C wakeup and WDT ON, Regulator OFF	–	–	45.0	µA	V_{DD} = 1.71 to 1.89
SID34	I_{DD29}	I^2C wakeup and WDT ON	–	15	60.0	µA	V_{DD} = 1.8 to 3.6
SID35	I_{DD30}	I^2C wakeup and WDT ON	–	–	45.0	µA	V_{DD} = 3.6 to 5.5
Hibernate mode, –40°C to +60°C							
SID39	I_{DD34}	Regulator OFF	–	–	1123	nA	V_{DD} = 1.71 to 1.89
SID40	I_{DD35}		–	150	1600	nA	V_{DD} = 1.8 to 3.6
SID41	I_{DD36}		–	–	1600	nA	V_{DD} = 3.6 to 5.5
Hibernate mode, +85°C							
SID42	I_{DD37}	Regulator OFF	–	–	4142	nA	V_{DD} = 1.71 to 1.89
SID43	I_{DD38}		–	–	9700	nA	V_{DD} = 1.8 to 3.6
SID44	I_{DD39}		–	–	10,400	nA	V_{DD} = 3.6 to 5.5
Stop mode							
SID304	I_{DD43A}	Stop mode current; V_{DD} = 3.6 V	–	20	659	nA	T = –40°C to +60°C
SID304A	I_{DD43B}	Stop mode current; V_{DD} = 3.6 V	–	–	1810	nA	T = +85°C
XRES current							
SID307	I_{DD_XR}	Supply current while XRES (Active Low) asserted	–	2	5	mA	–

Table 4 AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID48	F_{CPU}	CPU frequency	DC	–	48	MHz	$1.71 \le V_{DD} \le 5.5$
SID49	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	Guaranteed by characterization
SID50	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	25	µs	24-MHz IMO. Guaranteed by characterization
SID51	$T_{HIBERNATE}$	Wakeup from Hibernate mode	–	–	0.7	ms	Guaranteed by characterization
SID51A	T_{STOP}	Wakeup from Stop mode	–	–	1.9	ms	Guaranteed by characterization
SID52	$T_{RESETWIDTH}$	External reset pulse width	1	–	–	µs	Guaranteed by characterization

6.2.1 GPIO

Table 5 GPIO DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID57	V_{IH}[2]	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID57A	I_{IHS}	Input current when Pad > V_{DDIO} for OVT inputs	–	–	10	µA	per I^2C Spec
SID58	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID241	V_{IH}[2]	LVTTL input, V_{DDD} < 2.7 V	0.7 × V_{DDD}	–	–	V	–
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}	V	–
SID243	V_{IH}[2]	LVTTL input, $V_{DDD} \geq 2.7$ V	–	–	2.0	V	–
SID244	V_{IL}	LVTTL input, $V_{DDD} \geq 2.7$ V	0.8	–	–	V	–
SID59	V_{OH}	Output voltage HIGH level	V_{DDD} – 0.6	–	–	V	I_{OH} = 4 mA, $V_{DDD} \geq 3$ V
SID60	V_{OH}	Output voltage HIGH level	V_{DDD} – 0.5	–	–	V	I_{OH} = 1 mA at 1.8 V V_{DDD}
SID61	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 8 mA, $V_{DDD} \geq 3$ V
SID62A	V_{OL}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 3 mA, $V_{DDD} \geq 3$ V
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25°C, V_{DDD} = 3.0 V
SID65A	I_{IL_CTBM}	Input leakage current (absolute value) for CTBM pins	–	–	4	nA	–
SID66	C_{IN}	Input capacitance	–	–	7	pF	Not applicable for P6.4, P6.5, P12.0, P12.1, and for USB pins.
SID67	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DDD} \geq 2.7$ V
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	–
SID69	I_{DIODE}	Current through protection diode to V_{DD}/Vss	–	–	100	µA	Guaranteed by characterization
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200	mA	Guaranteed by characterization

Note
2. V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 6 GPIO AC specifications

(Guaranteed by characterization)[3]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in Slow Strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in Slow Strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Fast Strong mode.	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout;1.7 V≤ V_{DDD}≤ 3.3 V. Fast Strong mode.	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Slow Strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout;1.7 V ≤ V_{DDD} ≤ 3.3 V. Slow Strong mode.	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

6.2.2 XRES

Table 7 XRES DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID80	C_{IN}	Input capacitance	–	3	–	pF	–
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by characterization

Table 8 XRES AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	Guaranteed by characterization

Note

3. Simultaneous switching transitions on many fully-loaded GPIO pins may cause ground perturbations depending on several factors including PCB and decoupling capacitor design. For applications that are very sensitive to ground perturbations, the slower GPIO slew rate setting may be used.

6.3 Analog peripherals

6.3.1 Opamp

Table 9 Opamp specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
	I_{DD}	Opamp block current. No load.	–	–	–	–	–
SID269	I_{DD_HI}	Power = high	–	1100	1850	µA	–
SID270	I_{DD_MED}	Power = medium	–	550	950	µA	–
SID271	I_{DD_LOW}	Power = low	–	150	350	µA	–
	GBW	Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V	–	–	–	–	–
SID272	GBW_HI	Power = high	6	–	–	MHz	–
SID273	GBW_MED	Power = medium	4	–	–	MHz	–
SID274	GBW_LO	Power = low	–	1	–	MHz	–
	I_{OUT_MAX}	$V_{DDA} \geq 2.7$ V, 500 mV from rail	–	–	–	–	–
SID275	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	–
SID276	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	–
SID277	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	–
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail	–	–	–	–	–
SID278	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	–
SID279	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	–
SID280	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	–
SID281	V_{IN}	Input voltage range	–0.05	–	V_{DDA} – 0.2	V	Charge-pump ON, $V_{DDA} \geq 2.7$ V
SID282	V_{CM}	Input common mode voltage	–0.05	–	VDDA – 0.2	V	Charge-pump ON, $V_{DDA} \geq 2.7$ V
	V_{OUT}	$V_{DDA} \geq 2.7$ V	–	–	–		–
SID283	V_{OUT_1}	Power = high, I_{load}=10 mA	0.5	–	VDDA – 0.5	V	–
SID284	V_{OUT_2}	Power = high, I_{load}=1 mA	0.2	–	VDDA – 0.2	V	–
SID285	V_{OUT_3}	Power = medium, I_{load}=1 mA	0.2	–	VDDA – 0.2	V	–
SID286	V_{OUT_4}	Power = low, I_{load}=0.1mA	0.2	–	VDDA – 0.2	V	–
SID288	V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Low mode
SID291	CMRR	DC	60	70	–	dB	V_{DDD} = 3.6 V
SID292	PSRR	At 1 kHz, 100 mV ripple	70	85	–	dB	VDDD = 3.6 V

Table 9 Opamp specifications

(Guaranteed by characterization) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
	Noise		–	–	–	–	–
SID293	V_{N1}	Input referred, 1 Hz - 1GHz, power = high	–	94	–	µVrms	–
SID294	V_{N2}	Input referred, 1 kHz, power = high	–	72	–	nV/rtHz	–
SID295	V_{N3}	Input referred, 10kHz, power = high	–	28	–	nV/rtHz	–
SID296	V_{N4}	Input referred, 100kHz, power = high	–	15	–	nV/rtHz	–
SID297	Cload	Stable up to maximum load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	Slew_rate	Cload = 50 pF, power = high, $V_{DDA} \geq 2.7$ V	6	–	–	V/µs	–
SID299	T_op_wake	From disable to enable, no external RC dominating	–	25	–	µs	–
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	–
	Comp_mode	Comparator mode; 50 mV drive, $T_{rise} = T_{fall}$ (approx.)	–	–	–		–
SID300	T_{PD1}	Response time; power = high	–	150	–	ns	–
SID301	T_{PD2}	Response time; power = medium	–	400	–	ns	–
SID302	T_{PD3}	Response time; power = low	–	2000	–	ns	–
SID303	Vhyst_op	Hysteresis	–	10	–	mV	–
Deep Sleep mode		Mode 2 is lowest current range. Mode 1 has higher GBW.					Deep Sleep mode $V_{DDA} \geq 2.7$ V
SID_DS_1	IDD_HI_M1	Mode 1, High current	–	1400	–	µA	25°C
SID_DS_2	IDD_MED_M1	Mode 1, Medium current	–	700	–	µA	25°C
SID_DS_3	IDD_LOW_M1	Mode 1, Low current	–	200	–	µA	25°C
SID_DS_4	IDD_HI_M2	Mode 2, High current	–	120	–	µA	25°C
SID_DS_5	IDD_MED_M2	Mode 2, Medium current	–	60	–	µA	25°C
SID_DS_6	IDD_LOW_M2	Mode 2, Low current	–	15	–	µA	25°C
SID_DS_7	GBW_HI_M1	Mode 1, High current	–	4	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} – 1.5 V
SID_DS_8	GBW_MED_M1	Mode 1, Medium current	–	2	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} – 1.5 V
SID_DS_9	GBW_LOW_M1	Mode 1, Low current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} – 1.5 V

Table 9 Opamp specifications

(Guaranteed by characterization) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID_DS_10	GBW_HI_M2	Mode 2, High current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} – 1.5 V
SID_DS_11	GBW_MED_M2	Mode 2, Medium current	–	0.2	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} – 1.5 V
SID_DS_12	GBW_LOW_M2	Mode 2, Low current	–	0.1	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} – 1.5 V
SID_DS_13	VOS_HI_M1	Mode 1, High current	–	5	–	mV	With trim 25°C, 0.2 V to V_{DDA} – 1.5 V
SID_DS_14	VOS_MED_M1	Mode 1, Medium current	–	5	–	mV	With trim 25°C, 0.2 V to V_{DDA} – 1.5 V
SID_DS_15	VOS_LOW_M1	Mode 1, Low current	–	5	–	mV	With trim 25°C, 0.2 V to V_{DDA} – 1.5 V
SID_DS_16	VOS_HI_M2	Mode 2, High current	–	5	–	mV	With trim 25°C, 0.2 V to V_{DDA} – 1.5 V
SID_DS_17	VOS_MED_M2	Mode 2, Medium current	–	5	–	mV	With trim 25°C, 0.2 V to V_{DDA} – 1.5 V
SID_DS_18	VOS_LOW_M2	Mode 2, Low current	–	5	–	mV	With trim 25°C, 0.2 V to V_{DDA}-1.5 V
SID_DS_19	IOUT_HI_M1	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_20	IOUT_MED_M1	Mode 1, Medium current	–	10	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_21	IOUT_LOW_M1	Mode 1, Low current	–	4	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_22	IOUT_HI_M2	Mode 2, High current	–	1	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_23	IOUT_MED_M2	Mode 2, Medium current	–	1	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_24	IOUT_LOW_M2	Mode 2, Low current	–	0.5	–	mA	Output is 0.5 V to V_{DDA}-0.5 V

6.3.2 Comparator

Table 10 Comparator DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID85	$V_{OFFSET2}$	Input offset voltage. Custom trim. Common mode voltage range from 0 to V_{DD}-1.	–	–	±4	mV	–
SID85A	$V_{OFFSET3}$	Input offset voltage. Ultra low-power mode.	–	±12	–	mV	V_{DDD} ≥ 2.2 V for temp < 0°C, V_{DDD} ≥ 1.8 V for temp > 0°C
SID86	V_{HYST}	Hysteresis when enabled. Common mode voltage range from 0 to V_{DD} -1.	–	10	35	mV	Guaranteed by characterization
SID87	V_{ICM1}	Input common mode voltage in Normal mode	0	–	V_{DDD} – 0.2	V	Modes 1 and 2
SID247	V_{ICM2}	Input common mode voltage in low power mode	0	–	V_{DDD}	V	–
SID247A	V_{ICM2}	Input common mode voltage in Ultra low-power mode	0	–	V_{DDD} – 1.15	V	V_{DDD} ≥ 2.2 V for temp < 0°C, V_{DDD} ≥ 1.8 V for Temp > 0°C
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	V_{DDD} ≥ 2.7 V. Guaranteed by characterization
SID88A	CMRR	Common mode rejection ratio	42	–	–	dB	V_{DDD} < 2.7 V. Guaranteed by characterization
SID89	I_{CMP1}	Block current, Normal mode	–	280	400	µA	Guaranteed by characterization
SID248	I_{CMP2}	Block current, Low-power mode	–	50	100	µA	Guaranteed by characterization
SID259	I_{CMP3}	Block current, Ultra low- power mode	–	6	28	µA	Guaranteed by characterization, V_{DDD} ≥ 2.2 V for temp < 0°C, V_{DDD} ≥ 1.8 V for temp > 0°C
SID90	Z_{CMP}	DC input impedance of comparator	35	–	–	MΩ	Guaranteed by characterization

Table 11 Comparator AC specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID91	T_{RESP1}	Response time, Normal mode	–	38	110	ns	50-mV overdrive
SID258	T_{RESP2}	Response time, Low-power mode	–	70	200	ns	50-mV overdrive
SID92	T_{RESP3}	Response time, Ultra low-power mode	–	2.3	15	µs	200-mV overdrive. V_{DDD} ≥ 2.2 V for temp < 0°C, V_{DDD} ≥ 1.8 V for temp > 0°C

6.3.3 Temperature sensor

Table 12 Temperature sensor specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	+5	°C	–40°C to +85°C

6.3.4 SAR ADC

Table 13 SAR ADC DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID94	A_RES	Resolution	–	–	12	bits	–
SID95	A_CHNIS_S	Number of channels - single ended	–	–	16	–	–
SID96	A-CHNKS_D	Number of channels - differential	–	–	8	–	Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–	–	Yes, based on the characterization
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V_{REF}
SID100	A_ISAR	Current consumption	–	–	1	mA	–
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID103	A_INRES	Input resistance	–	–	2.2	kΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	–	–	10	pF	Based on device characterization

Table 14 SAR ADC AC specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	–
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP_1	Sample rate with external reference bypass cap	–	–	1	Msps	–
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}	–	–	500	ksps	–
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference	–	–	100	ksps	–
SID109	A_SNDR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	F_{IN} = 10 kHz
SID111	A_INL	Integral non linearity	–1.7	–	+2	LSB	V_{DD} = 1.71 to 5.5, 1 Msps, V_{REF} = 1 to 5.5

Table 14 SAR ADC AC specifications

(Guaranteed by characterization) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID111A	A_INL	Integral non linearity	–1.5	–	+1.7	LSB	V_{DDD} = 1.71 to 3.6, 1 Msps, V_{REF} = 1.71 to V_{DDD}
SID111B	A_INL	Integral non linearity	–1.5	–	+1.7	LSB	V_{DDD} = 1.71 to 5.5, 500 ksps, V_{REF} = 1 to 5.5
SID112	A_DNL	Differential non linearity	–1	–	+2.2	LSB	V_{DDD} = 1.71 to 5.5, 1 Msps, V_{REF} = 1 to 5.5
SID112A	A_DNL	Differential non linearity	–1	–	+2	LSB	V_{DDD} = 1.71 to 3.6, 1 Msps, V_{REF} = 1.71 to V_{DDD}
SID112B	A_DNL	Differential non linearity	–1	–	+2.2	LSB	V_{DDD} = 1.71 to 5.5, 500 ksps, V_{REF} = 1 to 5.5
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	F_{IN} = 10 kHz

6.3.5 CSD

Table 15 CSD block specification

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
CSD specification							
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	–
SID309	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	–
SID310	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	–
SID311	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	–
SID312	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	–
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity
SID314	IDAC1_CRT1	Output current of Idac1 (8-bits) in high range	–	612	–	µA	–
SID314A	IDAC1_CRT2	Output current of Idac1(8-bits) in low range	–	306	–	µA	–
SID315	IDAC2_CRT1	Output current of Idac2 (7-bits) in high range	–	304.8	–	µA	–
SID315A	IDAC2_CRT2	Output current of Idac2 (7-bits) in low range	–	152.4	–	µA	–

6.4 Digital peripherals

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode.

6.4.1 Timer/counter/PWM

Table 16 TCPWM specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (Timer/Counter/ PWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155	µA	All modes (Timer/Counter/ PWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650	µA	All modes (Timer/Counter/ PWM)
SID.TCPWM.3	TCPWMFREQ	Operating frequency	–	–	Fc	MHz	Fc max = Fcpu. Maximum = 48 MHz
SID.TCPWM.4	TPWMENEXT	Input trigger pulse width for all Trigger events	2/Fc	–	–	ns	Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected
SID.TCPWM.5	TPWMEXT	Output trigger pulse widths	2/Fc	–	–	ns	Minimum possible width of overflow, underflow, and CC (counter equals compare value) trigger outputs
SID.TCPWM.5A	TCRES	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs.

6.4.2 I²C

Table 17 Fixed I²C DC specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	10.5	55	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310	µA	–
SID152	I_{I2C4}	I²C enabled in Deep Sleep mode	–	–	1.4	µA	–

Table 18 Fixed I²C AC specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

6.4.3 LCD direct drive

Table 19 LCD direct drive DC specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	µA	16 × 4 small segment disp. at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	Guaranteed by Design
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	PWM Mode current. 5-V bias. 24-MHz IMO	–	0.6	–	mA	32 × 4 segments 50 Hz, 25°C
SID158	I_{LCDOP2}	PWM Mode current. 3.3-V bias. 24-MHz IMO.	–	0.5	–	mA	32 × 4 segments 50 Hz, 25°C

Table 20 LCD direct drive AC specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Table 21 Fixed UART DC specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	9	55	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	312	µA	–

Table 22 Fixed UART AC specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	F_{UART}	Bit Rate	–	–	1	Mbps	–

6.4.4 SPI specifications

Table 23 Fixed SPI DC specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit
SID163	I_{SPI1}	Block current consumption at 1 Mbits/sec	–	–	360	µA
SID164	I_{SPI2}	Block current consumption at 4 Mbits/sec	–	–	560	µA
SID165	I_{SPI3}	Block current consumption at 8 Mbits/sec	–	–	600	µA

Table 24 Fixed SPI AC specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit
SID166	F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz

Table 25 Fixed SPI master mode AC specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit
SID167	T_{DMO}	MOSI valid after Sclock driving edge	–	–	15	ns
SID168	T_{DSI}	MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used	20	–	–	ns
SID169	T_{HMO}	Previous MOSI data hold time with respect to capturing edge at Slave	0	–	–	ns

Table 26 Fixed SPI slave mode AC specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns
SID171	T_{DSO}	MISO valid after Sclock driving edge	–	–	$42+3\times T_{SCB}$	ns
SID171A	T_{DSO_ext}	MISO valid after Sclock driving edge in Ext. Clock mode	–	–	48	ns
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns

6.5 Memory

Table 27 Flash DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 28 Flash AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID174	$T_{ROWWRITE}$	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 256 bytes
SID175	$T_{ROWERASE}$	Row erase time	–	–	13	ms	–
SID176	$T_{ROWPROGRAM}$	Row program time after erase	–	–	7	ms	–
SID178	$T_{BULKERASE}$	Bulk erase time (128 KB)	–	–	35	ms	–
SID180	$T_{DEVPROG}$	Total device program time	–	–	15	seconds	Guaranteed by characterization
SID181	F_{END}	Flash endurance	100 k	–	–	cycles	Guaranteed by characterization
SID182	F_{RET}	Flash retention. $T_A \leq 55°C$, 100 k P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A		Flash retention. $T_A \leq 85°C$, 10 k P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	F_{RETQ}	Flash retention. $T_A \leq 105°C$, 10 k P/E cycles, ≤ three years at $T_A \geq 85°C$	10	20	–	years	Guaranteed by characterization

6.6 System resources

6.6.1 Power-on reset (POR) with brown out

Table 29 Imprecise power-on reset (PRES)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization
SID187	$V_{IPORHYST}$	Hysteresis	15	–	200	mV	Guaranteed by characterization

Table 30 Precise power-on reset (POR)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes	1.64	–	–	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.4	–	–	V	Guaranteed by characterization

6.6.2 Voltage monitors

Table 31 Voltage monitors DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID195	V_{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	–
SID196	V_{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	–
SID197	V_{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	–
SID198	V_{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	–
SID199	V_{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	–
SID200	V_{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	–
SID201	V_{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	–
SID202	V_{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	–
SID203	V_{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	–
SID204	V_{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	–
SID205	V_{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	–
SID206	V_{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	–
SID207	V_{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	–
SID208	V_{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	–
SID209	V_{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	–
SID210	V_{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	–
SID211	LVI_IDD	Block current	–	–	100	µA	Guaranteed by characterization

Table 32 Voltage monitors AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID212	$T_{MONTRIP}$	Voltage monitor trip time	–	–	1	µs	Guaranteed by characterization

6.6.3 SWD interface

Table 33 SWD interface specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 * T	–	–	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 * T	–	–	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 * T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

6.6.4 Internal main oscillator

Table 34 IMO DC specifications

(Guaranteed by design)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	325	µA	–
SID220	I_{IMO3}	IMO operating current at 12 MHz	–	–	225	µA	–
SID221	I_{IMO4}	IMO operating current at 6 MHz	–	–	180	µA	–
SID222	I_{IMO5}	IMO operating current at 3 MHz	–	–	150	µA	–

Table 35 IMO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID223	$F_{IMOTOL1}$	Frequency variation from 3MHz to 48 MHz	–	–	±2	%	–
SID226	$T_{STARTIMO}$	IMO startup time	–	–	12	µs	–
SID227	$T_{JITRMSIMO1}$	RMS jitter at 3 MHz	–	156	–	ps	–
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	–
SID229	$T_{JITRMSIMO3}$	RMS jitter at 48 MHz	–	139	–	ps	–

6.6.5 Internal low-speed oscillator

Table 36 ILO DC specifications

(Guaranteed by design)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID231	I_{ILO1}	ILO operating current at 32 kHz	–	0.3	1.05	µA	Guaranteed by characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2	15	nA	Guaranteed by design

Table 37 ILO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID237	$F_{ILOTRIM1}$	32 kHz trimmed frequency	15	32	50	kHz	±60% with trim

Table 38 PLL DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID410	IDD_PLL_48	In = 3 MHz, Out = 48 MHz	–	530	610	µA	–
SID411	IDD_PLL_24	In = 3 MHz, Out = 24 MHz	–	300	405	µA	–

Table 39 PLL AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID412	F_{PLLIN}	PLL input frequency	1	–	48	MHz	–
SID413	F_{PLLINT}	PLL intermediate frequency; prescaler out	1	–	3	MHz	–
SID414	F_{PLLVCO}	VCO output frequency before post-divide	22.5	–	104	MHz	–
SID415	D_{IVVCO}	VCO Output post-divider range; PLL output frequency is F_{PPLVCO}/D_{IVVCO}	1	–	8	–	–
SID416	PLLlocktime	Lock time at startup	–	–	250	µs	–
SID417	Jperiod_1	Period jitter for VCO ≥ 67 MHz	–	–	150	ps	Guaranteed By design
SID416A	Jperiod_2	Period jitter for VCO ≤ 67 MHz	–	–	200	ps	Guaranteed By design

Table 40 External clock specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID305	ExtClkFreq	External clock input frequency	0	–	48	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; measured at $V_{DD/2}$	45	–	55	%	Guaranteed by characterization

Table 41 Watch crystal oscillator (WCO) specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
IMO WCO-PLL calibrated mode							
SID330	IMOWCO1	Frequency variation with IMO set to 3 MHz	–0.6	–	0.6	%	Does not include WCO tolerance
SID331	IMOWCO2	Frequency variation with IMO set to 5 MHZ	–0.4	–	0.4	%	Does not include WCO tolerance
SID332	IMOWCO3	Frequency variation with IMO set to 7 or 9 MHZ	–0.3	–	0.3	%	Does not include WCO tolerance
SID333	IMOWCO4	All other IMO frequency settings	–0.2	–	0.2	%	Does not include WCO tolerance
WCO specifications							
SID398	FWCO	Crystal frequency	–	32.768	–	kHz	–
SID399	FTOL	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	–
SID401	PD	Drive Level	–	–	1	µW	–
SID402	TSTART	Startup time	–	–	500	ms	–
SID403	CL	Crystal load capacitance	6	–	12.5	pF	–
SID404	C0	Crystal shunt capacitance	–	1.35	–	pF	–
SID405	IWCO1	Operating current (High power mode)	–	–	8	µA	–

Table 42 External crystal oscillator (ECO) specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID316	IECO1	Block operating current	–	–	1.5	mA	–
SID317	FECO	Crystal frequency range	4	–	33	MHz	–

Table 43 UDB AC specifications

(Guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Datapath performance							
SID249	$F_{MAX-TIMER}$	Max frequency of 16-bit timer in a UDB pair	–	–	48	MHz	–
SID250	$F_{MAX-ADDER}$	Max frequency of 16-bit adder in a UDB pair	–	–	48	MHz	–
SID251	F_{MAX_CRC}	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	48	MHz	–
PLD performance in UDB							–
SID252	F_{MAX_PLD}	Max frequency of 2-pass PLD function in a UDB pair	–	–	48	MHz	–
Clock to output performance							–
SID253	$T_{CLK\_OUT\_UDB1}$	Prop. delay for clock in to data out at 25°C, typ.	–	15	–	ns	–
SID254	$T_{CLK\_OUT\_UDB2}$	Prop. delay for clock in to data out, worst case.	–	25	–	ns	–

Table 44 Block specs

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID256	T_{WS48}[4]	Number of wait states at 48 MHz	2	–	–	–	CPU execution from Flash. Guaranteed by characterization
SID257	T_{WS24}[4]	Number of wait states at 24 MHz	1	–	–	–	CPU execution from Flash. Guaranteed by characterization
SID260	V_{REFSAR}	Trimmed internal reference to SAR	–1	–	+1	%	Percentage of Vbg (1.024 V). Guaranteed by characterization
SID261	$F_{SARINTREF}$	SAR operating speed without external reference bypass	–	500	–	ksps	12-bit resolution. Guaranteed by characterization
SID262	$T_{CLKSWITCH}$	Clock switching from clk1 to clk2 in clk1 periods	3	–	4	Periods	Guaranteed by design

Note
4. Guaranteed by characterization.

Table 45 UDB port adaptor specifications

(Based on LPC component specs; all specs except TLCLKDO are guaranteed by design -10-pF load, 3-V V_{DDIO} and V_{DDD})

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID263	T_{LCLKDO}	LCLK to output delay	–	–	18	ns	
SID264	$T_{DINLCLK}$	Input setup time to LCLCK rising edge	–	–	7	ns	
SID265	$T_{DINLCLKHLD}$	Input hold time from LCLK rising edge	0	–	–	ns	
SID266	$T_{LCLKHIZ}$	LCLK to output tristated	–	–	28	ns	
SID267	T_{FLCLK}	LCLK frequency	–	–	33	MHz	
SID268	$T_{LCLKDUTY}$	LCLK duty cycle (percentage high)	40	–	60	%	

Table 46 USB device block specifications (USB only)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID321	Vusb_5	Device supply for USB operation	4.5	–	5.5	V	USB Configured, USB Reg. enabled
SID322	Vusb_3.3	Device supply for USB operation	3.15	–	3.6	V	USB Configured, USB Reg. bypassed
SID323	Vusb_3	Device supply for USB operation (Functional operation only)	2.85	–	3.6	V	USB Configured, USB Reg. bypassed
SID324	Iusb_config	Device supply current in Active mode, IMO = 24 MHz	–	10	–	mA	V_{DDD} = 5 V
SID325	Iusb_config	Device supply current in Active mode, IMO = 24 MHz	–	8	–	mA	V_{DDD} = 3.3 V
SID326	Isub_suspend	Device supply current in Sleep mode	–	0.5	–	mA	V_{DDD} = 5 V, PICU wakeup
SID327	Isub_suspend	Device supply current in Sleep mode	–	0.3	–	mA	V_{DDD} = 5 V, Device disconnected
SID328	Isub_suspend	Device supply current in Sleep mode	–	0.5	–	mA	V_{DDD} = 3.3 V, PICU wakeup
SID329	Isub_suspend	Device supply current in Sleep mode	–	0.3	–	mA	V_{DDD} = 3.3 V, Device disconnected

Table 47 SIO specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SIO DC specifications							
SID330	V_{IH}	Input voltage high threshold	0.7 * V_{DD}	–	–	V	CMOS input; with respect to V_{DDIO}
SID331	V_{IL}	Input voltage low threshold	–	–	0.3*VDD	V	CMOS input; with respect to V_{DDIO}
SID332	V_{IH}	Differential input mode high voltage; hysteresis disabled	Vr + 0.2	–	–	V	Vr is the SIO reference voltage
SID333	V_{IL}	Differential input mode low voltage, hysteresis disabled	–	–	Vr-0.2	V	Vr is the SIO reference voltage
SID334	V_{OH}	Output high voltage in unregulated mode	V_{DDIO} – 0.4	–	–	V	I_{OH} = 4 mA, V_{DD} = 3.3 V
SID335	V_{OH}	Output high voltage in regulated mode	Vr – 0.65	–	Vr + 0.2	V	I_{OH} = 1 mA
SID336	V_{OH}	Output high voltage in regulated mode	Vr – 0.3	–	Vr + 0.2	V	I_{OH} = 0.1 mA
SID337	V_{OL}	Output low voltage	–	–	0.8	V	V_{DDIO} = 3.3 V, I_{OL} = 25 mA
SID338	V_{OL}	Output low voltage	–	–	0.4	V	V_{DDIO} = 1.8 V, I_{OL} = 4 mA
SID339	Vinref	Input voltage reference	0.48	–	0.52 * V_{DDIO}	V	
SID340	Voutref	Output voltage reference (regulated mode)	1	–	V_{DDIO} – 1	V	V_{DDIO} > 3.3
SID341	Voutref	Output voltage reference (regulated mode)	1	–	V_{DDIO} – 0.5	V	V_{DDIO} < 3.3
SID342	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID343	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID344	I_{IL}	Input leakage current (absolute value)	–	–	14	nA	$V_{IH} \le V_{DDSIO}$; 25°C
SID345	I_{IL}	Input leakage current (absolute value)	–	–	10	nA	$V_{IH} > V_{DDSIO}$; 25°C
SID346	C_{IN}	Input capacitance	–	–	7	pF	–
SID347	VHYST-Single	Hysteresis in single-ended mode	–	40	–	mV	–
SID348	VHYST_Diff	Hysteresis in differential mode	–	35	–	mV	–
SID349	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
SIO AC specifications (Guaranteed by design)							
SID350	T_{RISEF}	Rise time in Fast Strong mode	–	–	12	ns	3.3-V V_{DD}, Cload = 25 pF
SID351	T_{FALLF}	Fall time in Fast Strong mode	–	–	12	ns	3.3-V V_{DD}, Cload = 25 pF
SID352	T_{RISES}	Rise time in Slow Strong mode	–	–	75	ns	3.3-V V_{DD}, Cload = 25 pF

Table 47 SIO specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID353	T_{FALLS}	Fall time in Slow Strong mode	–	–	70	ns	3.3-V V_{DD}, Cload = 25 pF
SID354	F_{SIOUT1}	SIO Fout; Unregulated, Fast Strong mode	–	–	33	MHz	3.3-V ≤ V_{DD} ≤ 5.5 V, 25 pF. Guaranteed by design
SID355	F_{SIOUT2}	SIO Fout; Unregulated, Fast Strong mode	–	–	16	MHz	1.71-V ≤ V_{DD} ≤ 3.3 V, 25 pF
SID356	F_{SIOUT3}	SIO Fout; Regulated, Fast Strong mode	–	–	20	MHz	3.3-V ≤ V_{DD} ≤ 5.5 V, 25 pF
SID357	F_{SIOUT4}	SIO Fout; Regulated, Fast Strong mode	–	–	10	MHz	1.71 V ≤ V_{DD} ≤ 3.3 V, 25 pF
SID358	F_{SIOUT3}	SIO Fout; Unregulated, Slow Strong mode.	–	–	5	MHz	3.3 V ≤ V_{DD} ≤ 5.5 V, 25 pF
SID359	F_{SIOUT4}	SIO Fout, Unregulated, Slow Strong mode.	–	–	3.5	MHz	1.71 V ≤ V_{DD} ≤ 3.3 V, 25 pF
SID360	F_{SIOUT5}	SIO Fout, Regulated, Slow Strong mode.	–	–	2.5	MHz	1.7 V ≤ V_{DD} ≤ 5.5 V, 25 pF
SID361	F_{GPIOIN}	GPIO input operating frequency;1.71 V ≤ V_{DD} ≤ 5.5 V	–	–	48	MHz	1.71 V ≤ V_{DD} ≤ 5.5 V

Table 48 CAN specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / conditions
SID420	IDD_CAN	Block current consumption	–	–	200	µA	–
SID421	CAN_bits	CAN Bit rate (Min 8-MHz clock)	–	–	1	Mbps	–

7 Ordering information

The PSoC™ 4200L family part numbers and features are listed in the following table.

Table 49 PSoC™ 4200L ordering information

Category	Product	Features														Package
		Max CPU speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Op-amp (CTBm)	CSD	Direct LCD drive	12-bit SAR ADC	LP comparators	TCPWM blocks	SCB blocks	USB Full-Speed	CAN	GPIO	124-VFBGA
4248	CY8C4248BZA-L489	48	256	32	8	4	2	Yes	1000 ksps	2	8	4	Yes	Yes	98	Yes
	CY8C4248BZS-L489	48	256	32	8	4	2	Yes	1000 ksps	2	8	4	Yes	Yes	98	Yes

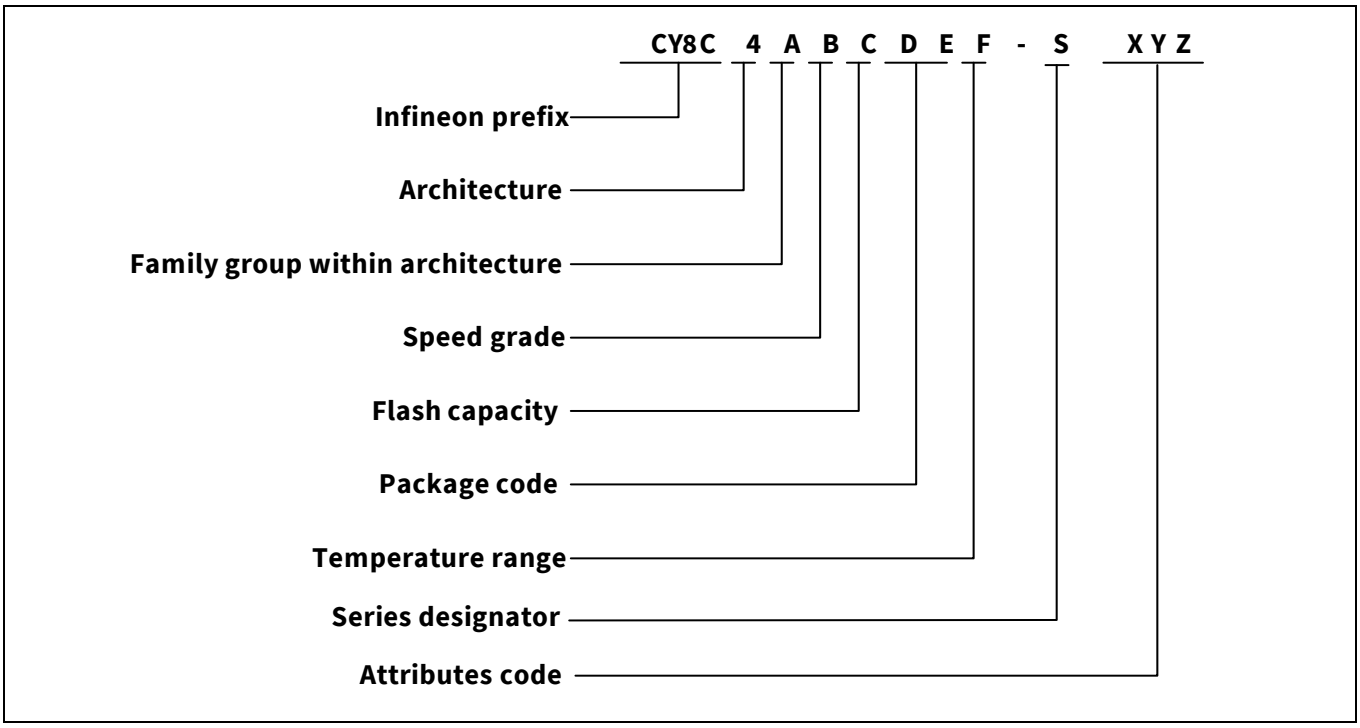
The nomenclature used in **Table 49** is based on the following part numbering convention:

Table 50 MPN nomenclature

Field	Description	Value	Meaning
CY8C	Infineon prefix		–
4	Architecture	4	PSoC™ 4
A	Family	2	4200 family
B	CPU speed	4	48 MHz
C	Flash capacity	6	64 KB
		7	128 KB
		8	256 KB
DE	Package code	AX, AZ	TQFP
		LT	QFN
		BZ	BGA
		FD	CSP
F	Temperature range	A	AUTO A (–40°C to +85°C)
		S	AUTO S (–40°C to +105°C)
S	Series designator	S	PSoC™ 4 S-series
		L	PSoC™ 4 L-series
		M	PSoC™ 4 M-series
XYZ	Attributes code	000-999	Code of feature set in the specific family

7.1 Part numbering conventions

The part number fields are defined as follows.



8 Packaging

Table 51 Package dimensions

SPEC ID#	Package	Description	Package DWG #
PKG_1	124-ball VFBGA	124-ball, 9 mm x 9 mm x 1.0 mm height with 0.65 mm ball pitch	001-97718

Table 52 Package characteristics

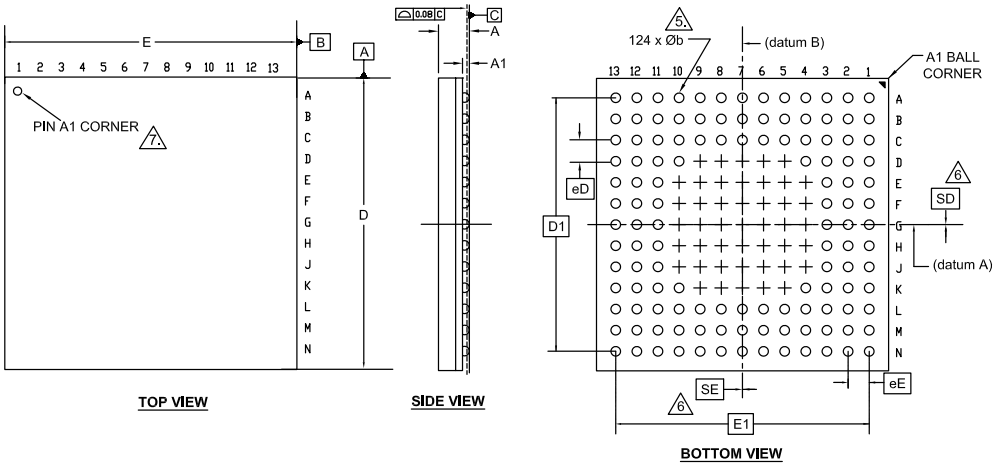
Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature (CY8C4248BZS - L489)	–	–40	25	105	°C
	Operating ambient temperature (CY8C4248BZA-L489)	–	–40	25	85	°C
T_J	Operating junction temperature	–	–40	–	125	°C
T_{JA}	Package θ_{JA} (124-ball VFBGA)	–	–	85	–	°C/watt
T_{JC}	Package θ_{JC} (124-ball VFBGA)	–	–	6	–	°C/watt

Table 53 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time at peak temperature
124-ball VFBGA	260°C	30 seconds

Table 54 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
124-ball VFBGA	MSL 3



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	0.21	0.26
D	8.90	9.00	9.10
E	8.90	9.00	9.10
D1	7.80 BSC		
E1	7.80 BSC		
MD	13		
ME	13		
N	124		
Ø b	0.25	0.30	0.35
eD	0.65 BSC		
eE	0.65 BSC		
SD	0		
SE	0		

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MO-280.

001-97718 *B

Figure 8 Package outline, 124 -ball VFBGA 9.0 × 9.0 × 1.0 mm BZ0AA/VZC124/D2A124 (PG-VFBGA-124)

9 Acronyms

Table 55 Acronyms used in this document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	Central Processing Unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	Do Not Use
DR	Port Write Data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	Execution Program Status register
ESD	electrostatic discharge
ETM	embedded trace macrocell

Table 55 Acronyms used in this document *(continued)*

Acronym	Description
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	Full-Speed
GPIO	general-purpose input/output, applies to a PSoC™ pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	Link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier

Table 55 Acronyms used in this document *(continued)*

Acronym	Description
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC™	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion

Table 55 Acronyms used in this document *(continued)*

Acronym	Description
TIA	transimpedance amplifier
RM	reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC™ pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

10 Document conventions

10.1 Units of measure

Table 56 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
W	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

11 Errata

1. CTBM offset shift due to floating inputs	
Problem definition	CTBm opamp inputs require bias when opamp is powered down.
Parameters affected	SID288 (V_{OS_TR}) – Offset voltage, trimmed.
Trigger condition(s)	Leaving the CTBm opamp powered down with floating inputs for long periods of time will result in offset voltage shifting Out-of-Specification (OOS).
Scope of impact	Only impacts CTBm opamp.
Workaround	If the opamp is powered down during chip operation, it should be configured in opamp mode, with V_{pos} & V_{neg} inputs connected to GPIOs configured in Open Drain (Pull-down OFF, Strong pull-up, Input Buffer ON) mode.
Fix status	Will not fix, use workaround.

Revision history

Document revision	Date	Description of changes
*B	2023-11-20	Public release.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2023-11-20
Published by

Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Email:
erratum@infineon.com

Document reference
002-35633 Rev. *B

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.