Recent Additions
CD54AC649/3A
CD54ACT649/3A

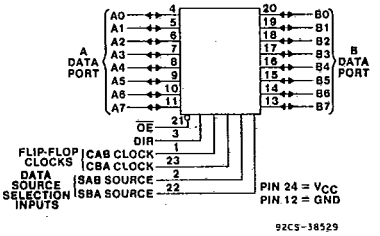
T-52-31

Octal-Bus Transceiver/Register, with Open Drain

Inverting

The RCA CD54AC649 and CD54ACT649 are open-drain, octal-bus transceivers/registers that utilize the new RCA ADVANCED CMOS LOGIC technology. The CD54AC649 and CD54ACT649 have inverting outputs. These devices are bus transceivers with D-type flip-flops which act as internal storage registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Output Enable ($\overline{OE}$) and Direction (DIR) inputs control the transceiver functions. Data present at the high-impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The Select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The Direction control determines which data bus will receive data when the Output Enable ($\overline{OE}$) is LOW. In the high-impedance mode (Output Enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the Direction (DIR) and Output Enable ($\overline{OE}$) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

The CD54AC649 and CD54ACT649 are supplied in 24-lead dual-in-line ceramic packages (F suffix).



FUNCTIONAL DIAGRAM

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Package Specifications
(See Section 11, Fig. 15)

Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
					+25		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	
Quiescent Supply Current (MSI)	I_{CC}	V_{CC} or GND	0	5.5	—	8•	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
DIR	0.67
$\overline{OE}$	1.17
An, Bn	0.4

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Recent Additions
CD54AC649/3A
CD54ACT649/3A

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: Store $\overline{A}$ Data to B Bus Store $\overline{B}$ Data to A Bus	t_{PZL}	1.5 3.3* 5†	— 4 2.7	194 23.3 15.5•	ns
	t_{PLZ}	1.5 3.3 5	— 4.7 3.2	232 23.1 18.5•	ns
$\overline{A}$ Data to B Bus $\overline{B}$ Data to A Bus	t_{PZL}	1.5 3.3 5	— 3.7 2.4	178 23 14.2•	ns
	t_{PLZ}	1.5 3.3 5	— 4.4 3	215 21.5 17.2•	ns
Select to Data	t_{PZL}	1.5 3.3 5	— 4 2.7	194 23.3 15.5•	ns
	t_{PLZ}	1.5 3.3 5	— 4.7 3.2	232 23.1 18.5•	ns
Enable, Disable Times Bus to Output or Register to Output	t_{PZL} t_{PLZ}	1.5 3.3 5	— 4 2.7	194 23.3 15.5•	ns
Power Dissipation Capacitance	C_{PD}§	—			pF
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1 Typ. @ 25°C		V
Input Capacitance	C_I	—	—	10	pF
Off-State Output Capacitance	C_O	—	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
For AC, $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

(Limits with black dots (•) are tested 100%.)

Recent Additions
CD54AC649/3A
CD54ACT649/3A

T-52-31

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: Store $\overline{A}$ Data to B Bus, Store $\overline{B}$ Data to A Bus	t_{PZL}	5†	2.7	15.5•	ns
	t_{PLZ}	5	3.2	18.5•	ns
$\overline{A}$ Data to B Bus, $\overline{B}$ Data to A Bus	t_{PZL}	5	2.4	14.2•	ns
	t_{PLZ}	5	3	17.2•	ns
Select to Data	t_{PZL}	5	2.7	15.5•	ns
	t_{PLZ}	5	3.2	18.5	ns
Enabe, Disable Times Bus to Output or Register to Output	t_{PZL}, t_{PLZ}	5	2.7	15.5•	ns
Power Dissipation Capacitance	C_{PD}§	—			pF
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1 Typ. @ 25°C		V
Input Capacitance	C_I	—	—	10	pF
Off-State Output Capacitance	C_O	—	—	15	pF

†5 V: min. is @ 5.5 V, max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
For ACT, $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage

(Limits with black dots (•) are tested 100%.)

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