M-969 Pulse Dialer

The Teltone® M-969 is a binary-input pulse dialer IC with many enhancements useful for tone-to-pulse conversion. The IC contains a 16 digit FIFO (first-in-first-out) buffer and controls outpulsing at pin 8 (SZ) at 10 pulses per second with interdigit times of 700 milliseconds.

The dialer IC is enabled by a logic low at pin 12 (ANSW) and a logic high at pin 11 (LC) that has persisted at least 20 milliseconds before entering data. For proper outpulsing operation, digits should be entered within 2 seconds of each other and under any circumstances within 16 seconds of the previous digit to prevent time-out.

Digits are entered by placing the binary code corresponding to the desired digit at pins 3 through 6 (D3-D0) and latching with a high-to-low transition on pin 18 (STROBE).

Special functions are included to control line splitting, enabling an optional DTMF receiver, or monitoring reverse loop current. These functions are detailed in Table 1.

Applications

- Automatic dialers
- Tone-to-pulse dial converters
- Mobile telephone systems
- Alarm systems

Features

- 10 PPS dial pulse output from binary input
- 16 digit buffer
- Compatible with the M-957 DTMF receiver
- 20-pin plastic DIP
- Special I/O features for digit conversion (tone to pulse)
- Accurate time base derived from color burst crystal
- Single 5-volt supply

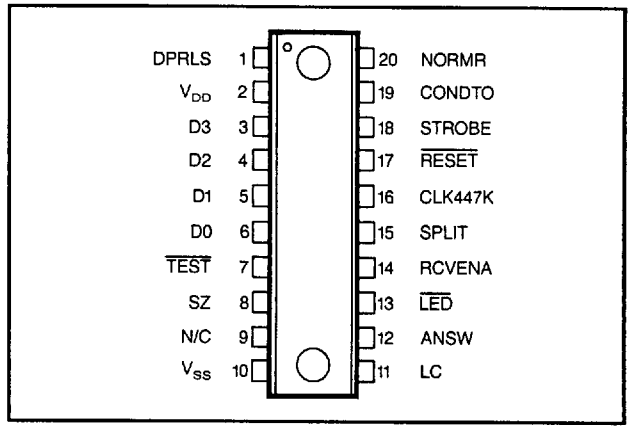

Figure 1 Pin Diagram

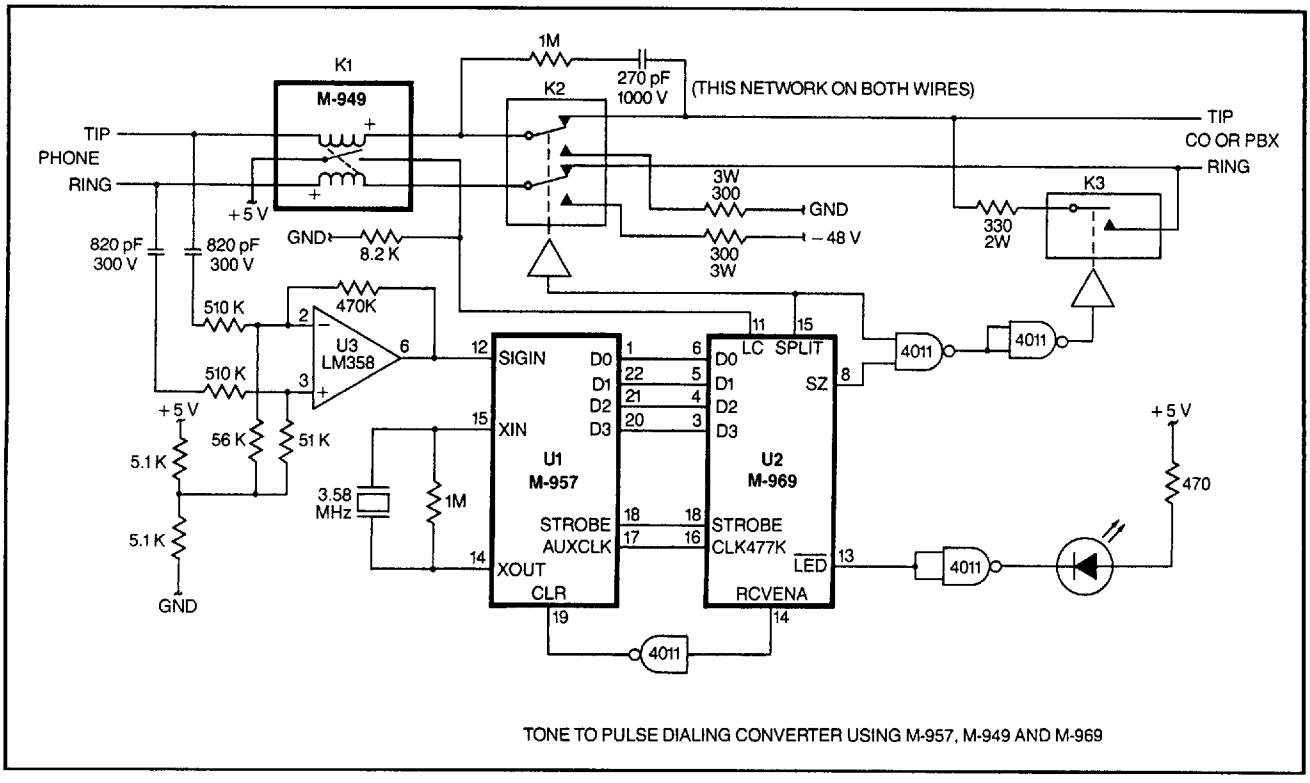

Figure 2 Typical Application

Table 1 Pin Functions

PIN	FUNCTION
DPRLS	The dial pulse release function is enabled when DPRLS is at a logic 1 and LC has been at a logic 1 for 3 seconds. When enabled, a logic 0 at LC for at least 30 ms (a dial pulse) will inhibit the M-969. The IC is re-enabled when new data has been received.
V_{DD}	Most positive power supply input pin.
D3	Data 3 input pin (see Table 2).
D2	Data 2 input pin (see Table 2).
D1	Data 1 input pin (see Table 2).
D0	Data 0 input pin (see Table 2).
$\overline{TEST}$	Factory test input pin (must be tied high for normal operation).
SZ	SEIZE is an output pin intended to drive a pulsing circuit. A logic 1 shall be interpreted as a make condition (pulsing circuit on). The outpulsing rate is 10 pps.
V_{SS}	Most negative power supply input pin.
LC	Loop current sense input pin driven by external circuitry. A logic 1 for at least 20 ms will enable the dialer (off-hook recognition). With DPRLS at logic 0 the dialer will be inhibited when a logic 0 of 200 ms persists at LC (on-hook recognition).
ANSW	A logic 1 at this input for 200 ms will inhibit any further outpulsing or digit entries. This input is intended to be driven from reverse loop current sense circuitry (optional). If reverse loop sensing is not used this pin should be tied to logic 0.
$\overline{LED}$	Dialer status monitor output. In the on-hook condition (idle) $\overline{LED}$ is at a logic 1. In the off-hook condition (enabled) $\overline{LED}$ is at logic 0. When the dialer is outpulsing $\overline{LED}$ goes to a logic 1 for each break pulse (SZ to logic 0). When the dialer chip is in the inhibited state, $\overline{LED}$ oscillates at 20 Hz.
RCVENA	Receiver enable output can be used to enable or disable a companion DTMF receiver. RCVENA will go to a logic 1 after 90 ms of logic 1 at LC and will return to a logic 0 under the following conditions: a. time-out elapsed b. Answer supervision c. on-hook d. dial pulse release e. '#', '*' release
SPLIT	Output pin intended to drive line split circuitry. At recognition of a falling edge of STROBE, the SPLIT pin will go to a logic 1 (line split) and remains high until all digits have been outpulsed.
CLK477K	Clock input pin requires externally generated 447.443 kHz (3.58 MHz/8).
$\overline{RESET}$	Reset input will clear and reinitialize the dialer when a logic 0 is applied for at least 55 microseconds.
STROBE	Data inputs D3-D0 are latched within 4 ms of the falling edge of the STROBE input.
CONDTO	A logic 0 at this pin selects normal time-out operation (time-out begins at off-hook recognition). A logic 1 at this pin selects conditional time-out operation (time-out begins when the most recently received digit has been outpulsed). In both normal and conditional time-out the timer is reset with the receipt of a new digit entry.
NORMR	If NORMR is at a logic 1 and all digits have been outpulsed, SPLIT will go to logic 0 following the last break pulse of the last digit by 700 ms. If NORMR is at a logic 0, SPLIT will return to logic 0 40 ms after the last break pulse of the last digit has been outpulsed.

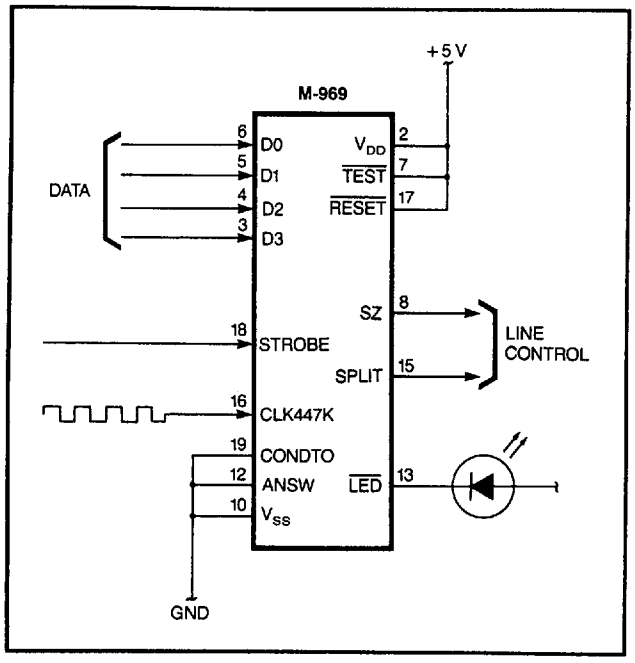

Figure 3 M-969 Typical Connections

Table 2 Data Input

D3	D2	D1	D0	USE
0	0	0	0	IGNORED
0	0	0	1	DIGIT 1
0	0	1	0	DIGIT 2
0	0	1	1	DIGIT 3
0	1	0	0	DIGIT 4
0	1	0	1	DIGIT 5
0	1	1	0	DIGIT 6
0	1	1	1	DIGIT 7
1	0	0	0	DIGIT 8
1	0	0	1	DIGIT 9
1	0	1	0	DIGIT 0
1	0	1	1	RELEASE
1	1	0	0	RELEASE
1	1	0	1	IGNORED
1	1	1	0	IGNORED
1	1	1	1	IGNORED

Table 3 Absolute Maximum Ratings (Note 1)

Voltage at Any Pin Relative to GND	−0.5 to +10 V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C
Power Dissipation	0.65 Watt at 25°C, 0.3 Watt at 70°C
Total Source Current	120 mA
Total Sink Current	100 mA

NOTES:

1. Exceeding these ratings may permanently damage the M-969.
2. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

Table 4 Specifications

	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Operating	Voltage V_{CC}	—	4.5	—	9.5	VDC	
	Supply Current	—		—	5	mA	1
	Temperature	—	0	—	70	Deg. C	
External Clock	Duty-cycle	—	30	—	60	%	
	Rise time	—	—	—	0.5	µs	
	Fall time	—	—	—	0.2	µs	
Input Levels	CLK477K logic 1	—	0.7 V_{CC}	—	V_{CC}		
	CLK477K logic 0	—	0	—	0.6	V	
	$\overline{\text{RESET}}$ logic 1	—	0.7 V_{CC}	—	V_{CC}		
	$\overline{\text{RESET}}$ logic 0	—	0	—	0.6	V	
	$\overline{\text{TEST}}$ logic 1	—	0.7 V_{CC}	—	V_{CC}		
	$\overline{\text{TEST}}$ logic 0	—	0	—	2.0	V	
	All other inputs logic 1	—	2.0	—	V_{CC}	V	
	All other inputs logic 0	—	0	—	0.8	V	
Output Sink Current	$\overline{\text{LED}}$	—	1.0	—	4.5	mA	2
	SPLIT, RCVENA	—	7.5	—	35	mA	2
	SZ	—	2.2	—	11	mA	2
Output Source Current	$\overline{\text{LED}}$, SPLIT, RCVENA	—	−26	—	−190	µA	3
	SZ	—	−0.07	—	−2.8	mA	3
Data Input	Data Setup Time (tDS)	—	8	—	—	µs	
	Data Hold Time (tDH)	—	8	—	—	ms	
Hookswitch Status	On-hook recognition	—	150	—	200	ms	4
	Off-hook recognition	—	10	—	20	ms	
	Dial pulse release enabled	—	2	—	3	sec.	
	Dial pulse recognition	—	15	—	30	ms	
Pulsing	Pause for first break pulse	—	39	—	41	ms	5
	Make duration	—	39	—	41	ms	
	Break duration	—	59	—	61	ms	
	Pulses per second	—	9.8	—	10.2	pps	
	Interdigital time	—	710	—	770	ms	
Line Split	STROBE low to SPLIT high	—	.04	—	4	ms	
	SPLIT high to SZ high	—	30	—	40	ms	
Reverse Loop	Answer recognition	—	150	—	200	ms	6
Line Restore	Last break to SPLIT low	—	670	—	730	ms	NORMR= 1
	Last break to SPLIT low	—	39	—	41	ms	NORMR= 0
	SPLIT low to SZ low	—	16	—	19	ms	NORMR= 1
	LC low to SZ low	—	150	—	200	ms	
Time Out	From off-hook recognition	—	15	—	17	sec.	
	From most recently received digit	—	15	—	17	sec.	CONDTO= 1

Notes

1. V_{CC} = 5 V, TA = 25°C, with all inputs and outputs open.
2. V_{CC} = 4.5 V, V_O = 1.0 V.
3. V_{CC} = 4.5 V, V_O = 2.25 V.
4. The hookswitch status is monitored through the LC input pin. A logic 1 denotes off-hook, a logic 0 denotes on-hook or a break pulse.
5. For pause before first break, make, and interdigital periods SZ output will be at logic 1. For break period SZ output will be at logic 0.
6. Answer supervision is monitored through the ANSW input pin. A logic 1 denotes answer.

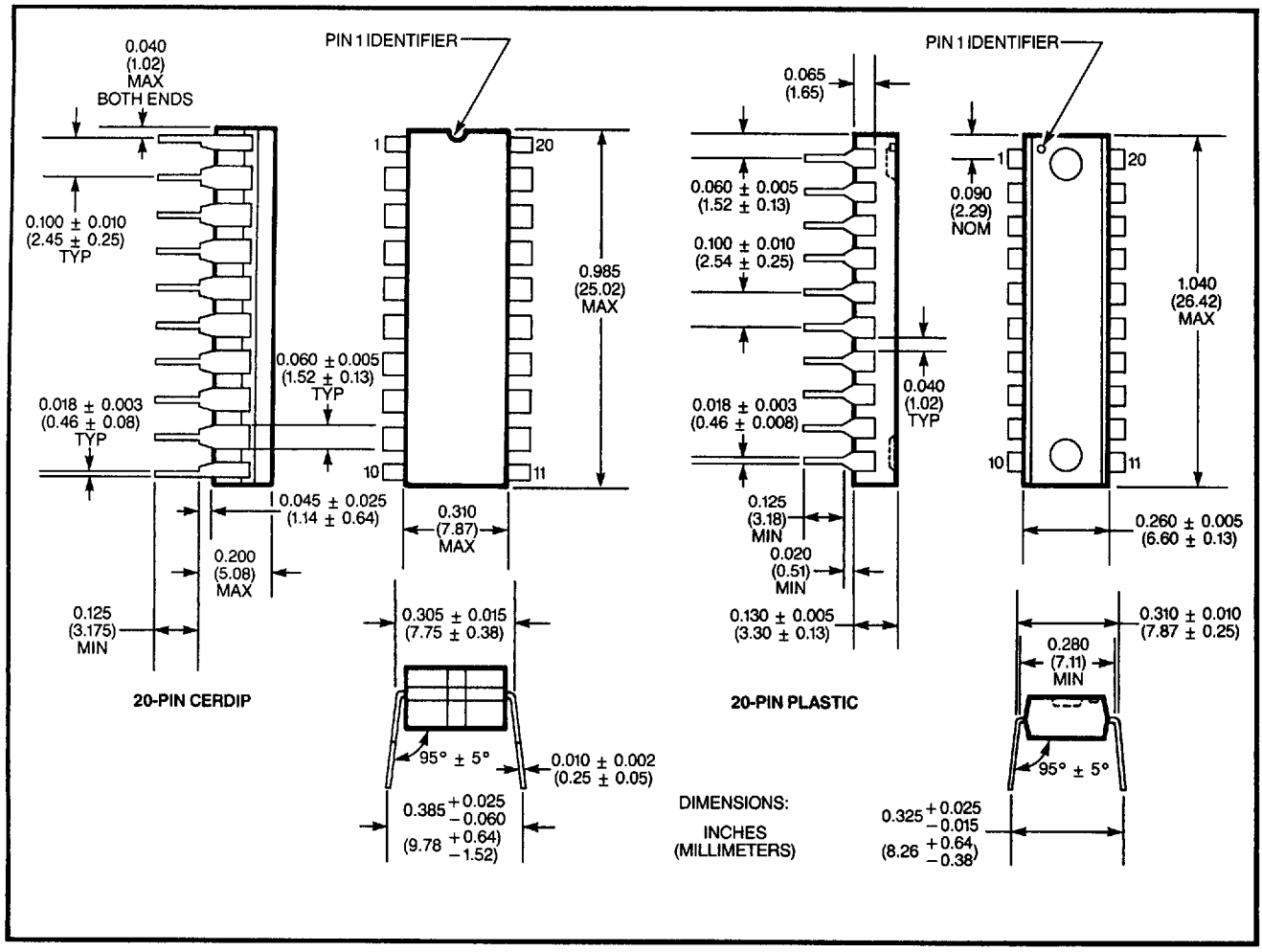

Figure 4 Package Dimensions