MP87L95

Low Voltage CMOS
Very Low Power 10-Bit
Analog-to-Digital Converter

EXAR

FEATURES

- 3.3 V Operation
- 10-Bit Resolution
- Sampling Rates from <1 kHz to 500 kHz
- DNL better than 1/2 LSB (typ) up to 250 kHz
- Very Low Power CMOS - 5 mW (typ)
- Power Down; Lower Consumption – 1 mW (typ)
- Interface to any Input Range between GND and V_{DD}
- No S/H Required for CCD Signals less than 250 kHz
- Latch-Up Free
- ESD Protection: 2000 Volts Minimum
- Monotonic. No Missing Codes
- For new design, use XRD64L15AIP and XRD64L15AID

BENEFITS

- Reliable Operation
- Reduced Board Space (Small Package)
- Reduced External Parts, No Sample/Hold Needed
- Suitable for Battery & Power Critical Applications
- Designer Can Adapt Input Range & Scaling

APPLICATIONS

- µP/DSP Interface and Control Applications
- High Resolution Imaging – Scanners, Copiers, Facsimile
- Multiplexed Data Acquisition
- Radar Pulse Analysis
- Low Power A/D Applications

5

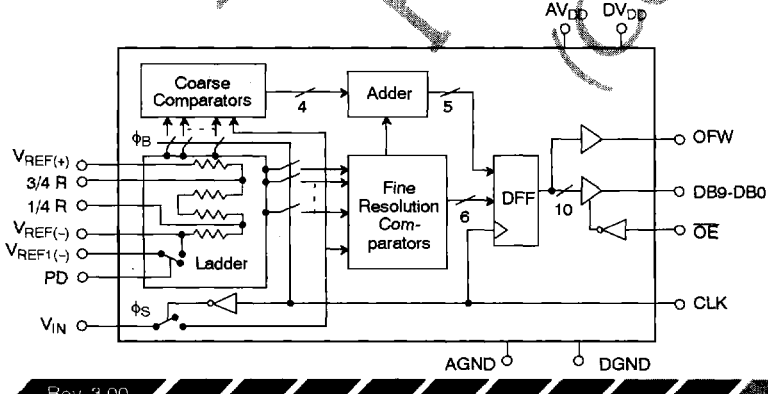
GENERAL DESCRIPTION58

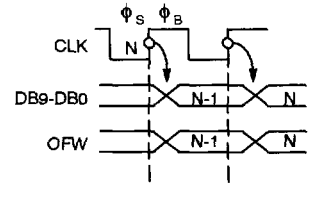
The MP87L95 is a flexible, easy to use, precision 10-bit Analog-to-Digital Converter that operates over a wide range of input and sampling conditions. The MP87L95 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 250 kHz. The elimination of the S/H and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications, up to 250 kHz, or multiplexed input applications when the signal source bandwidth is limited to 20 kHz. The input architecture of the MP87L95 allows direct interface to any analog input range between AGND and AV_{DD} (0 to 2 V, 3 V). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range. Scaled reference resistor taps 1/4 R and 3/4 R allow for customizing the transfer curve. Digital outputs offer 3-state operation.

The MP87L95 uses a two-step flash technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

When the power down input is "high", the data outputs DB9 to DB0 hold the current values and $V_{REF(-)}$ is disconnected from $V_{REF1(-)}$. The power consumption during the power down mode is approximately 1mW.

SIMPLIFIED BLOCK AND TIMING DIAGRAM



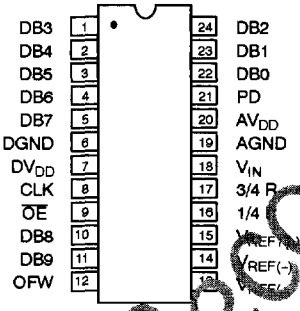


ORDERING INFORMATION

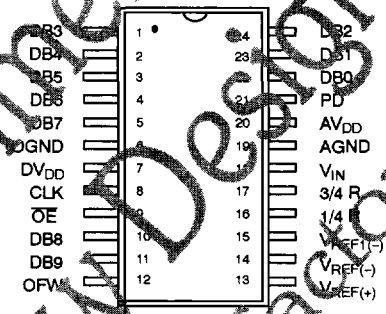
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	-40 to +85°C	MP87L95AN	±1	±2
SOIC	-40 to +85°C	MP87L95AS	±1	±2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")



24 Pin SOIC (Jedec, 0.300")

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB3	Data Output Bit 3
2	DB4	Data Output Bit 4
3	DB5	Data Output Bit 5
4	DB6	Data Output Bit 6
5	DB7	Data Output Bit 7
6	DGND	Digital Ground
7	DV_{DD}	Digital V_{DD}
8	CLK	Clock Input
9	$\overline{OE}$	Output Enable (Active Low)
10	DB8	Data Output Bit 8
11	DB9	Data Output Bit 9 (MSB)
12	OFW	Overflow Output

PIN NO.	NAME	DESCRIPTION
13	$V_{REF(+)}$	Upper Reference Voltage
14	$V_{REF(-)}$	Lower Reference Voltage
15	$V_{REF1(-)}$	Lower Reference Voltage
16	1/4 R	Reference Ladder Tap @ 1/4 FS
17	3/4 R	Reference Ladder Tap @ 3/4 FS
18	V_{IN}	Analog Signal Input
19	AGND	Analog Ground
20	AV_{DD}	Analog V_{DD}
21	PD	Power Down
22	DB0	Data Output Bit 0 (LSB)
23	DB1	Data Output Bit 1
24	DB2	Data Output Bit 2