54F/74F401

CRC Generator/Checker

PRELIMINARY

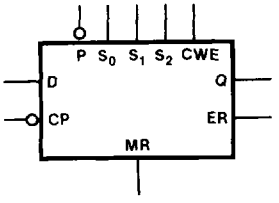
Description

The 'F401 Cyclic Redundancy Check (CRC) Generator/Checker provides an advanced tool for implementing the most widely used error detection scheme in several digital data handling systems. A 3-bit control input selects one-of-eight generator polynomials. The list of polynomials includes CRC-16 and CRC-CCITT, as well as their reciprocals (reverse polynomials). Automatic right justification is incorporated for polynomials of degree less than 16. Separate clearing/presetting inputs are provided for floppy disk and other applications. The Error output indicates whether or not a transmission error has occurred. A single control input inhibits feedback during check word transmission. The 'F401 is fully compatible with all TTL families.

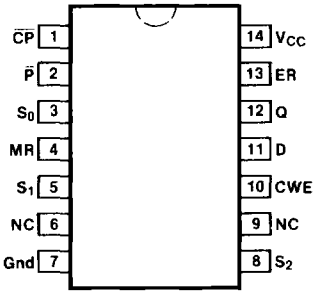
- **Eight Selectable Polynomials**
- **Error Indicator**
- **Separate Preset and Clear Controls**
- **Automatic Right Justification**
- **Fully Compatible with all TTL Logic Families**
- **14-Pin Package**
- **9401 Equivalent**
- **Typical Applications:**
  - **Floppy and Other Disk Storage Systems**
  - ***Digital Cassette and Cartridge Systems***
  - **Data Communication Systems**

Ordering Code: See Section 5

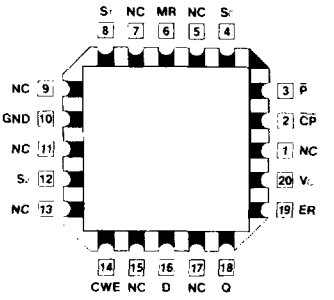
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

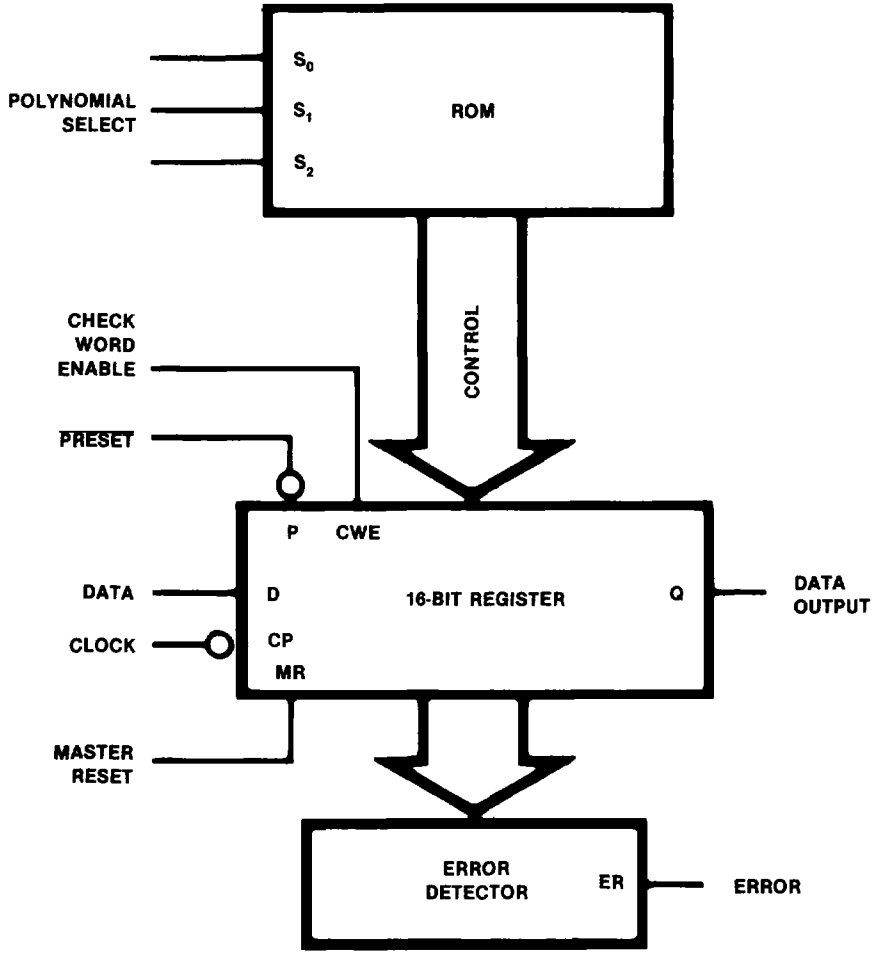


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
S_0-S_2	Polynomial Select Inputs	0.5/0.375
D	Data Input	0.5/0.375
$\overline{CP}$	Clock Input (Operates on HIGH-to-LOW Transition)	0.5/0.375
CWE	Check Word Enable Input	0.5/0.375
$\overline{P}$	Preset (Active LOW) Input	0.5/0.375
MR	Master Reset (Active HIGH) Input	0.5/0.375
Q	Data Output	25/12.5
ER	Error Output	25/12.5

Block Diagram



Functional Description

The 'F401 is a 16-bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. The 'F401 implements the polynomials listed in Table 1 by applying the appropriate logic levels to the select pins S_0, S_1 and S_2.

The 'F401 consists of a 16-bit register, a Read Only Memory (ROM) and associated control circuitry as shown in the block diagram. The polynomial control code presented at inputs S_0, S_1 and S_2 is decoded by the ROM, selecting the desired polynomial by establishing shift mode operation on the register with Exclusive OR gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data inputs (D), using the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). This data is gated with the most significant output (Q) of the register, and controls the Exclusive OR gates (Figure 1). The Check Word Enable (CWE) must be held HIGH while the data is being entered. After the last data bit is entered, the CWE is brought LOW and the check bits are shifted out of the register and appended to the data bits using external gating (Figure 2).

To check an incoming message for errors, both the data and check bits are entered through the D input with the CWE input held HIGH. The 'F401 is not in the data path, but only monitors the message. The Error Output becomes valid after the last check bit has been entered into the 'F401 by a HIGH-to-LOW transition of $\overline{CP}$. If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error Output (ER) is LOW. If a detectable error has occurred, ER is HIGH.

A HIGH on the Master Reset input (MR) asynchronously clears the register. A LOW on the Preset input ($\overline{P}$) asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of 12 or 8-bit check polynomials only the most significant 12 or 8 register bits are set and the remaining bits are cleared.

Table 1

Select Code			Polynomial	Remarks
S_2	S_1	S_0		
L	L	L	$X^{16}+X^{15}+X^2+1$	CRC-16
L	L	H	$X^{16}+X^{14}+X+1$	CRC-16 REVERSE
L	H	L	$X^{16}+X^{15}+X^{13}+X^7+X^4+X^2+X^1+1$	
L	H	H	$X^{12}+X^{11}+X^3+X^2+X+1$	CRC-12
H	L	L	$X^8+X^7+X^5+X^4+X+1$	
H	L	H	X^8+1	LRC-8
H	H	L	$X^{16}+X^{12}+X^5+1$	CRC-CCITT
H	H	H	$X^{16}+X^{11}+X^4+1$	CRC-CCITT REVERSE

Fig. 1 Equivalent Circuit for $X^{16} + X^{15} + X^2 + 1$

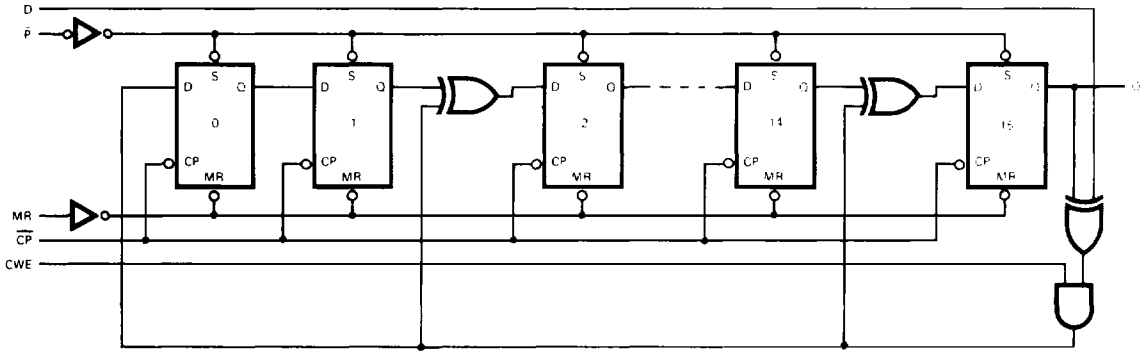
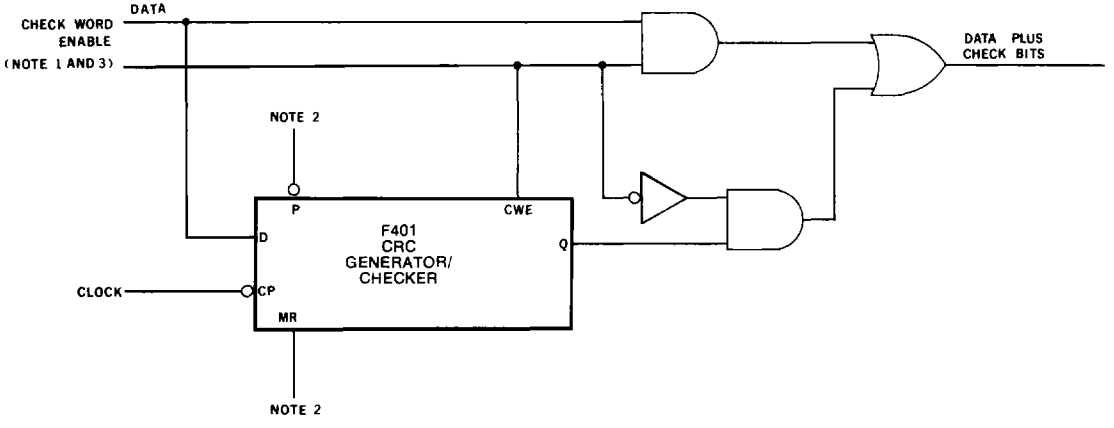


Fig. 2 Check Word Generation



NOTES:
1. Check word Enable is HIGH while data is being clocked, LOW while transmission of check bits.
2. 'F401 must be reset or preset before each computation.
3. CRC check bits are generated and appended to data bits.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		70	110	mA	V_{CC} = Max, Inputs Open

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	70							MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q		15.0 15.0						ns	3-1 3-8
t_{PHL}	Propagation Delay MR to Q		11.0						ns	3-1 3-11
t_{PLH}	Propagation Delay $\overline{P}$ to ER		12.0						ns	3-1 3-11
t_{PLH}	Propagation Delay $\overline{P}$ to Q		12.0						ns	3-1 3-11
t_{PHL}	Propagation Delay MR to ER		15.0						ns	3-1 3-11
t_{PLH}	Propagation Delay $\overline{P}$ to ER		15.0						ns	3-1 3-11
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to ER		15.0 15.0						ns	3-1 3-8

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW D to $\overline{CP}$	5.0 5.0			ns	3-6
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW CWE to $\overline{CP}$	5.0 5.0				
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D and CWE to $\overline{CP}$	0 0				
$t_w(L)$	$\overline{P}$ Pulse Width, LOW	9.0			ns	3-9
$t_w(L)$	Clock Pulse Width, LOW	10.0			ns	3-8
$t_w(H)$	MR Pulse Width, HIGH	9.0			ns	3-11
t_{rec}	Recovery Time MR to $\overline{CP}$	10.0			ns	3-11
t_{rec}	Recovery Time $\overline{P}$ to $\overline{CP}$	10.0			ns	3-11