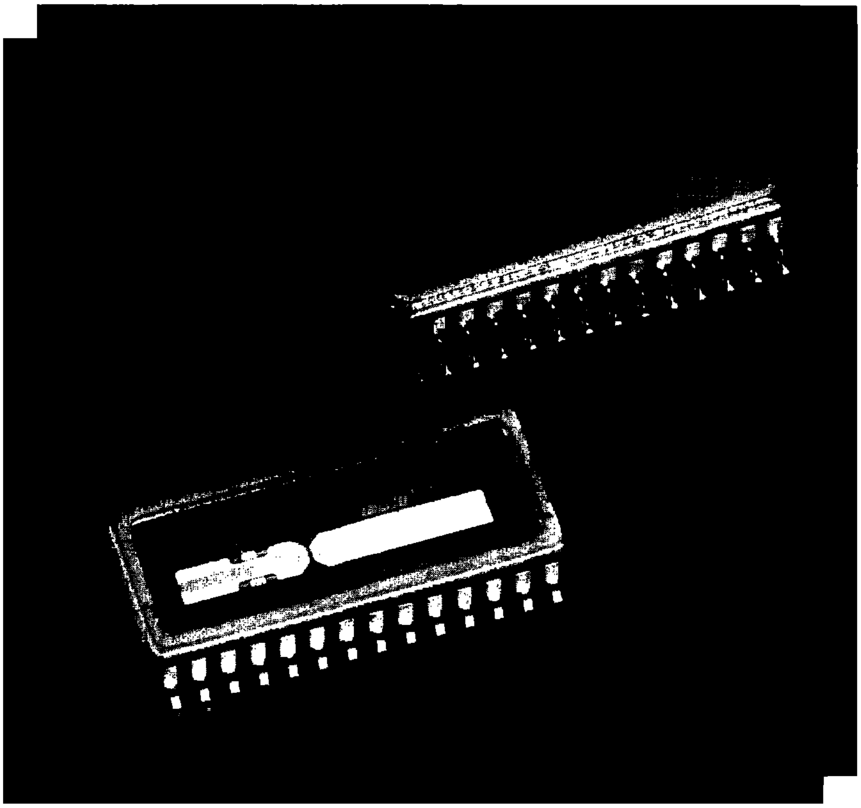
TRU600

Clock Recovery and Data Retiming Module



TRU600 Clock Recovery and Data Retiming Module.

Features

- Output jitter typically 10 ps RMS
- Low-cost modular solution
- Choice of data rates from 124.416 Mb/s to 622.08 Mb/s
- SONET/SDH compatible
- 100K ECL/PECL compatible inputs and outputs
- Single supply voltage
- Low power consumption
- Quartz SAW filter technology
- Miniature hermetically sealed ceramic surface-mount package (S0-28, approx. 0.7 in. x 0.3 in.)
- External Clock Enable for LOS

Description

The TRU600A module is used to generate data and clock signals from nonreturn-to-zero (NRZ) digital data streams, such as those encountered in fiber-optic data links and telecommunications applications. The module features a high-speed bipolar integrated circuit and a quartz filter in a hermetically sealed, 28-lead, ceramic package. To extract a clock signal from the input data, the data is first passed through a frequency doubler (see Figure 1). This generates pulses containing significant spectral energy at the input data rate. A precision narrow-band filter, centered at the clock frequency, substantially suppresses jitter by rejecting other frequencies. The extracted clock signal is then accurately aligned with the incoming data signal at the input of a decision circuit. This circuit retimes the data. The output data and clock signals are thus free of undesirable jitter and distortion. Unlike phase-locked loop designs, the jitter transfer function of the TRU600A is stable because it is controlled by the shape of the bandpass filter.

In addition to producing outputs with very low jitter, the TRU600A has excellent stability, fast acquisition time, and robust operation over specified operating conditions.

Description (continued)

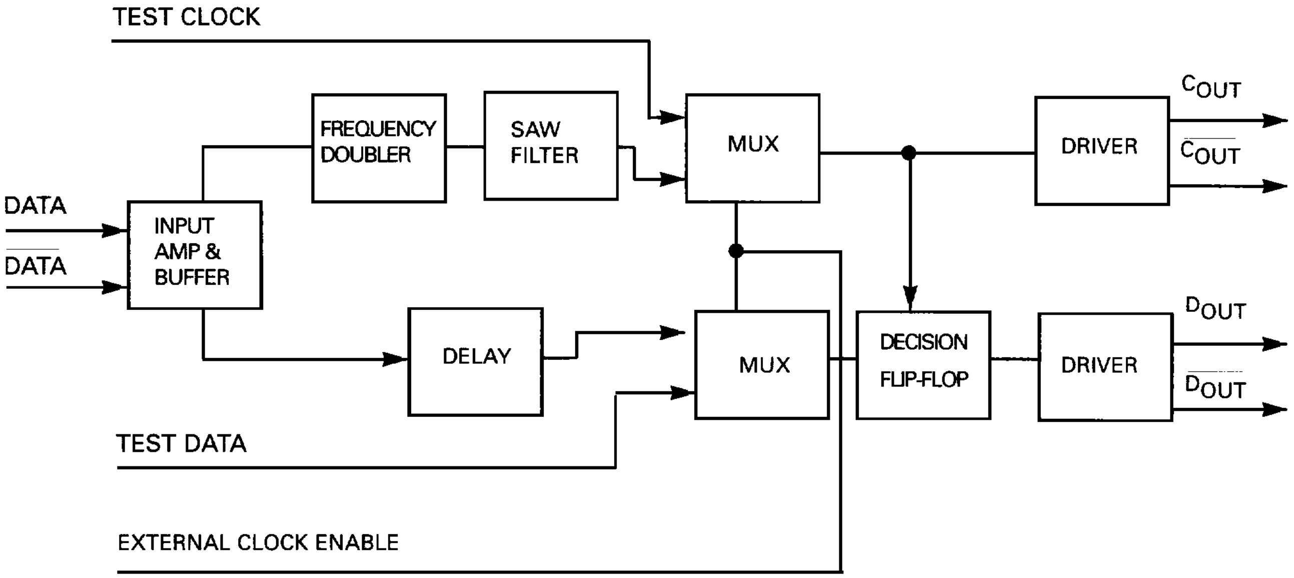


Figure 1. TRU600A Simplified Block Diagram

Pin Information

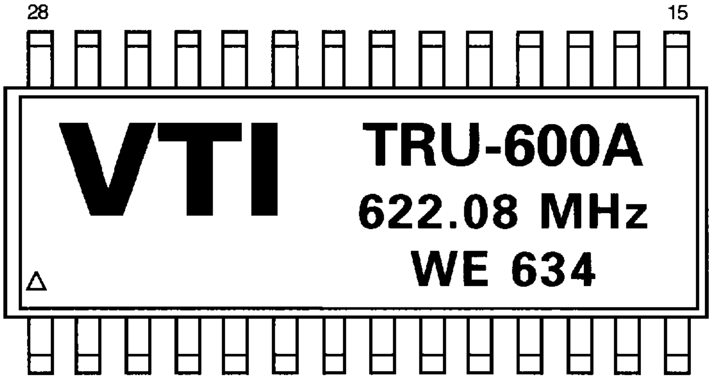


Figure 2. Pin Diagram

Table 1. Pin Descriptions

Pin #	Symbol	Description
2	TDI	Test data in
4	D_{OUT}	Retimed data out.
6	$\overline{D_{OUT}}$	Complementary retimed data out.
8	TCI	Test clock in
10	C_{OUT}	Recovered clock output.
12	$\overline{C_{OUT}}$	Complementary recovered clock output.
14	ECE	External Clock Enable
16	V_{CC}	Positive supply voltage.
19	V_{EE}	Negative supply voltage.
21	V_{CC}	Positive supply voltage.
23	$\overline{D_{IN}}$	Complementary data input.
25	D_{IN}	Data input.
1, 3, 5, 7, 9, 11, 13, 15, 17, 18, 20, 22, 24, 26, 27, 28	Case	Case connected to circuit ground.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum ratings can cause permanent damage to this device. These are absolute stress ratings only. Functional operation of this device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to Absolute Maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Tstg	-55	125	°C
Soldering Temperature/Duration	TLS	–	240/10	°C/s
Supply Voltage	V_{CC}-V_{EE}	0	8.0	V

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. VTI employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the mode. Although no industry-wide standard has been adopted for the CDM, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Model	Minimum	Unit
Human body	1000	V
Charged Device	1000	V

Electrical Characteristics

TA=-40 ° C to +85 °C

Parameter	Symbol	Min	Typical	Max	Unit
Nominal Clock Frequency[1]	F_N	124.416	_	622.08	MHz
Supply Current	I_{EE}	50	65	75	mA
Supply Voltage	V_{CC}	4.5	5	5.5	V
Data Input Voltage Low	V_{IL}	-1.81	-	-1.48	V
Data Input Voltage High	V_{IH}	-1.17	_	-0.88	V
Data/Clock Output Voltage Low[2]	V_{OL}	-1.95	_	-1.63	V
Input Clock /Frequency Deviation[3]	D_C	-200	_	200	ppm
Clock/Data Alignment[4]	T_{CDA}	-100	_	100	ps
Data/Clock Output Rise Time[5]	T_{TLH}	275	375	575	ps
Data/Clock Output Fall Time[5]	T_{THS}	275	375	575	ps
Output Clock Duty Cycle	-	45	-	55	%
Acquisition Time[6]	T_A	-	-	2	µs
Output Clock Random Jitter[7]	J_C	-	10	-	ps rms
Power Consumption	P_d	_	325	_	mW

1. The TRU600 meets all SONET/SDH requirements for jitter transfer and jitter tolerance mask characteristics at the standard SONET transmission rates.
2. Measured with respect to V_{CC} with load RL of 50 ohms to V_{CC} - 2V. See Figures 3 and 4. ECL voltage levels are specified for dc measurement. An additional tolerance of 50 mV should be added for dynamic measurement.
3. Allowable input clock frequency variation with respect to the nominal clock frequency (F_N) over the entire operating temperature range.
4. Alignment of clock and data outputs (see Figure 5).
5. Measured at 20% to 80% levels.
6. Time required to achieve valid data and clock outputs with an input transition density of at least 50%.
7. Measured with an input data pseudorandom word (PRW) 2^{23}-1.

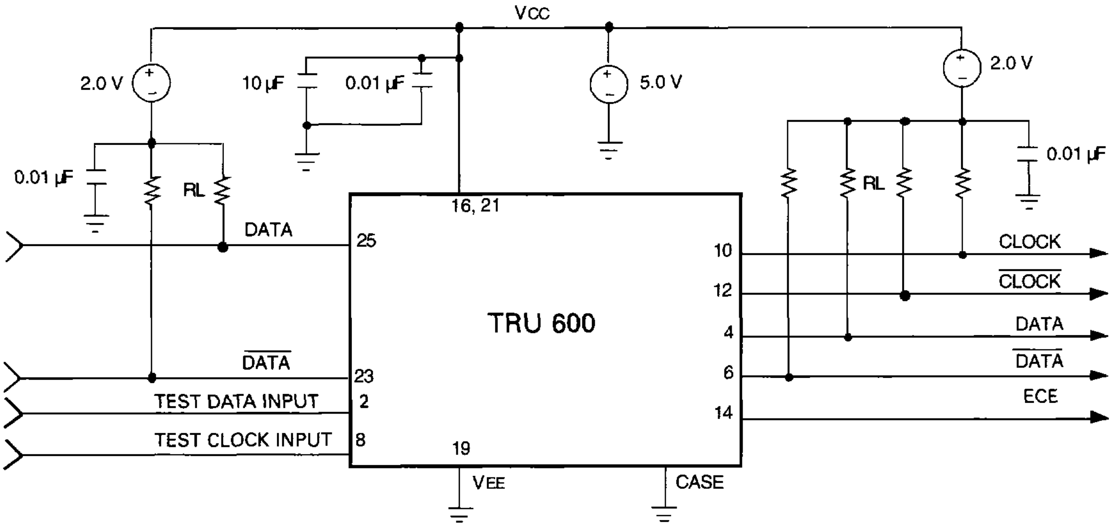


Figure 3. Positive Power Supply configuration

Electrical Characteristics (continued)

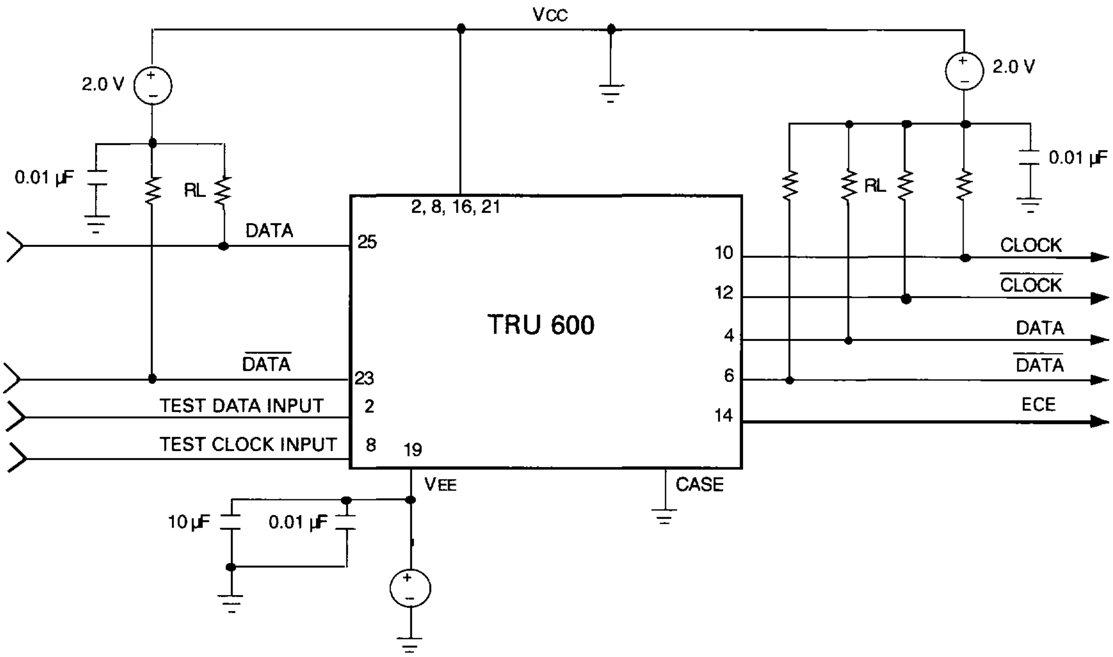


Figure 4. Negative Power Supply Configuration

Notes:

Pins 16 and 21 provide the power V_{CC} connections. Bypass capacitors should be located close to these pins in the positive supply configuration.

When used on a positive supply, all inputs and outputs are ECL referenced to V_{CC}.

The data inputs are internally tied to V_{BB} (V_{CC}-1.3 V) through 400 ohm resistors. For single ended or ac coupling, external biasing of the inputs is not required.

All outputs are open-emitter circuits and may be terminated with any standard ECL configuration.

Unused clock and data outputs should be terminated in the same manner as used outputs.

Case connections can be made at pins 1, 3, 5, 9, 11, 13, 15, 17, 18, 20, 22, 24, 26, 27, and 28.

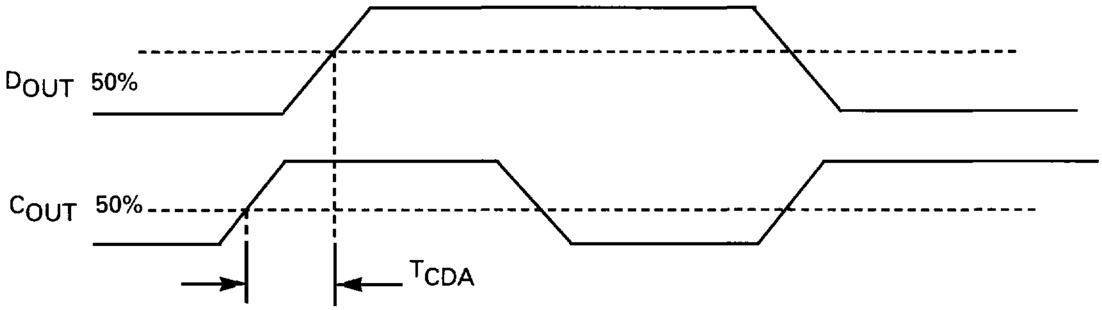
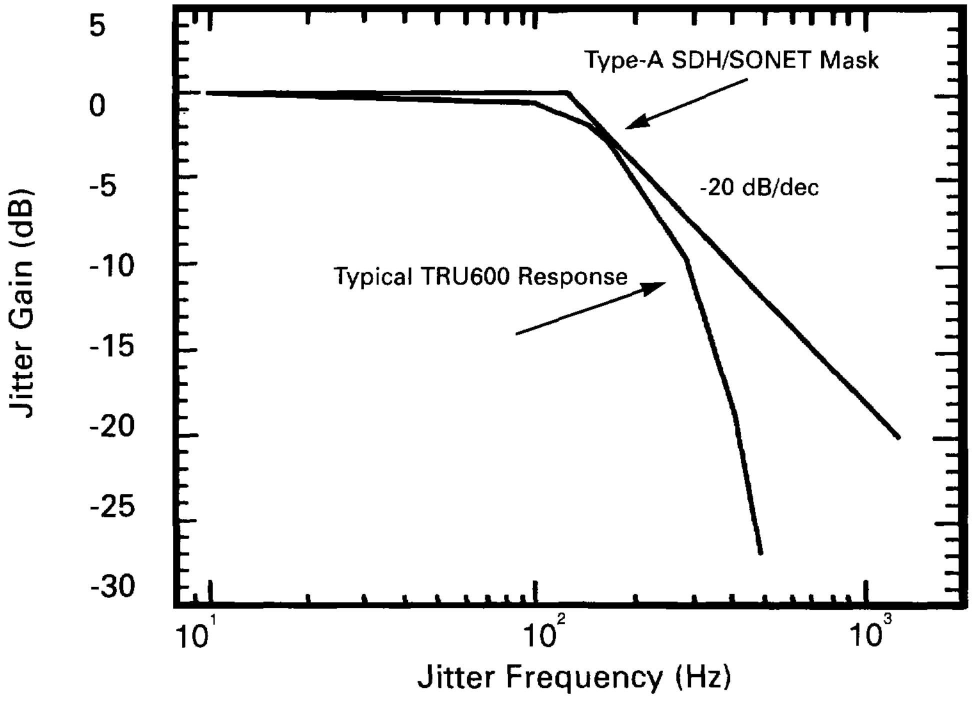
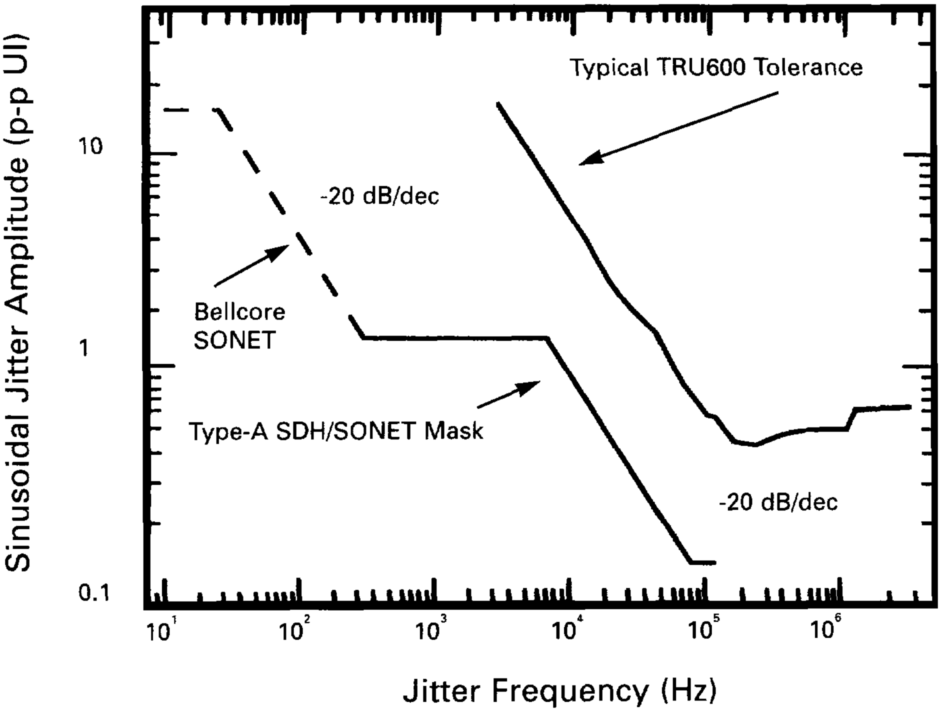


Figure 5. Clock / Data Alignment (T_{CDA})



OC-3 Jitter Transfer Function

Figure 6



OC-3 Jitter Tolerance

Figure 7

Mechanical Characteristics

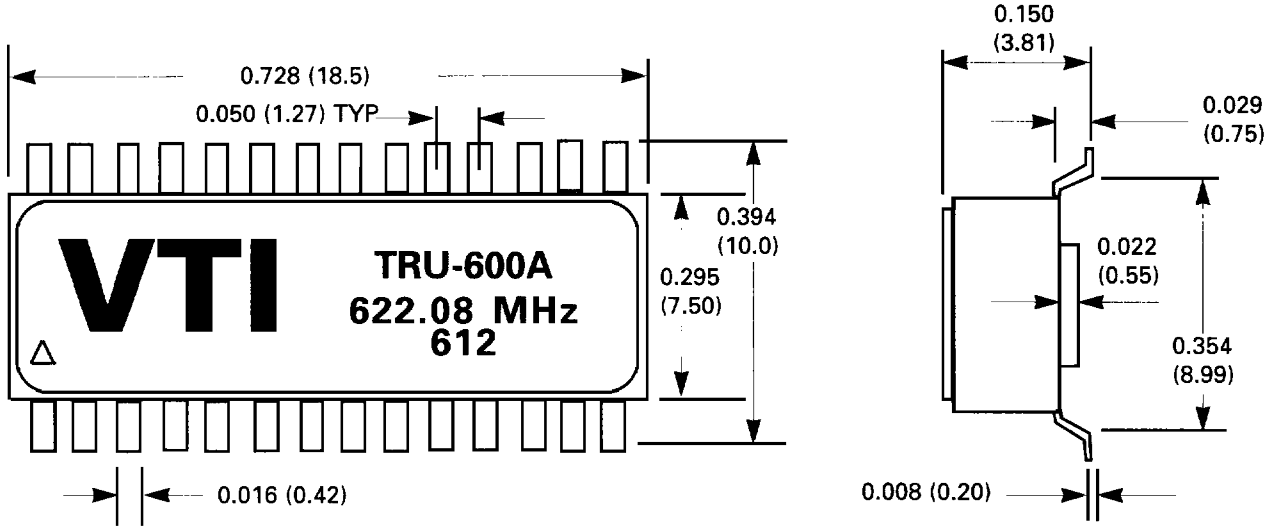
Table 5. Mechanical and Environmental Conditions

Parameter	Value
Mechanical Shock	MIL-STD-883C 2002.3 Test A
Mechanical Vibration	MIL-STD-883C 2007.1 Test A
Solderability	MIL-STD-883C 2003.5
Gross Leak Test	MIL-STD-883C 1014.7 (All Devices Tested)
Fine Leak Test	MIL-STD-883C 1014.7 (All Devices Tested)
Storage Temperature	-55 °C to +125 °C
Resistance to Solvents	MIL-STD-883C M2016

Outline Diagram

TRU600 Package

Dimensions are in inches and (millimeters).



Ordering Information

Standard Frequency (MHz)*	Part Number
124.416	C107316424
155.520	C107208670
155.520 (Tape and Reel)	C106859002
278.528	C107316440
311.040	C107097933
622.080	C106859028
622.080 (Tape and Reel)	C107208662

*Other frequencies available upon request.