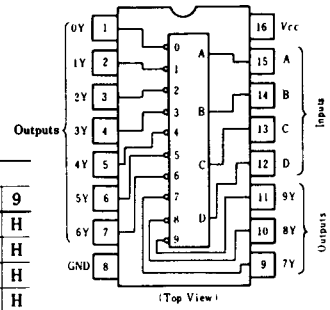
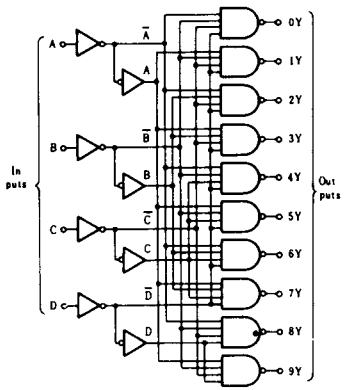
HD74LS42 ●BCD-to-Decimal Decoder

This monolithic decimal decoder consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

■PIN ARRANGEMENT



■BLOCK DIAGRAM



■FUNCTION TABLE

No.	BCD Input				Decimal Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H; high level, L; low level

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	–	–	V
	V_{IL}			–	–	0.8	V
Output voltage	V_{OH}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V, I_{OH}=−400μA		2.7	–	–	V
	V_{OL}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V	I_{OL}=8mA	–	–	0.5	V
			I_{OL}=4mA	–	–	0.4	
Input current	I_{IH}	V_{CC}=5.25V, V_I=2.7V		–	–	20	μA
	I_{IL}	V_{CC}=5.25V, V_I=0.4V		–	–	−0.4	mA
	I_I	V_{CC}=5.25V, V_I=7V		–	–	0.1	mA
Short-circuit output current	I_{OS}	V_{CC}=5.25V		−20	–	−100	mA
Supply current	I_{CC}**	V_{CC}=5.25V		–	7	13	mA
Input clamp voltage	V_{IK}	V_{CC}=4.75V, I_{IN}=−18mA		–	–	−1.5	V

* V_{CC} = 5V, Ta = 25°C
** I_{CC} is measured with all outputs open and all inputs grounded.

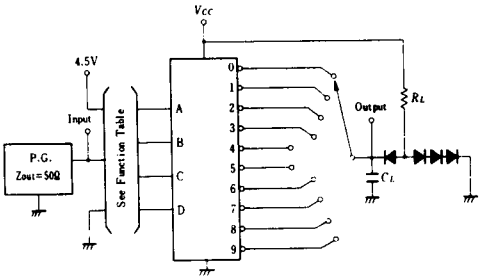
HITACHI
Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300

■SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃)

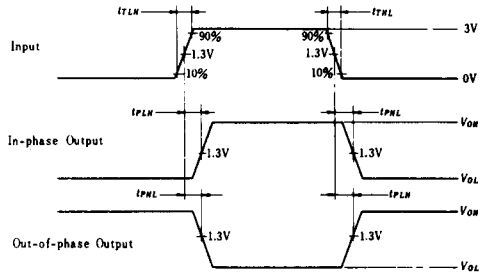
Item		Symbol	Test Conditions	min	typ	max	Unit
Propagation delay time	2 Stage	t_{PLH}	C_L=15pF, R_L=2kΩ	–	15	25	ns
	3 Stage			–	20	30	
	2 Stage	t_{PHL}		–	15	25	ns
	3 Stage			–	20	30	

■TESTING METHOD

1) Test Circuit



Waveform



Input pulse: $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, PRR=1MHz, duty cycle 50%.

PACKAGING INFORMATIONS

T-90-20

Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

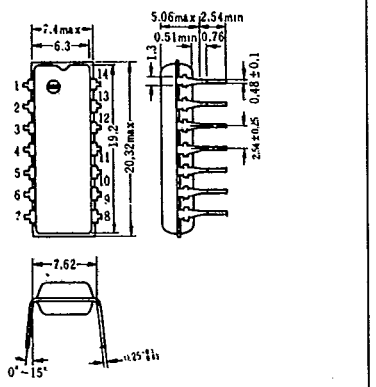
HD 74LS00 P

- Package ; Plastic DIP ; letters P
  Cerdip ; non-letters
- Circuit description
- Prefix : HD ; Hitachi Digital IC

■Plastic DIP

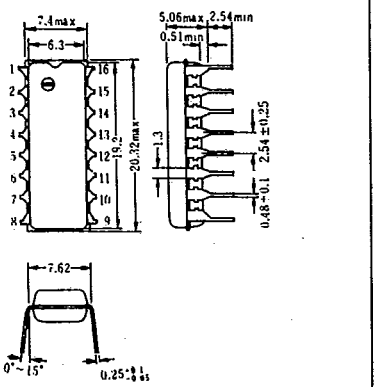
●14 Pin

DP-14



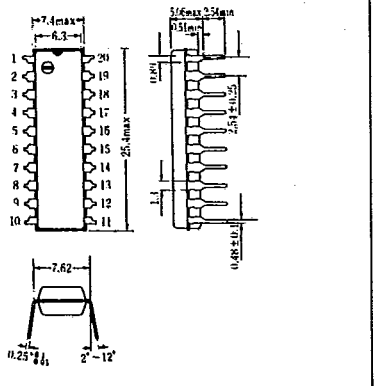
●16 Pin

DP-16



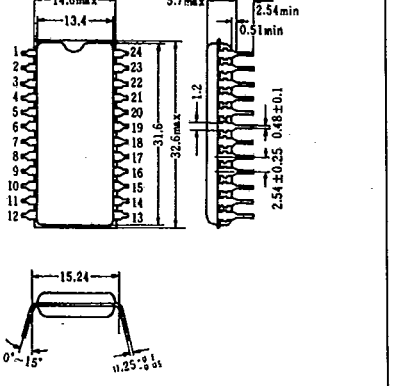
●20 Pin

DP-20



●24 Pin

DP-24

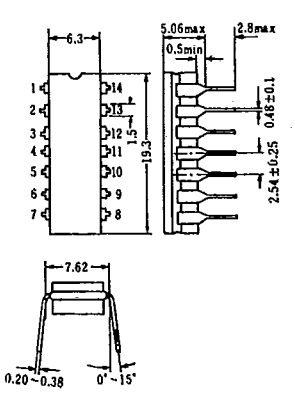


PACKAGING INFORMATIONS

■Cerdip

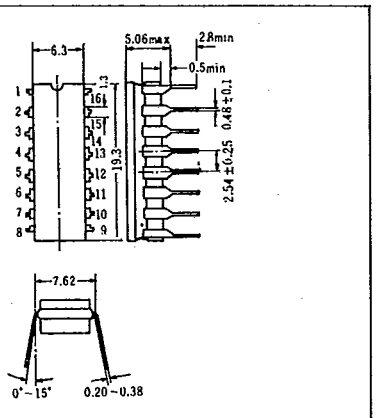
●14 Pin

DG-14



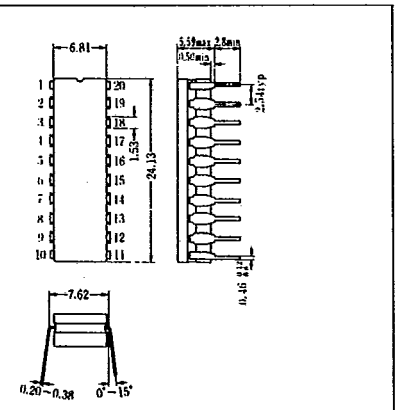
●16 Pin

DG-16



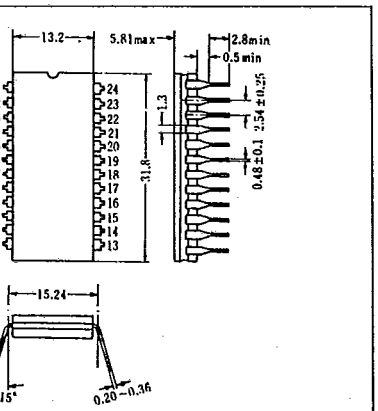
●20 Pin

DG-20



●24 Pin

DG-24



HITACHI
Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300